Datasheet Confidential

ADS6102

1D Time of Flight Sensor – OLGA12

Version 1.1 | May. 4, 2023

[Note]

Please be aware that most values written in the datasheet are in the **preliminary stages**.

As continual tests and improvements are being implemented, Adapts Photonics reserves the right to change any information without prior notice.

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Revision History

Version	Date	Description
0.1	Sep 1, 2021	Initial Version
1.0	April 28, 2023	For smart phone application, 1.8V IO only, Part number ADS6102C01BEO5X
1.1	May 3, 2023	Tape's outline drawing updated

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1. Introduction

Features & Benefits

- **High accuracy multi objects detection ranging sensor.**
  - Single Photon Avalanche Photodiode (SPAD) histogram-based architecture
  - Typical full FoV: 25° single zone detect with multi-objects detection (three objects).
  - High accurate detection with long and short distance.
  - Up to 5000 mm detection with full field of view (FoV)
  - 60 Hz frame rate capability (turn the laser pulse to option the different frame rate.)

- **Fully integrated module with flexible function behavior**
  - Size: 4.4 mm × 2.4 mm × 1.0 mm
  - Invisible light vertical cavity surface emitting 940nm laser (VCSEL) and integrated pulse laser driver.
  - Ultra-low power without firmware update.

- **Easy integration**
  - Single reflowable component.
  - Flexible communication bus integrating includes I^2C interface.
  - I^2C interface (up to 1MHz).
  - Provide interrupt GPIO pin for frame ready event.
  - Flexible power supply options, single 3.3V or 2.8V operation.
  - Works with many types of cover glass materials and compensate for smudge on glass.
  - Class 1 Eye Safety.

Description

The ADS6102 is a direct time-of-flight (dTOF) sensor module, with 940 nm VCSEL and VCSEL driver integrated. The TOF sensor has DSP module which can report distance information by its excellent algorithm. This device can achieve 5000^{+} mm detection range.

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Applications

This TOF sensor can be used in many applications including:

- Assist camera auto-focus; enhance the camera auto-focus (AF) system performance. Improve camera performance in low light and low contrast scenes.
- Presence detection for laptop.
- Collision avoidance for robots.
- 1D gesture recognition.
- 1D distance measurement of Lidar application.
- IoT (User and object detection).
- Video focus tracking assistance.



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2. ADS6102 Module Description

2.1. Block Diagram

The function blocks of this device are as shown below:

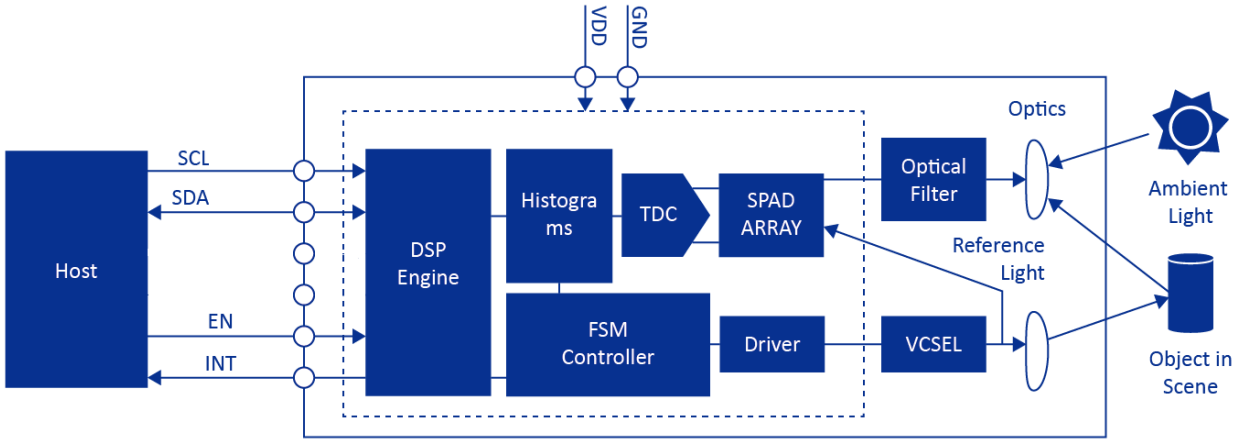


Figure 2-1 ADS6102 Block Diagram

2.2. Pin Diagram

Modules that using I²C communication, please refer to section 2.3. for detailed description about these pins.

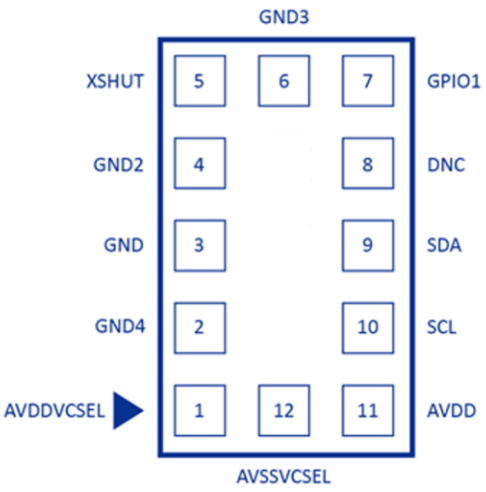


Figure 2-2 ADS6102 Pin Diagram (TOP VIEW)

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2.3. Pin Description

Table 2-1 Pin Description

Pin Name	Pin Number	Signal Type	Description
AVDDVCSEL	1	Power supply	VCSEL supply, to be connected to main supply
GND4	2	Ground	to be connected to main ground
GND	3	Ground	to be connected to main ground
GND2	4	Ground	to be connected to main ground
XSHUT	5	Digital input	Xshutdown pin, active low
GND3	6	Ground	to be connected to main ground
GPIO1	7	Digital output	Interrupt pin
DNC	8	VCCIO	Do not connect to GND, must be floating (Default)
SDA	9	Digital IO	I^2C data
SCL	10	Digital input	I^2C clock input
AVDD	11	Power supply	Supply, to be connected to main supply
AVSSVCSEL	12	Ground	VCSEL ground, to be connected to main ground

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3. Electrical Characteristics

3.1. Absolute Maximum Ratings

Table 3-1 Electrical Parameters

Symbol	Parameter	Min.	Max.	Unit
AVDD, AVDDVSCEL	Supply 3V Voltage to GND	-0.3	3.6	V
GND, GND2, GND3, GND4, AVSSVCSEL	Ground	0	0	V
GPIO1	Digital output	-0.3	2	V
SDA	Digital I/O	-0.3	2	V
SCL	Digital input	-0.3	2	V
XSHUT	Analog input	-0.3	2	V

3.2. Digital input and output

Table 3-2 Electrical Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
GPIO pins					
VIL	Low level input voltage	-0.3	-	0.3 * IOVCC	V
VIH	High level input voltage	0.7 * IOVCC		1.1*IOVCC	
VOL	Low level output voltage (I_{out} = 6mA)	-		0.4	
VOH	High level output voltage (I_{out} = 6mA)	0.8 * IOVCC		-	
IIL	Low level input leakage@ Vi = 0V	-0.15		0.15	uA
IIH	High level input leakage@ Vi=1.1*IOVCC	-10		10(1)	
XSHUT Pin					
VIL	Low level input voltage	-0.3	-	0.5	V
VIH	High level input voltage	1.17		1.1*IOVCC	
IIL	Low level input leakage@ Vi = 0V	-0.15		0.15	uA
IIH	High level input leakage@ Vi=1.1*IOVCC	-10		10	

Note(1): When IOVCC using external VCC, IIH ＜30uA @Temp ＞ 60°

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3.3. ESD

Electrostatic discharge

The ADS6102 module is compliant with electrostatic discharge (ESD) values presented in the table below.

Table 3-3 ESD Performance

Parameter	Specification	Condition
Human body model	JS-001-2017	± 2000V, 1500 Ohms, 100pF
Charged device model	JESD22-C101-C	± 500 V

3.4. Temperature

Table 3-4 Temperature Ranges and Storage Conditions

Symbol	Parameter	Min.	Max.	Unit	Comments
T_{STRG}	Storage Temperature Range	-40	85	°C	
T_{BODY}	Package Body Temperature		260 °C (max)	°C	IPC / JEDEC J-STD-020 The reflow peak soldering temperature (body temperature) is specified according to IPC / JEDEC J-STD-020 “Moisture / Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices.”
RH_{NC}	Relative Humidity (non-condensing)		85	%	

3.5. MSL

Moisture sensitivity level

Moisture sensitivity level (MSL) is level 3 as described in IPC/JEDEC JSTD-020-C

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3.6. Typical Operating Conditions

Device parameters are guaranteed at nominal conditions unless otherwise noted. While the device is operational across the temperature range, functionality will vary with temperature.

Table 3-5 Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
AVDD，AVDDVCSEL	Supply 3.3V Voltage to GND	2.8	3.3	3.6	V
VCCIO	Internal 1.8V, self-supporting	1.68	1.8	2	V
GPIO1	Digital I/O with internal VCCIO	1.62	1.8	2	V
SDA	Digital I/O with internal VCCIO	1.62	1.8	2	V
SCL	Digital input with internal VCCIO	1.62	1.8	2	V
XSHUT	Analog input with internal VCCIO	1.62	1.8	2	V
Temperature Range	Free-air temperature	-20	25	85	°C

Note*: XSHUT: VIL650mV, VIH850mv

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3.7. Power Consumption

Table 3-6 Power consumption with typical condition

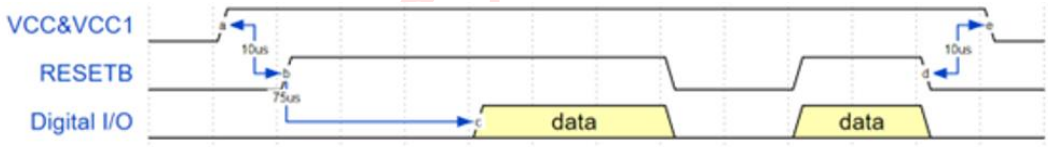
Mode	Typ.	Unit	Duty Ratio
Idle (1)	11	μA	Re-initialization required
Active Ranging (1)	26	mA	Ranging 30 Hz, 33 ms, default settings

Note 1. Temperature and voltage are nominal conditions (25 "C and 3.3V)

3.8. Operation Sequence

In Power up sequence, VCC1 and VCC should be powered up at the same time. After power up, the XSHUT pin can be set to 1 after a 10 us delay. Digital I/O can be ready for operation after another 75us delay.

In Power down sequence, to avoid electricity leakage, XSHUT(RESETB) pin must be set to 0 before VCC&VCC1 is powered down. This time delay is 10us.



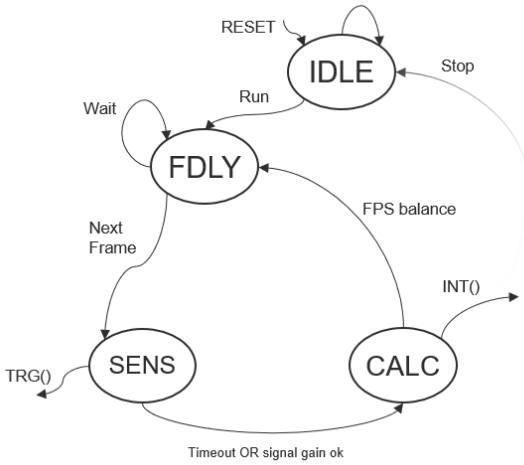
Digital I/O include INTR, GPIO2, SDA, SCL,XSHUT.

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3.9. State Machine

ADS6102 system is controlled by a Finite State Machine. The diagram of the state machine is shown below:



The FSM is in default IDLE state after power up. During this state, Driver will do housekeeping sequence to setup, and configure the chip to expected working mode.

Then the software driver will configure the chip to enter working mode. In working mode, chip will enter FDLY state first. As for each FRAME, this state will help balance the Frame period configured by registers.

After each frame delay cycle has finished, FSM will start sensing, this is SENS state. In this state, chip will trigger multiple configured laser pulses, and for each trigger, wait for configured times based on configured clock frequency. The time of SENS state can be configured by two aspects, 1st is highest signal value, when the max value in histogram reached configured value, SENS state will finish and FSM proceed to next state; 2nd is timeout, if maximum (timeout) flashes reached, before max histogram value reached its threshold, FSM will also move on to CALC state.

CALC state is for point distance calculation, during this state, histogram will be processed by internal DSP. After the DSP processing has finished, an interrupt request will be sent out to chip, generating an interrupt. FSM move on to FPS balance, and then start the next frame.

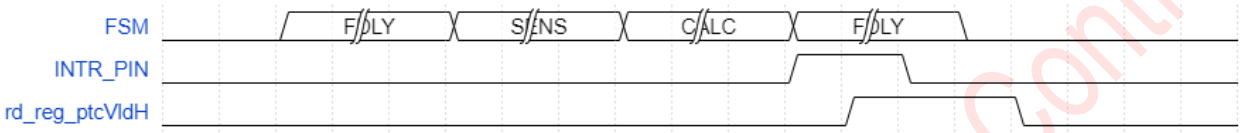
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3.10. Interrupt Behavior and Timing

The INTR_PIN is level-sensitive interrupt pin which can be HIGH active.

The interrupt will be HIGH at the end of each frame and can be cleared by reading register ptcVldH.



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4. Optical Characteristics

4.1. VCSEL Electrical and Optical Characteristics

4.1.1. Electrical-Optical Characteristics

Table 4-1 Electrical-Optical Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Threshold Current	I_{th}		5		mA	
Output Power	P_o	18	21		mW	I_F =30mA
Slope Efficiency	η		1		W/A	
Forward Voltage	V_F	1.7	2		V	I_F =30mA
Conversion efficiency	PCE		42		%	I_F =30mA
Wavelength	λ_P	930	940	950	nm	I_F =30mA
Wavelength Shift			0.07		nm / ℃	
Beam Divergence	θ		25		degree	I_F =30mA (1/e^2)

Note*: All parameters except mentioned are measured at 25 ℃, CW operation.

4.1.2. VCSEL Beam Divergence

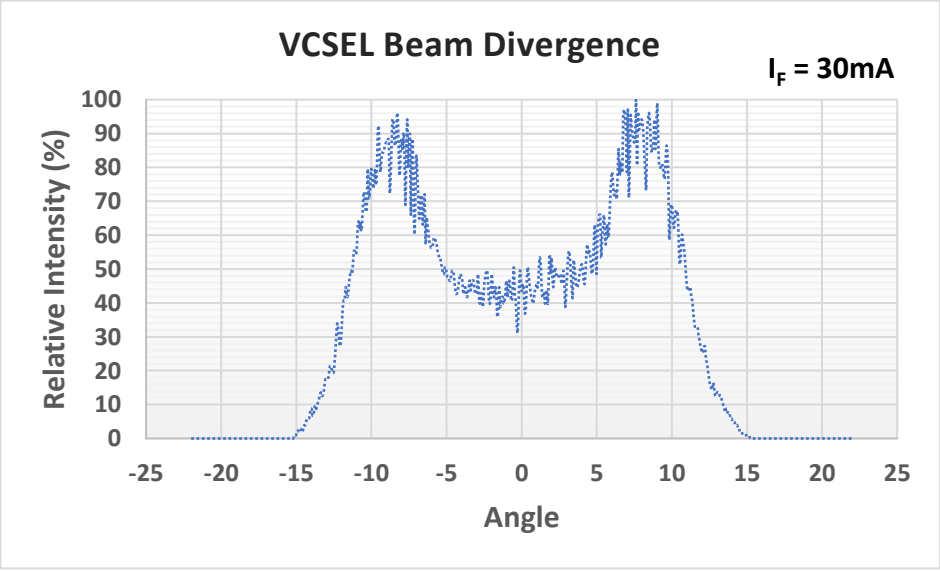


Figure 4-1-2 VCSEL Beam Divergence

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4.2. IR Bandpass Filter Characteristics

The ADS6102 has IR bandpass filter which improves the time-of-flight measurement performance.

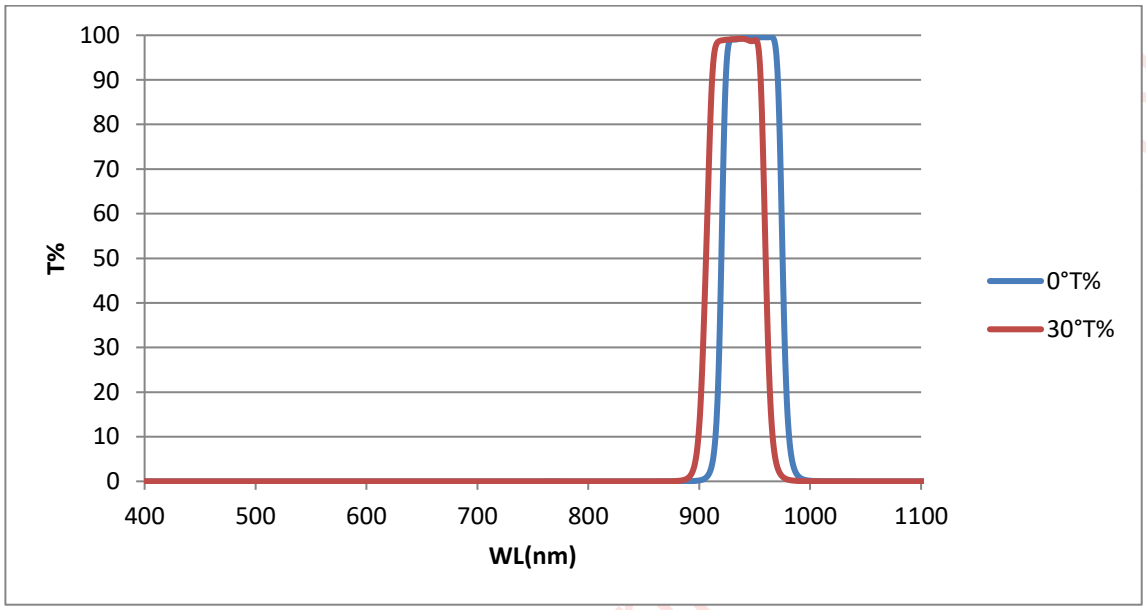


Figure 4-3-1 Cut Band (400 ~ 900 & 995 ~ 1100)

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5. Communication Interfaces

5.1. I²C

5.1.1. I²C Protocol

The device uses I²C serial communication protocol for communication. The device supports 7-bit chip addressing and both standard and full-speed clock frequency modes. Read and Write transactions comply with the standard set by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification.

Internal to the device, an 8-bit buffer stores the register address location of the desired byte to read or write. This buffer auto-increments upon each byte transfer and is retained between transaction events (i.e. valid even after the master issues a STOP command and the I²C bus is released). During consecutive Read transactions, the future / repeated I²C Read transaction may omit the memory address byte normally following the chip address byte; the buffer retains the **last register address +1**.

All 16-bit fields have a latching scheme for reading and writing. In general, it is recommended to use I²C bursts whenever possible, especially in this case when accessing two bytes of one logical entity. When reading these fields, the low byte must be read first, and it triggers a 16-bit latch that stores the 16-bit field The high byte must be read immediately afterwards. When writing to these fields, the low byte must be written first, immediately followed by the high byte. Reading or writing to these registers without following these requirements will cause errors.

A Write transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS WRITE. DATA BYTE (S), and STOP. Following each byte (9TH clock pulse) the slave places an ACKNOWLEDGE / NOT-ACKNOWLEDGE (ACK / NACK) on the bus. If NACK is transmitted by the slave, the master may issue a STOP.

A Read transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS, RESTART, CHIP-ADDRESSREAD, DATA BYTE (S), and STOP. Following all but the final byte, the master places an ACK on the bus (9TH clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

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5.1.1.1. The I²C Device Address

The Sensor contains eight-bit registers accessed via the I²C bus. All operations can be controlled by the command register. The simple command structure makes user easy to configure the operation setting and latch the output data from the Sensor.

The Sensor provides fixed I²C slave address of **0x10 or 0x01** (default) using 7 bit addressing protocol.

The address is record in the OTP during the CP testing process.

Table 5-1 Slave Address

7-bit Slave Address	R / W Command Bit 0	OPERATION
0x10 or 0x01	0	Write Command to Sensor
	1	Read Data from Sensor

5.1.2. I²C Write

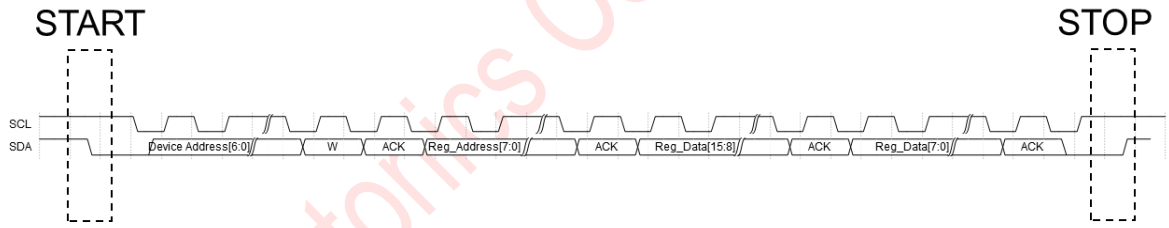


Figure 5-1 I²C Write

5.1.3. I²C Read

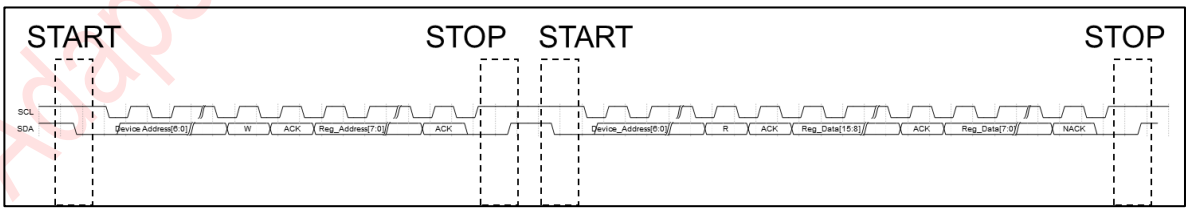


Figure 5-2 I²C Read

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5.1.4. I²C Sequential Read with STOP / START

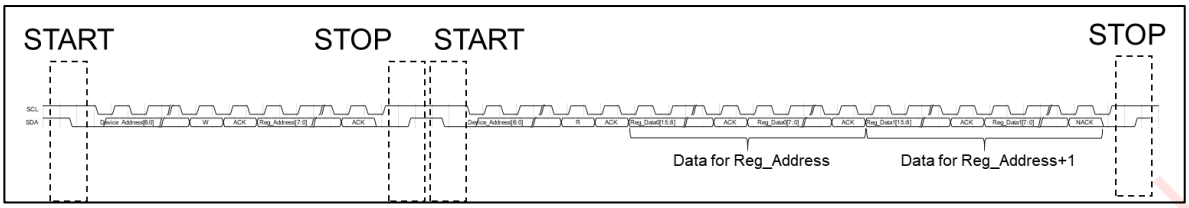


Figure 5-3 I²C Sequential Read with STOP / START

5.1.5. I²C Sequential Read with RESTART

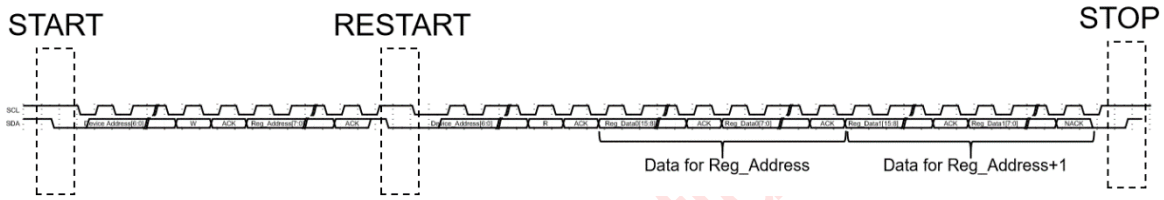


Figure 5-4 I²C Sequential Read with RESTART

5.1.6. I²C Sequential Write

Notice: with I²C squential write mode, support Regsiters and RAM

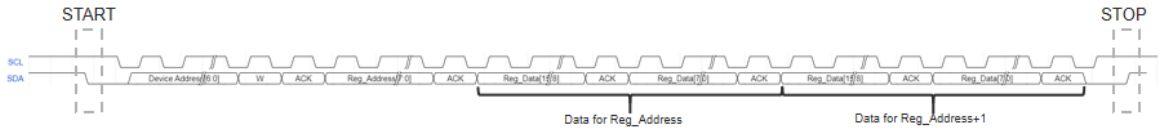


Figure 5-5 I²C Sequential Write

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5.1.7. I²C Timing Specification

The I²C Timing Specification is as shown in Table 5-2 and Figure 5-6.

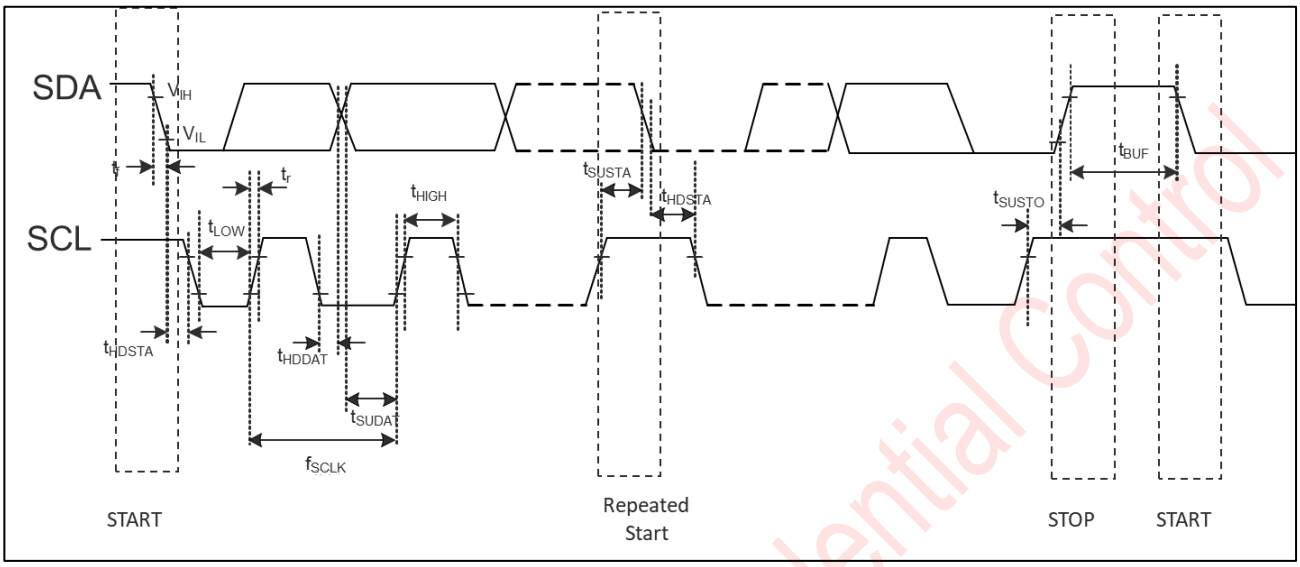


Figure 5-6 I²C Timing Specification

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Table 5-2 I²C Timing Specification

Symbol	Parameter	Standard Mode		Fast Mode		Fast Plus Mode		Unit
		Min.	Max.	Min.	Max.	Min.	Max	
F_{SCL}	SCL clock frequency	0	100	0	400	0	1000	KHz
$t_{HD.STA}$	Hold time after (repeated) start condition. After this period, the first clock is generated.	4.0	-	0.6	-	0.26	-	us
t_{LOW}	Low period of the SCL clock	4.7	-	1.3	-	0.5	-	us
t_{HIGH}	HIGH period of the SCL clock	4.0	-	0.6	-	0.26	-	us
$t_{SU.STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	0.26	-	us
$t_{HD.DAT}$	Data in hold time	0.25	-	0.25	-	0.25	-	us
$t_{SU.DAT}$	Data in setup time	250	-	100	-	50	-	ns
t_R	Rise time of both SDA and SCL signals	-	1000	-	300	-	120	ns
t_F	Fall time of both SDA and SCL signals	-	300	-	300	-	120	ns
$t_{SU.STO}$	Set-up time for STOP condition	4.0	-	0.6	-	0.26	-	us
t_{BUF}	Bus free time between STOP and START condition	4.7	-	1.3	-	0.5	-	us

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6. Ranging Performances

6.1. Ranging Accuracy

Measurement conditions:

- The full of FOV (full of view) is covered by 25°.
- Targets used are grey (18 % reflectance) and white (88 % reflectance).
- Normal voltage supply (2.8V or 3.3V) and temperature (23 °C).
- Indoor: No external light within the wavelength band 940nm, +/- 30nm.
- All tests are performed without cover glass.
- Range 10 mm~5000 mm.
- Typical samples used.

Table 6-1 Summary of ADS6102 ranging performances.

Target reflectance	Performance		Dark
White 88 %	Max distance		5000mm
	Accuracy	10~90 mm	±6.15mm
		90mm~110 mm	±4.39%
		110~5000 mm	±1.21%
Grey 18 %	Max distance		2900mm
	Accuracy	10~90 mm	±7.0mm
		90mm~110 mm	±4.39%
		110~2900 mm	±1.84%

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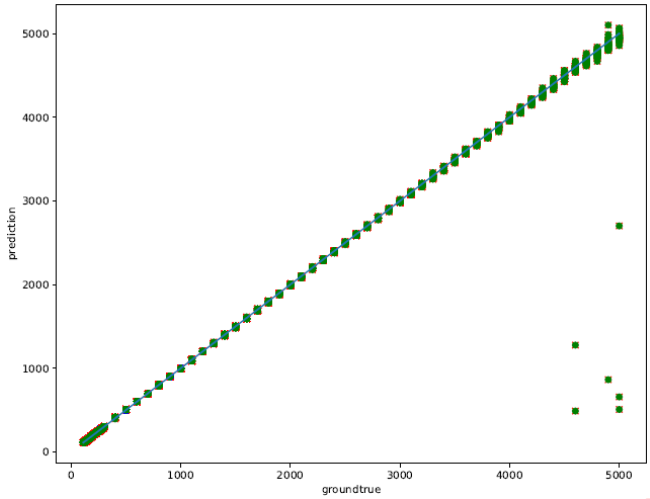


Figure 6-1 88 % White Card, ranging distance 110 mm to 5000 mm

Measurement conditions for ambient light:

- The full of FOV (full of view) is covered by 25°
- Targets used are grey (18 % reflectance) and white (88 % reflectance).
- Normal voltage supply (2.8V or 3.3V) and temperature (23 ° C).
- Tests are performed with 1950 lux Halogen Lamp on (is equivalent to 10kLux sunlight).
- All tests are performed without cover glass.

Table 6-2 Summary of ADS6102 module ranging performances.

Target reflectance	Performance		Ambient (IR Light)
White 88 %	Max distance		2300 mm
	Accuracy	300 mm~2300 mm	±1.90%
Grey 18 %	Max distance		1700 mm
	Accuracy	300 mm~1700 mm	±4.12%

Note: IR light represents 10k sunlight equivalence; light on object only.

- Up to 2300mm detection distance with white targets with 88% reflectance.

  Up to 1700mm detection distance with grey targets with 18% reflectance.

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7. Register Description

7.1. CHIP_ID Register (Address 0x00)

Bit	Bit Name	Default	Access	Bit Description
15:0	CHIP_ID	0xA118	RO	Chip ID

7.2. I²C_ADDR Register (Address 0x01)

Bit	Bit Name	Default	Access	Bit Description
15	Reserved	0	RW	Reserved. Must be set to default value.
14:8	I²C_ADDR_1	0x10	RW	7bit I²C address 1
7	Reserved	0	RO	Reserved
6:0	I²C_ADDR_2	0x01	RW	7bit I²C address 2

7.3. CFG1 Register (Address 0x02)

Bit	Bit Name	Default	Access	Bit Description
15:11	Reserved	10110	RW	Reserved. Must be set to default value.
10	BST_NEXT	0	RW	This bit is to control the internal smudge calibration feature. 1: enable smudge calibration. 0: disable smudge calibration.
9	RMV_NEXT	0	RW	This bit is to control the internal cover glass calibration feature. 1: enable cover glass calibration. 0: disable cover glass calibration.
8:3	Reserved	000010	RW	Reserved. Must be set to default value.
2	Reserved	0	RW	Reserved. Must be set to default value.
1	CFG_DONE	0	RW	CFG_DONE is the bit to control internal state machine to measure or not. User should firstly configure all registers' value, then set this bit to 1 to start the measurement. 0: stop measurement. 1: start measurement. (bit 0 should be set to 1 firstly)
0	SLEEP	1	RW	1: default value, means sensor will enter sleep mode after initialization. 0: means sensor will exit sleep mode. Before starting to measure, this bit should be set to 0.

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7.4. CFG4 Register (Address 0x05)

Bit	Bit Name	Default	Access	Bit Description
15:3	Reserved	0	RW	Reserved. Must be set to default value.
3	GLB_SFT_RST	0	WO	Reset both logic and Reg
2	SOFT_RST	0	RW	Reset logic except Reg
1	INT_CLR	0	RW	Interrupt mask
0	Reserved	0	RW	Reserved. Must be set to default value.

7.5. PULSE_NUM Register (Address 0x06)

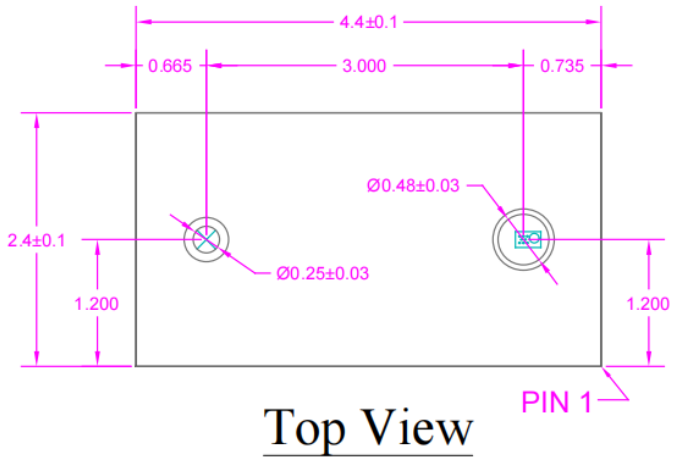
Bit	Bit Name	Default	Access	Bit Description
15:0	PULSE_NUM	0x4000	RW	Number of pulses to emit in each frame. This value is multiplied by 16 in hardware. Like a value of 1 means 16 pulses, a value of N means N*16 pulses.

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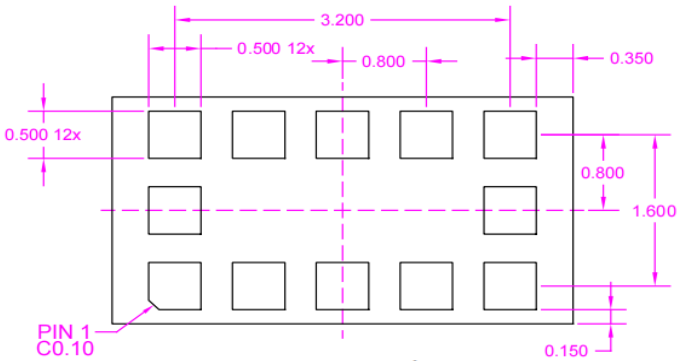
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8. Package Information

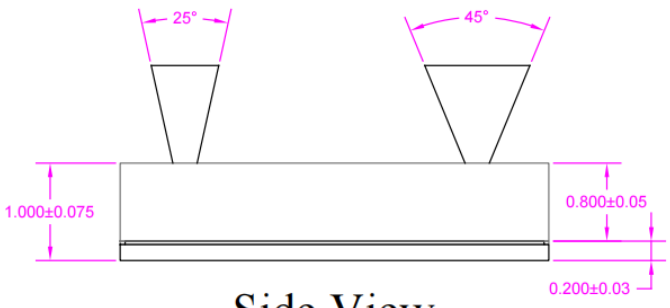
The ADS6102 module size is 4.4 mm x 2.4 mm x 1.0 mm. the package is reflowable component. The customer can integrate the ADS6102 in the system easily.



Top View



Bottom View

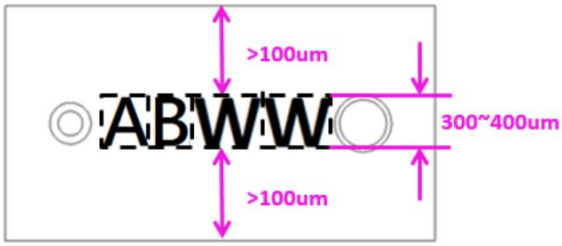


Side View

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ABWW（e.g.G236）

A : Device code

B: Year Code (B) Production Year (last digits of year)

WW: Production Code (WW) Weeks

Figure 8-1 MARKING INFORMATION

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9. Application Information

9.1. Application Schematic

Notes: GPIO1 as interrupt pin, shouldn't be pulled up

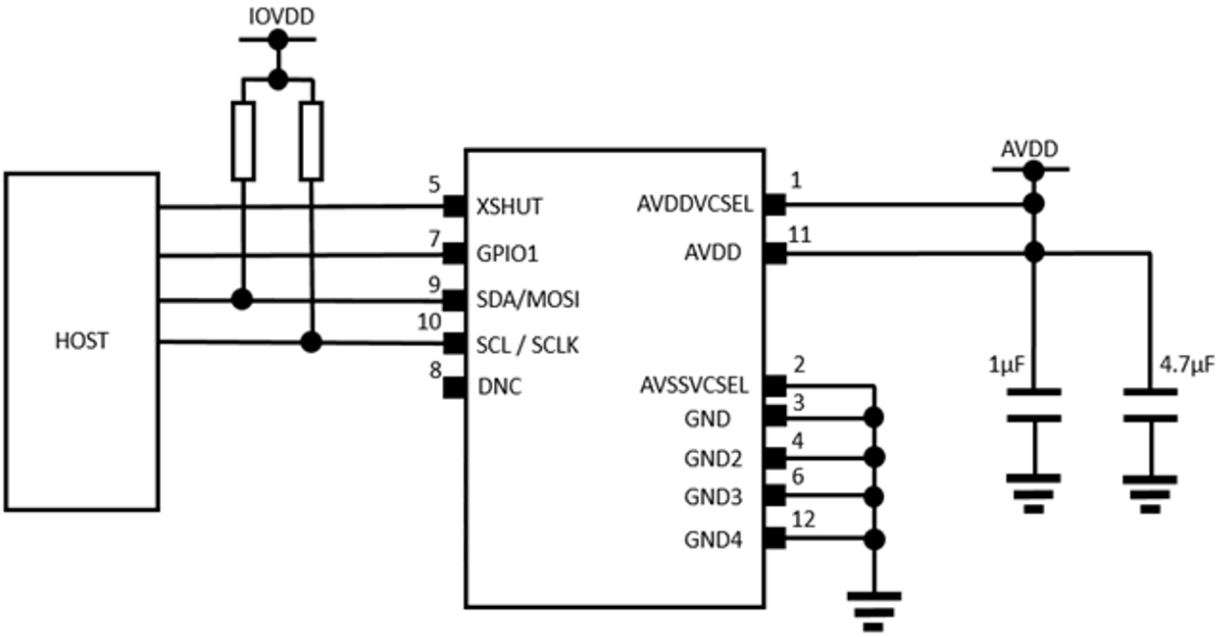


Figure 9-1 ADS6102 Application Schematic of I²C

9.2. Tape and outline drawing

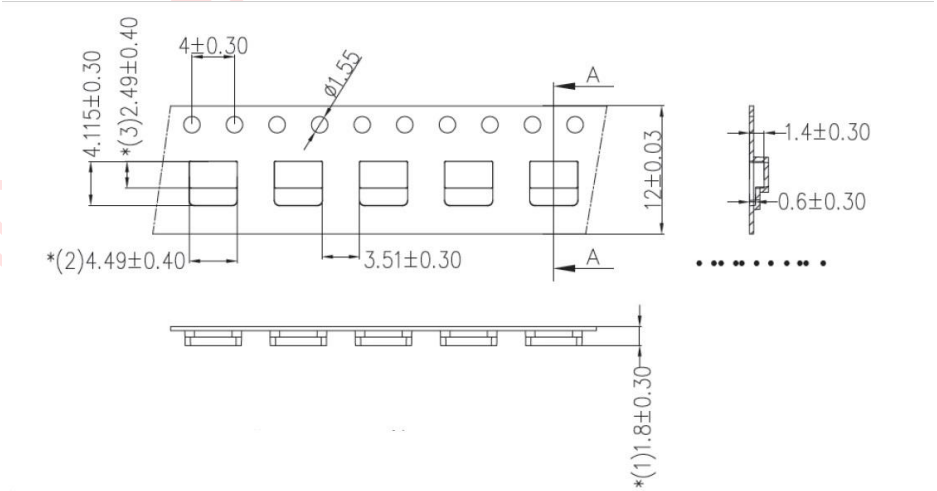


Figure 9-2 ADS6102 OLGA12 Tape and outline drawing

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10. Lead-free solder reflow process

Reflow Soldering	
Pre-heat	150~200°C
Pre-heat time	Max. 120 seconds
Peak temperature	Max. 260°C
Soldering time	Max. 10 seconds (Max. two times)

Table 10-1 Reflow Soldering

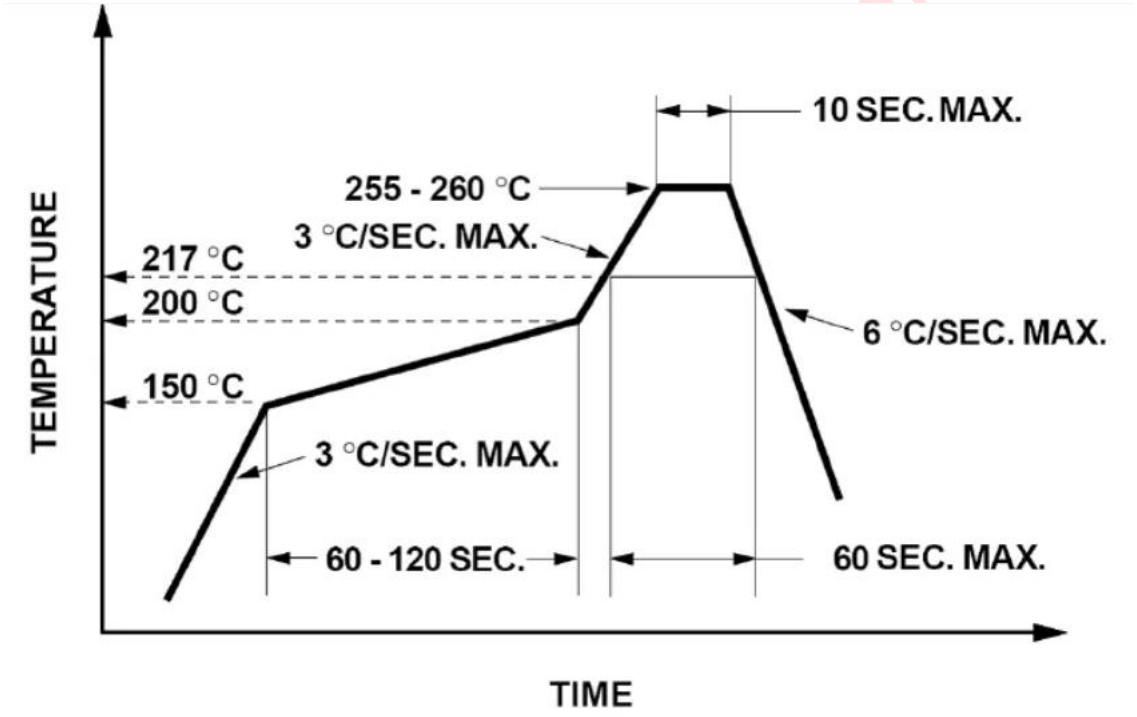


Figure 10-1 Reflow Soldering

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11. Laser Eye Safety

The ADS6102 contains a laser emitter and corresponding drive circuitry. The laser output is designed to remain within Class 1 laser safety limits under all reasonably foreseeable conditions including single faults in compliance with IEC 60825-1:2007 and IEC 60825-1:2014.

The laser output power must not be increased by any means and no optics should be used with the intention of focusing the laser beam.

Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.



Figure 11-1 Class 1 laser label

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12. Ordering Information

Table 12-1 Ordering Information

Order codes	Packing	Minimum Order Quantity
ADS6102C01BEO5X	OLGA12 with Tape and Reel	5000 pcs

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