CX25601N I²C Controlled 3.0-A Single Cell Battery Charger for High Input Voltage and Narrow Voltage DC (NVDC) Power Path Management

1 Features

- High-Efficiency, 1.1-MHz, Synchronous Switch Mode Buck Charger
  - 92.50% Charge Efficiency at 2 A from 5-V Input
  - 90.61% Charge Efficiency at 2 A from 9-V Input
  - Selectable Low Power Pulse Frequency Modulation (PFM) Mode for Light Load Operations
- Supports USB On-The-Go (OTG)
  - Boost Converter with Up to 1.2-A Output
  - 94.13% Boost Efficiency at 1-A Output
  - Accurate Constant Current (CC) Limit
  - Soft-Start Up To 500-µF Capacitive Load
  - Output Short Circuit Protection
  - Selectable Low Power PFM Mode for Light Load Operations
- Single Input to Support USB Input and High Voltage Adapters
  - Support 3.9-V to 13-V Input Voltage Range With 23-V Absolute Maximum Input Voltage Rating
  - Programmable Input Current Limit (100 mA to 3 A With 20-mA Resolution) to Support USB 2.0, USB 3.0 Standards and High Voltage Adaptors (IINDPM)
- High Battery Discharge Efficiency With 20-mΩ Battery Discharge MOSFET
- Narrow VDC (NVDC) power path management
  - Instant-On Works with No Battery or Deeply Discharged Battery
  - Ideal Diode Operation in Battery Supplement Mode
- BATFET Control to Support Ship Mode, Wake Up
- Flexible Autonomous and I2C Mode for Optimal System Performance
- High Integration Includes All MOSFETs, Current Sensing and Loop Compensation
- 1-µA Battery Leakage Current in ship mode
- High accuracy
  - ±0.5% charge voltage regulation
  - ±5% charge current regulation
  - ±5% input current regulation

2 Application

- Tablet
- Gaming and Computer Accessories
- Portable Medical Equipment

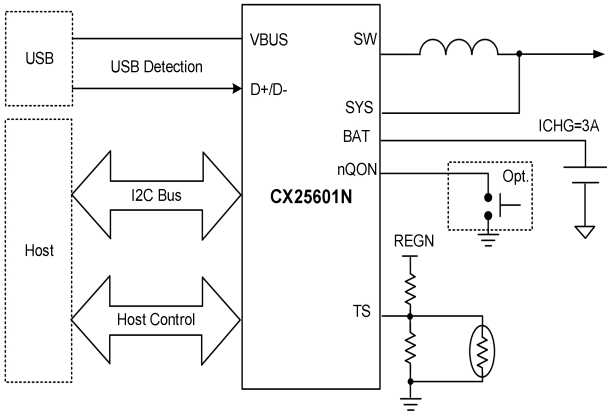
3 Description

The CX25601N device is a highly-integrated 3-A switch-mode battery charge management and system power path management device for single cell Li-Ion and Li-polymer battery. The low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life during discharging phase. The I²C serial interface with charging and system settings makes the device a truly flexible solutions.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CX25601N	WQFN (24)	4.00mm x 4.00mm

Simplified Schematic



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4 Description (continued)

The CX25601N is a highly-integrated 3.0-A switch-mode battery charge management and system power path management device for single cell Li-Ion and Li-polymer battery. It features fast charging with high input voltage support for a wide range of smart phones, tablets and portable devices. Its low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life during discharging phase. Its input voltage and current regulation deliver maximum charging power to battery. The solution is highly integrated with input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4) between system and battery. It also integrates the bootstrap diode for the high-side gate drive for simplified system design. The I^2C serial interface with charging and system settings makes the device a truly flexible solution.

The device supports a wide range of input sources, including standard USB host port, USB charging port, and USB compliant high voltage adapter. The device sets default input current limit based on the built-in USB interface. To set the default input current limit, the device takes the result from detection circuit in the system, such as USB PHY device. The device is compliant with USB 2.0 and USB 3.0 power specifications for input current and voltage regulation and meets USB On-the-Go (OTG) operation power rating specification with constant current limit up to 1.2A.

The power path management regulates the system slightly above battery voltage but does not drop below 3.52 V minimum system voltage (programmable). With this feature, the system maintains operation even when the battery is completely depleted or removed. When the input current limit or voltage limit is reached, the power path management automatically reduces the charge current to zero. As the system load continues to increase, the power path discharges the battery until the system power requirement is met. This Supplement Mode prevents overloading the input source.

The device initiates and completes a charging cycle without software control. It senses the battery voltage and charges the battery in three phases: pre-conditioning, constant current and constant voltage. At the end of the charging cycle, the charger automatically terminates when the charge current is below a preset limit and the battery voltage is higher than recharge threshold. If the fully charged battery falls below the recharge threshold, the charger automatically starts another charging cycle.

The charger provides various safety features for battery charging and system operations, including battery negative temperature coefficient thermistor monitoring, charging safety timer and overvoltage and overcurrent protections. The thermal regulation reduces charge current when the junction temperature exceeds 120°C (programmable). The STAT output reports the charging status and any fault conditions. Other safety features include battery temperature sensing for charge and boost mode, thermal regulation and thermal shutdown and input UVLO and overvoltage protection.

The device also provides nQON pin for BATFET enable and reset control to exit low power ship mode or full system reset function.

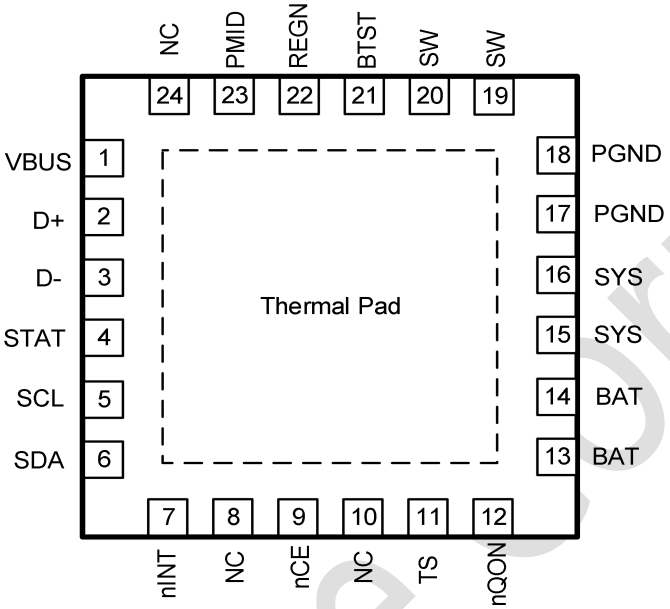
The device is available in 24-pin, 4 mm × 4 mm x 0.75 mm thin WQFN package.

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5 Pin Configuration and Functions

CX25601N
24-Pin WQFN
Top View



PIN Functions

PIN		TYPE(1)	DESCRIPTION
NAME	No.		
VBUS	1	AI	Charger Input Voltage. The internal n-channel reverse block MOSFET (RBFET) is connected between VBUS and PMID pins. Place a 1-uF ceramic capacitor from VBUS to GND close to device.
D+	2	AIO	Positive line of the USB data line pair. D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2, and Adjustable high voltage adapter.
D-	3	AIO	Negative line of the USB data line pair. D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2, and Adjustable high voltage adapter.
STAT	4	DO	Open drain charge status output to indicate various charger operation. Connect to the pull up rail via 10-kΩ resistor. LOW indicates charge in progress. HIGH indicates charge complete or charge disabled. When any fault condition occurs, STAT pin blinks in 1 Hz. The STAT pin function can be disabled when DIS_STAT bit is set.
SCL	5	DI	I^2C Interface clock. Connect SCL to the logic rail through a 10-kΩ resistor.
SDA	6	DIO	I^2C Interface data. Connect SDA to the logic rail through a 10-kΩ resistor.
nINT	7	DO	Charger Open-drain Interrupt Output. Connect the INT1 to a logic rail via 10-kΩ resistor. The INT1 pin sends active low, 256-μs pulse to host to report charger device status and fault.

(1) DI (Digital Input), DO (Digital Output), DIO (Digital Input/Output), AI (Analog Input), AO (Analog Output), AIO (Analog Input/Output)

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PIN Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	No.		
NC	8	-	No Connect. Keep the pins float.
nCE	9	DI	Active low Charge Enable pin. Battery charging is enabled when EN_CHG = 1 and pin = Low. pin must be pulled High or Low.
NC	10	-	No Connect. Keep the pins float.
TS	11	AI	Temperature qualification voltage input. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS to GND. Charge suspends when either TS pin is out of range. Recommend 103AT-2 thermistor.
nQON	12	DI	BATFET enable/reset control input. If the charger is in ship mode, a logic low on this pin with t_{SM_EXIT} duration forces the device to exit ship mode. If the charger is not in ship mode, a logic low on this pin with t_{QON_RST} initiates a full system power reset if either $V_{VBUS} < V_{VBUS_UVLO}$ or BATFET_CTRL_WVBUS = 1. nQON has no effect during shutdown mode. The pin contains an internal pull-up to maintain default high logic.
BAT	13	P	Battery connection point to the positive terminal of the battery pack. The internal BATFET is connected between BAT and SYS. Connect a 10uF closely to the BAT pin.
	14		
SYS	15	P	System connection point. The internal BATFET is connected between BAT and SYS. When the battery falls below the minimum system voltage, switch-mode converter keeps SYS above the minimum system voltage. Connect a 20uF closely to the SYS pin.
	16		
PGND	17	P	Power ground connection for high-current power converter node. Internally, PGND is connected to the source of the n-channel LSFET. On PCB layout, connect directly to ground connection of input and output capacitors of the charger. A single point connection is recommended between power PGND and the analog GND near the IC PGND pin.
	18		
SW	19	P	Switching node connecting to output inductor. Internally SW is connected to the source of the n-channel HSFET and the drain of the n-channel LSFET. Connect the 0.047μF bootstrap capacitor from SW to BTST.
	20		
BTST	21	P	PWM high side driver positive supply. Internally, the BTST is connected to the anode of the boost-strap diode. Connect the 0.047 μF bootstrap capacitor from SW to BTST.
REGN	22	P	PWM low side driver positive supply output. Internally, REGN is connected to the cathode of the boost-strap diode. Connect a 4.7 μF (10 V rating) ceramic capacitor from REGN to analog GND. The capacitor should be placed close to the IC. REGN also serves as bias rail of TS pin.
PMID	23	DO	Connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Given the total input capacitance, put 1μF on VBUS to PGND, and the rest capacitance on PMID to PGND.
NC	24	-	No Connect. Keep the pins float.
Thermal Pad	—	P	Exposed pad beneath the IC for heat dissipation. Always solder Thermal PAD Pad to the board, and have vias on the Thermal PAD plane star-connecting to PGND and ground plane for high-current power converter.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	VALUE
Voltage range (with respect to GND)	VBUS (converter not switching)	-2	23	V
	PMID (converter not switching)	-0.3	23	V
	BTST	-0.3	29	V
	SW	-2(50ns)	23	V
	BAT,SYS (converter not switching)	-0.3	6	V
	SDA,SCL,nINT,REGN,nCE	-0.3	6	V
	D+,D-	-0.3	6	V
	BTST to SW	-0.3	6	V
	PGND to GND	-0.3	0.3	V
Output sink current	nINT		6	mA
	STAT		6	mA
Junction temperature		-40	150	℃
Storage temperature range, Tstg		-55	150	℃

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	3.9		13(1)	V
I_{IN}	Input current (VBUS)			3	A
I_{SW}	Output current (SW)			3	A
V_{BAT}	Battery voltage			4.8	V
I_{BAT}	Fast charging current			3	A
	Discharging current with internal MOSFET			Up to 6 (continues)	A
				10 (peak) (Up to 1 sec duration)	A
T_A	Operating free-air temperature range	-40		85	℃

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either the BTST or SW pins. A tight layout minimizes switching noise.

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6.4 Thermal Information

THERMAL METRIC(1)		CX25601N RYK(QFN) 24-PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.3	℃/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.1	℃/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

$V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to +125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
I_{BAT}	Battery discharge current (BAT, SW, SYS) in buck mode	V_{BAT} = 4 V, $V_{BUS} < V_{BUS_UVLOZ}$, leakage between BAT and VBUS, T_J< 85°C			5	μA
I_{BAT}	Battery discharge current (BAT) in buck mode	V_{BAT} = 4 V, No VBUS, I²C Disabled, BATFET Disabled. T_J < 85°C		1		μA
I_{BAT}	Battery discharge current (BAT, SW, SYS)	V_{BAT} = 4 V, No VBUS, I²C Enabled, BATFET Enabled. T_J < 85°C		9		μA
I_{VBUS_HIZ}	Input supply current (VBUS) in buck mode	V_{VBUS} = 5 V, V_{BAT}= 4 V, High-Z Mode		14		μA
I_{VBUS_HIZ}	Input supply current (VBUS) in buck mode	V_{VBUS} = 9 V, VBAT= 4 V, High-Z Mode		20		μA
I_{VBUS}	Input supply current (VBUS) in buck mode	V_{VBUS} = 5 V, V_{VBAT} = 4 V, converter switching ISYS = 0 A, PFM enabled		1.2		mA
I_{BOOST}	Battery Discharge Current in boost mode	V_{BAT} = 4.2 V, boost mode, I_{VBUS} = 0 A, converter switching, TS float, TS_IGNORE = 1		1		mA
VBUS AND BAT PIN POWER-UP						
V_{VBUS_OP}	VBUS operating range	V_{VBUS} rising	3.9		13	V
V_{VBUS_OVP}	VBUS overvoltage rising threshold	VBUS rising, VBUS_OVP = 0	6.1	6.4	6.7	V
V_{VBUS_OVPZ}	VBUS overvoltage falling threshold	VBUS rising, VBUS_OVP = 0	5.6	5.9	6.2	V
V_{VBUS_OVP}	VBUS overvoltage rising threshold	VBUS rising, VBUS_OVP = 1	12.7	13	13.3	V
V_{VBUS_OVPZ}	VBUS overvoltage falling threshold	VBUS falling, VBUS_OVP = 1	12.2	12.5	12.8	V
V_{VBUS_UVLOZ}	VBUS for active I²C, no battery	V_{VBUS} rising	3.2	3.35	3.5	V
$V_{VBUS_UVLOZ_HYS}$	I²C active hysteresis	V_{VBUS} falling from above V_{VBUS_UVLOZ}		200		mV

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Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP} , T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{POORSRC}$	Bad adapter detection threshold	VBUS falling	3.6	3.7	3.75	V
$I_{POORSRC}$	Bad adapter detection current source			10		mA
V_{SLEEP}	Sleep mode falling threshold	(V_{VBUS} – V_{VBAT}), V_{BUSMIN_FALL} ≤ V_{BAT} ≤ V_{REG}, VBUS falling	9	45	85	mV
V_{SLEEPZ}	Sleep mode rising threshold	(V_{VBUS} – V_{VBAT}), V_{BUSMIN_FALL} ≤ V_{BAT} ≤ V_{REG}, VBUS rising	115	220	340	mV
V_{BAT_UVLOZ}	BAT for active I^2C, no adapter	V_{BAT} rising	2.3	2.4	2.5	V
V_{BAT_UVLO}	BAT for turn off I^2C, no adapter	V_{BAT} falling, VBAT_UVLO = 0	2.1	2.2	2.3	V
		V_{BAT} falling, VBAT_UVLO = 1	1.7	1.8	1.9	V
$V_{VBUSMIN_FALL}$	Bad adapter detection falling threshold	V_{BUS} falling	3.6	3.7	3.75	V
I_{BADSRC}	Bad adapter detection current source	Sink current from VBUS to GND		10		mA
POWER-PATH						
$V_{SYS_REG_ACC}$	Typical system voltage regulation	ISYS = 0A, VBAT > VSYSMIN, Charge Disabled. Offset above VBAT		50		mV
		ISYS = 0A, VBAT < VSYSMIN, Charge Disabled. Offset above VSYSMIN		230		mV
V_{SYSMIN_REG}	VSYSMIN register range		2.56		3.84	V
$V_{SYSMIN_REG_STEP}$	VSYSMIN register step size			80		mV
$V_{SYSMIN_REG_ACC}$	System regulation voltage	I_{SYS} = 0 A, V_{BAT} < VSYSMIN = B00h (3.52V), Charge Disabled	3.52	3.75		V
$R_{ON(RBFET)}$	Top reverse blocking MOSFET on-resistance between VBUS and PMID - Q1	-40°C≤ T_A ≤ 125°C		30		mΩ
$R_{ON(HSFET)}$	Top switching MOSFET on-resistance between PMID and SW-Q2	V_{REGN} = 5 V , -40°C≤ T_A ≤ 125°C		80		mΩ
$R_{ON(LSFET)}$	Bottom switching MOSFET on-resistance between SW and GND - Q3	V_{REGN} = 5 V , -40°C≤ T_A ≤ 125°C		80		mΩ

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Electrical Characteristics (continued)

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{ON(BAT-SYS)}$	SYS-BAT MOSFET on-resistance	QFN package, Measured from BAT to SYS, V_{BAT} = 4.2V, T_J = 25°C		20		mΩ
BATTERY CHARGER						
V_{REG_RANGE}	Charge voltage program range		3.84		4.8	V
V_{REG_STEP}	Charge voltage step			10		mV
V_{REG_ACC}	Charge voltage setting accuracy	T_J = 25°C	–0.5		0.5	%
$I_{CHG_REG_RANGE}$	Charge current regulation range		0.08		3.04	A
$I_{CHG_REG_STEP}$	Charge current regulation step			80		mA
$I_{CHG_REG_ACC}$	Charge current regulation	I_{CHG} =1040 mA, VBUS=5V, V_{BAT} = 3.8 V	-5.5		5.5	%
	Charge current regulation	I_{CHG} = 1760 mA, VBUS=5V, V_{BAT} = 3.8 V	-5.5		5.5	%
$V_{BATLOWV_FALL}$	Battery LOWV falling threshold	Transition from fast charge to pre-charge	2.7	2.8	2.9	V
$V_{BATLOWV_RISE}$	Battery LOWV rising threshold	Transition from pre-charge to fast charge	2.9	3.0	3.1	V
I_{PRECHG_RANGE}	Precharge current range		100		620	mA
I_{PRECHG_STEP}	Typical precharge current step			20		mA
I_{PRECHG_ACC}	Precharge current accuracy	VBAT = 2.5V, IPRECHG = 200mA, T_J = –10°C - 85°C	-20		20	%
I_{TERM_RANGE}	Typical termination current range		100		620	mA
I_{TERM_STEP}	Typical termination current step			10		mA
I_{TERM_ACC}	Termination current regulation accuracy	ITERM = 300mA, T_J=-10℃ - 85℃	-20		20	%
V_{BAT_SHORTZ}	Battery short voltage	V_{VBAT} rising		2.25		V
V_{BAT_SHORT}	Battery short voltage	V_{VBAT} falling, VBAT_UVLO=0		2.05		V
		V_{VBAT} falling, VBAT_UVLO=1		1.85		V
I_{BAT_SHORT}	Battery short current	V_{VBAT} < V_{BAT_SHORTZ}, ITRICKLE = 0		17		mA
		V_{VBAT} < V_{BAT_SHORTZ}, ITRICKLE = 1		65		mA
V_{RECHG}	Recharge Threshold below V_{REG}	V_{BAT} falling		200		mV
I_{BAT_LOAD}	Battery discharge load current			15		mA
I_{SYS_LOAD}	System discharge load current			15		mA

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Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = –40°C to +125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE AND CURRENT REGULATION						
V_{INDPM_RANGE}	Typical input voltage regulation range		3.8		13.2	V
V_{INDPM_STEP}	Typical input voltage regulation step			40		mV
V_{INDPM_ACC}	Input voltage regulation accuracy	VINDPM = 4.6 V	–4		4	%
		VINDPM = 8 V	–3		3	%
$V_{INDPM_VBAT_ACC}$	Input voltage regulation accuracy tracking VBAT	VBAT = 3.9V, VINDPM_BAT_TRACK=1, VINDPM = 4V	4.15	4.3	4.45	V
I_{INDPM_RANGE}	Typical input current regulation range		0.1		3.0	A
I_{INDPM_STEP}	Typical input current regulation step			20		mA
I_{INDPM}	USB input current regulation limit	V_{VBUS} = 5 V, current pulled from SW, I_{INDPM} = 500 mA, –40 ≤ T_J ≤ 85°C	400	450	500	mA
		V_{VBUS} = 5 V, current pulled from SW, I_{INDPM} = 900 mA, –40 ≤ T_J ≤ 85°C	750	825	900	mA
		V_{VBUS} = 5 V, current pulled from SW, I_{INDPM} = 1.5 A, –40 ≤ T_J ≤ 85°C	1.35	1.425	1.5	A
BAT OVER-VOLTAGE/CURRENT PROTECTION						
V_{BATOVP_RISE}	Battery overvoltage threshold	V_{BAT} rising, as percentage of V_{REG}		104		%
V_{BATOVP_FALL}	Battery overvoltage threshold	V_{BAT} falling, as percentage of V_{REG}		102		%
I_{BATFET_OCP}	BATFET over-current rising threshold		6			A
I_{BAT_PK}	Battery discharging peak current rising threshold	IBAT_PK = 10	6			A
		IBAT_PK = 11	13			A
THERMAL REGULATION AND THERMAL SHUTDOWN						
$T_{JUNCTION_REG}$	Junction Temperature Regulation Threshold	TREG = 1		120		°C
$T_{JUNCTION_REG}$	Junction Temperature Regulation Threshold	TREG = 0		60		°C
T_{SHUT}	Thermal Shutdown Rising Temperature	Temperature Increasing		140		°C
T_{SHUT_HYST}	Thermal Shutdown Hysteresis	Temperature Decreasing by T_{SHUT_HYS}		30		°C

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Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = –40°C to +125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMISTOR COMPARATORS (CHARGE MODE)						
V_{TS_COLD}	TS pin rising voltage threshold for TH1 comparator to transition from TS_COOL to TS_COLD. Charge suspended above this voltage.	As Percentage to TS pin bias reference (-5°C w/ 103AT), TS_TH1_TH2_TH3= 100, 101, 110	75	75.5	76	%
		As Percentage to TS pin bias reference (0°C w/ 103AT), TS_TH1_TH2_TH3 = 000, 001, 010, 011, 111	72.8	73.3	73.8	%
V_{TS_COLDZ}	TS pin falling voltage threshold for TH1 comparator to transition from TS_COLD to TS_COOL. TS_COOL charge settings resume below this voltage.	As Percentage to TS pin bias reference (-2.5°C w/ 103AT), TS_TH1_TH2_TH3 = 100, 101, 110	73.9	74.4	74.9	%
		As Percentage to TS pin bias reference (2.5°C w/ 103AT), TS_TH1_TH2_TH3 = 000, 001, 010, 011, 111	71.7	72.2	72.7	%
V_{TS_COOL}	TS pin rising voltage threshold for TH2 comparator to transition from TS_PRECOOL to TS_COOL. TS_COOL charging settings used above this voltage.	As Percentage to TS pin bias reference (5°C w/ 103AT), TS_TH1_TH2_TH3 = 000, 100	70.6	71.1	71.6	%
		As Percentage to TS pin bias reference (10°C w/ 103AT), TS_TH1_TH2_TH3 = 001, 101, 110, 111	67.9	68.4	68.9	%
		As Percentage to TS pin bias reference (15°C w/ 103AT), TS_TH1_TH2_TH3 = 010	65	65.5	66	%
		As Percentage to TS pin bias reference (20°C w/ 103AT), TS_TH1_TH2_TH3 = 011	61.9	62.4	62.9	%
V_{TS_COOLZ}	TS pin falling voltage threshold for TH2 comparator to transition from TS_COOL to TS_PRECOOL. TS_PRECOOL charging settings resume below this voltage.	As Percentage to TS pin bias reference (7.5°C w/ 103AT), TS_TH1_TH2_TH3 = 000, 100	69.3	69.8	70.3	%
		As Percentage to TS pin bias reference (12.5°C w/ 103AT), TS_TH1_TH2_TH3 = 001, 101, 110, 111	66.6	67.1	67.6	%
		As Percentage to TS pin bias reference (17.5°C w/ 103AT), TS_TH1_TH2_TH3 = 010	63.7	64.2	64.7	%
		As Percentage to TS pin bias reference (22.5°C w/ 103AT), TS_TH1_TH2_TH3 = 011	60.6	61.1	61.6	%

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Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = –40°C to +125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{TS_PRECOOL}$	TS pin rising voltage threshold for TH3 comparator to transition from TS_NORMAL to TS_PRECOOL. TS_PRECOOL charge settings used above this voltage.	As Percentage to TS pin bias reference (15°C w/ 103AT), TS_TH1_TH2_TH3 = 000, 001, 100, 101	65	65.5	66	%
		As Percentage to TS pin bias reference (20°C w/ 103AT), TS_TH1_TH2_TH3 = 010, 011, 110, 111	61.9	62.4	62.9	%
$V_{TS_PRECOOLZ}$	TS pin falling voltage threshold for TH3 comparator to transition from TS_PRECOOL to TS_NORMAL. Normal charging resumes below this voltage.	As Percentage to TS pin bias reference (17.5°C w/ 103AT), TS_TH1_TH2_TH3 = 000, 001, 100, 101	63.7	64.2	64.7	%
		As Percentage to TS pin bias reference (22.5°C w/ 103AT), TS_TH1_TH2_TH3 = 010, 011, 110, 111	60.6	61.1	61.6	%
$V_{TS_PREWARM}$	TS pin falling voltage threshold for TH4 comparator to transition from TS_NORMAL to TS_PREWARM. TS_PREWARM charging settings used below this voltage.	As Percentage to TS pin bias reference (35°C w/ 103AT), TS_TH4_TH5_TH6 = 000, 001, 010, 100, 101	51.5	52	52.5	%
		As Percentage to TS pin bias reference (40°C w/ 103AT), TS_TH4_TH5_TH6 = 011, 110, 111	47.9	48.4	48.9	%
$V_{TS_PREWARMZ}$	TS pin rising voltage threshold for TH4 comparator to transition from TS_PREWARM to TS_NORMAL. Normal charging resumes above this voltage.	As Percentage to TS pin bias reference (32.5°C w/ 103AT), TS_TH4_TH5_TH6 = 000, 001, 010, 100, 101	53.3	53.8	54.3	%
		As Percentage to TS pin bias reference (37.5°C w/ 103AT), TS_TH4_TH5_TH6 = 011, 110, 111	49.2	49.7	50.2	%
V_{TS_WARM}	TS pin falling voltage threshold for TH5 comparator to transition from TS_PREWARM to TS_WARM. TS_WARM charging settings used below this voltage.	As Percentage to TS pin bias reference (40°C w/ 103AT), TS_TH4_TH5_TH6 = 000, 100	47.9	48.4	48.9	%
		As Percentage to TS pin bias reference (45°C w/ 103AT), TS_TH4_TH5_TH6 = 001, 101, 110	44.3	44.8	45.3	%
		As Percentage to TS pin bias reference (50°C w/ 103AT), TS_TH4_TH5_TH6 = 010, 111	40.7	41.2	41.7	%
		As Percentage to TS pin bias reference (55°C w/ 103AT), TS_TH4_TH5_TH6 = 011	37.2	37.7	38.2	%

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Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = –40°C to +125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{TS_WARMZ}	TS pin rising voltage threshold for TH5 comparator to transition from TS_WARM to TS_PREWARM. TS_PREWARM charging settings resume above this voltage.	As Percentage to TS pin bias reference (37.5°C w/ 103AT), TS_TH4_TH5_TH6 = 000, 100	49.2	49.7	50.2	%
		As Percentage to TS pin bias reference (42.5°C w/ 103AT), TS_TH4_TH5_TH6 = 001, 101, 110	45.6	46.1	46.6	%
		As Percentage to TS pin bias reference (47.5°C w/ 103AT), TS_TH4_TH5_TH6 = 010, 111	42	42.5	43	%
		As Percentage to TS pin bias reference (52.5°C w/ 103AT), TS_TH4_TH5_TH6 = 011	38.5	39	39.5	%
V_{TS_HOT}	TS pin falling voltage threshold for TH6 comparator to transition from TS_WARM to TS_HOT. Charging is suspended below this voltage.	As Percentage to TS pin bias reference (50°C w/ 103AT), TS_TH4_TH5_TH6 = 100 or 101	40.7	41.2	41.7	%
		As Percentage to TS pin bias reference (60°C w/ 103AT), TS_TH4_TH5_TH6 = 000, 001, 010, 011, 110 or 111	33.9	34.4	34.9	%
V_{TS_HOTZ}	TS pin rising voltage threshold for TH6 comparator to transition from TS_HOT to TS_WARM. TS_WARM charging settings resume above this voltage.	As Percentage to TS pin bias reference (47.5°C w/ 103AT), TS_TH4_TH5_TH6 = 100 or 101	42	42.5	43	%
		As Percentage to TS pin bias reference (57.5°C w/ 103AT), TS_TH4_TH5_TH6 = 000, 001, 010, 011, 110 or 111	35.2	35.7	36.2	%
THERMISTOR COMPARATORS (OTG MODE)						
$V_{TS_OTG_COLD}$	TS pin rising voltage threshold to transition from TS_OTG_NORMAL to TS_OTG_COLD. OTG suspended above this voltage.	As Percentage to TS pin bias reference (–20°C w/ 103AT), TS_TH_OTG_COLD = 0	79.5	80	80.5	%
		As Percentage to TS pin bias reference (–10°C w/ 103AT), TS_TH_OTG_COLD = 1	76.6	77.1	77.6	%
$V_{TS_OTG_COLDZ}$	TS pin falling voltage threshold to transition from TS_OTG_COLD to TS_OTG_NORMAL. OTG resumes below this voltage.	As Percentage to TS pin bias reference (–15°C w/ 103AT), TS_TH_OTG_COLD = 0	78.2	78.7	79.2	%
		As Percentage to TS pin bias reference (–5°C w/ 103AT), TS_TH_OTG_COLD = 1	75	75.5	76.5	%

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Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = –40°C to +125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{TS_OTG_HOT}$	TS pin falling voltage threshold to transition from TS_OTG_NORMAL to TS_OTG_HOT. OTG suspended below this voltage.	As Percentage to TS pin bias reference (55°C w/ 103AT), TS_OTG_HOT = 00	37.2	37.7	38.2	%
		As Percentage to TS pin bias reference (60°C w/ 103AT), TS_OTG_HOT = 01	33.9	34.4	34.9	%
		As Percentage to TS pin bias reference (65°C w/ 103AT), TS_OTG_HOT = 10	30.8	31.3	31.8	%
$V_{TS_OTG_HOTZ}$	TS pin rising voltage threshold to transition from TS_OTG_HOT to TS_OTG_NORMAL. OTG resumes above this threshold.	As Percentage to TS pin bias reference (52.5°C w/ 103AT), TS_OTG_HOT = 00	38.5	39	39.5	%
		As Percentage to TS pin bias reference (57.5°C w/ 103AT), TS_OTG_HOT = 01	35.2	35.7	36.2	%
		As Percentage to TS pin bias reference (62.5°C w/ 103AT), TS_OTG_HOT = 10	32	32.5	33	%
PWM						
f_{SW}	PWM switching frequency	Oscillator frequency, buck mode		1100		kHz
D_{MAX}	Maximum PWM duty cycle			97		%
BOOST MODE OPERATION						
V_{OTG_RANGE}	Typical OTG mode voltage regulation range		3.8		5.28	V
V_{OTG_STEP}	Typical OTG mode voltage regulation step			80		mV
V_{OTG_ACC}	OTG mode voltage regulation accuracy	IVBUS = 0A, VOTG = 5V	-3		3	%
V_{BAT_OTG}	BAT voltage rising threshold to enable OTG mode	V_{VBAT} rising, VBAT_OTG_MIN = 0	2.9	3	3.4	V
V_{BAT_OTGZ}	BAT voltage falling threshold to disable OTG mode	V_{VBAT} falling, VBAT_OTG_MIN = 0	2.7	2.8	2.9	V
V_{BAT_OTG}	BAT voltage rising threshold to enable OTG mode	VBAT rising, VBAT_OTG_MIN = 1	2.5	2.6	2.7	V
V_{BAT_OTGZ}	BAT voltage falling threshold to disable OTG mode	VBAT falling, VBAT_OTG_MIN = 1	2.3	2.4	2.5	V
I_{OTG_RANGE}	OTG mode current regulation range		0.1		1.2	A
I_{OTG_STEP}	OTG mode current regulation step			20		mA

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Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = –40°C to +125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OTG_OVP}	OTG overvoltage threshold	Rising threshold		VOTG* 1.09		V
REGN LDO						
V_{REGN}	REGN LDO output voltage	V_{VBUS} = 9V, I_{REGN} = 20mA	4.8	5.0	5.2	V
		V_{VBUS} = 5V, I_{REGN} = 20mA	4.4	4.6		V
LOGIC I/O PIN CHARACTERISTICS (nCE, STAT, nINT)						
V_{ILO}	Input low threshold				0.4	V
V_{IH}	Input high threshold		1.3			V
I_{BIAS}	High-level leakage current	Pull up rail 1.8 V			1	μA
V_{OL}	Low-level output voltage				0.4	V
I2C Interface (SCL, SDA)						
V_{IH}	Input high threshold level	Pull up rail 1.8 V		673		mV
V_{IL}	Input low threshold level	Pull up rail 1.8 V		553		mV
V_{OL}	Output low threshold level	Sink current = 5 mA			0.4	V

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6.6 Timing Requirement

			MIN	TYP	MAX	UNIT
VBUS/BAT POWER UP						
t_{BADSRC}	Bad adapter detection duration			30		ms
BATTERY CHARGER						
t_{SAFETY_TRKCHG}	Charge safety timer accuracy in trickle charge		0.85	1	1.1	hr
t_{SAFETY_PRECHG}	Charge safety timer accuracy in pre-charge	PRECHG_TMR = 0	1.75	2	2.2	hr
t_{BATOVP}	Battery over-voltage deglitch time to disable charge			10		μs
t_{SAFETY}	Typical Charge Safety Timer Range	CHG_TMR = 0	10.5	12	12.5	hr
BATFET_CONTROL						
t_{BATFET_DLY}	Time after writing to BATFET_CTRL before BATFET turned off for shutdown	BATFET_DLY = 0		24		ms
t_{SM_EXIT}	Deglitch time for nQON to be pulled low in order to exit from Ship Mode		1.69	2	2.31	s
t_{QON_RST}	Time nQON is held low to initiate system power reset		9	10.5	11.5	s
t_{BATFET_RST}	Duration that BATFET is disabled during system power reset			524		ms
DIGITAL CLOCK AND WATCHDOG TIMER						
t_{WDT}	Watchdog Reset time (EN_HIZ = 0, WATCHDOG = 200s)			200		s
f_{SCL}	SCL clock frequency				1	MHz

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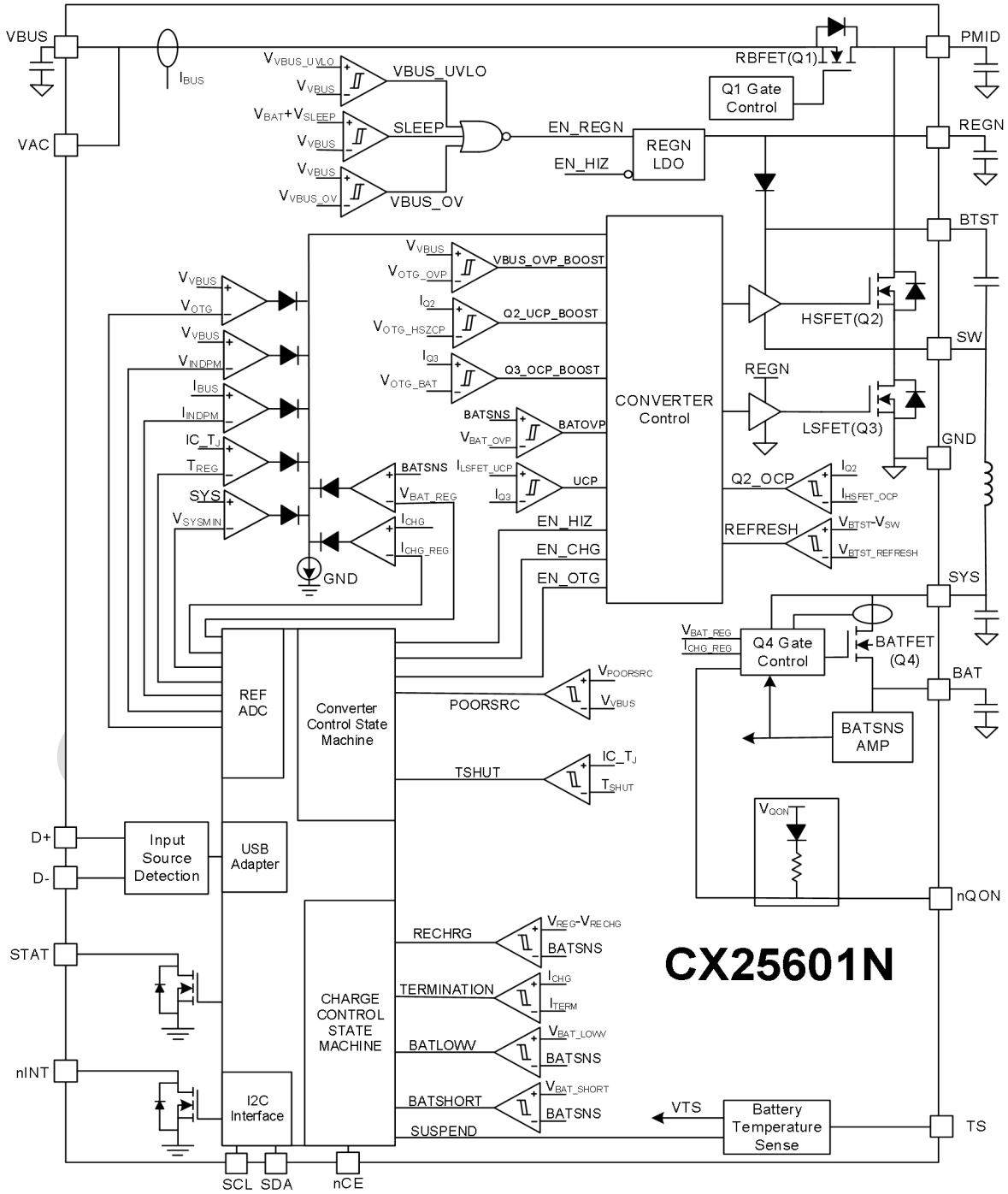
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7 Detailed Description

7.1 Overview

The CX25601N is highly-integrated 3-A switch-mode battery charger for single-cell Li-ion and Li-polymer batteries. The device includes input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), battery FET (BATFET, Q4), and bootstrap diode for the high-side gate driver.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Power-On-Reset (POR)

The CX25601N power internal bias circuits from the higher voltage of VBUS and BAT. When either voltage rises above its undervoltage lockout (UVLO) threshold, all registers are reset to their POR values and the I²C interface is enabled for communication. A non-maskable nINT pulse is generated, after which the host can access all of the registers.

7.3.2 Device Power Up from Battery without Input Source

If only the battery is present and the VBAT is above depletion threshold (V_{BAT_UVLOZ}), the CX25601N performs a power-on reset then turns on the BATFET to connect the battery to system. The REGN LDO output remains off to minimize the quiescent current. The low RDSON of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time.

7.3.3 Power Up from Input Source

When a valid input source is plugged in with VBAT < V_{BAT_UVLOZ}, the CX25601N performs a power-on reset then checks the input source voltage to turn on the REGN LDO and all the bias circuits. It detects and sets the input current limit before the buck converter is started. The power up sequence from input source is as listed:

1. REGN LDO power up
2. Poor source qualification
3. Input source type detection using D+/D– to set input current limit (IINDPM) register and input source type
4. Input voltage limit threshold setting
5. Converter power-up

7.3.3.1 Power Up REGN Regulation

The REGN LDO regulator supplies internal bias circuits as well as the HSFET and LSFET gate drive. The REGN LDO also provides bias rail to TS external resistors. The pull-up rail of STAT can be connected to REGN as well. The REGN is enabled when all the below conditions are valid.

- VBUS above V_{VBUS_UVLOZ}
- VBUS above V_{BAT} + V_{SLEEPZ}
- EN_HIZ = 0
- After 220-ms delay is completed

If any one of the above conditions is not valid, the REGN LDO and the converter power stage remain off with the converter disabled. In this state, the battery supplies power to the system.

7.3.3.2 Poor Source Qualification

After REGN LDO powers up, the device checks the current capability of the input source. The input source has to meet the following requirements in order to move forward to the next power on steps.

- VBUS voltage below V_{VBUS_OVP}
- VBUS voltage above $V_{POORSRC}$ when pulling $I_{POORSRC}$

Once these conditions are met, the device proceeds to input source type detection.

7.3.3.3 D+/D– Detection Sets Input Current Limit

After the REGN LDO is powered, the adapter has been qualified as a good source, and AUTO_INDET_EN bit = 1 (POR default), CX25601N runs input source detection through D+/D– lines to detect USB Battery Charging Specification 1.2 (BC1.2) input sources (CDP / SDP / DCP) and non-standard adapters. If DCP is

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detected, CX25601N runs HVDCP detection if EN_9V is 1. The detection algorithm runs automatically each time that VBUS is plugged in, updating the IINDPM according to Table 7-2. If AUTO_INDET_EN = 0, the detection algorithm is not run and IINDPM remains unchanged. The host can force the detection algorithm to run and update IINDPM by setting FORCE_INDET to 1.

The USB BC1.2 is able to identify Standard Downstream Port (SDP), Charging Downstream Port (CDP), and Dedicated Charging Port (DCP). When the Data Contact Detection (DCD) timer of 500ms is expired, the non-standard adapter detection is applied to set the input current limit.

The secondary detection is used to distinguish two types of charging ports (CDP and DCP). Most of the time, a CDP requires the portable device (such as smart phone, tablet) to send back an enumeration within 2.5 seconds of CDP plug-in. Otherwise, the port reverts back to SDP even though the D+/D– detection indicates CDP.

Upon the completion of input source type detection, the following registers are changed:

1. Input Current Limit (IINDPM) register is changed to set current limit
2. VBUS_STAT bits are updated to indicate the detected input source type

After detection completes, the host can over-write the IINDPM register to change the input current limit if needed.

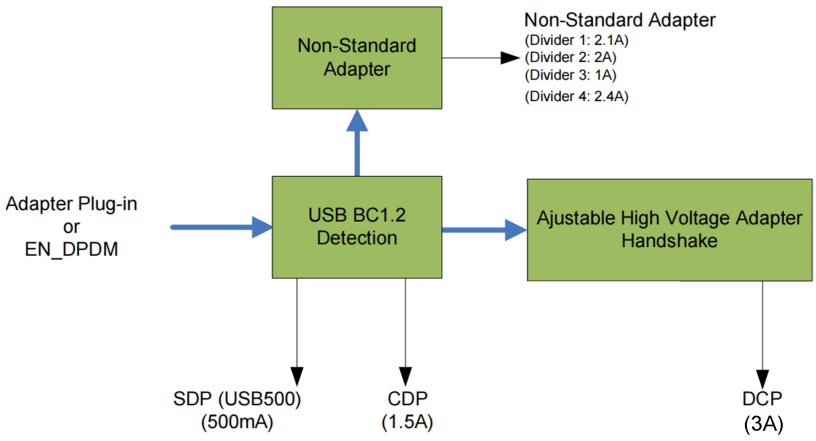


Figure 7-1. D+/D– Detection Flow

If DCP is detected (VBUS_STAT = 011), CX25601N turns on $V_{D+D-_0p6V_SRC}$ on D+ if EN_DCP_BIAS is set to 1. Setting EN_DCP_BIAS to 0 while VBUS_STAT = 011 disables the $V_{D+D-_0p6V_SRC}$ on D+ pin, and setting EN_DCP_BIAS to 1 while VBUS_STAT = 011 enables the $V_{D+D-_0p6V_SRC}$ on D+ pin. The EN_HIZ bit has priority over EN_DCP_BIAS.

High Voltage Dedicated Charging Port (HVDCP) is used to negotiate 9V from the power source if BC1.2 DCP support is detected.

In order to remain in 9V HVDCP, CX25601N must maintain a bias on D+ and D-, resulting in higher quiescent current. The host may remove this bias and associated quiescent current by setting EN_9V to 0 at any time. Setting EN_9V to 0 when an HVDCP adapter is providing 9V causes the adapter to revert to 5V DCP operation.

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The non-standard detection is used to distinguish vendor specific adapters based on their unique dividers on the D+/D- pins. Comparators detect the voltage applied on each pin and determine the input current limit according to Table 7-1.

Table 7-1. Non-Standard Adapter Detection

Non-Standard Adapter	Input Current Limit (A)
Divider 1	1
Divider 2	2.1
Divider 3	2.4

Table 7-2. Input Current Limit Setting from D+/D– Detection

D+/D– DETECTION	INPUT CURRENT LIMIT (IINLIM)	VBUS_STAT
USB SDP (USB500)	500 mA	0x1
USB CDP	1.5 A	0x2
USB DCP	1.5 A	0x3
Divider 1	1A	0x5
Divider 2	2.1 A	0x5
Divider 3	2.4 A	0x5
HVDCP	1.5 A	0x6
Unknown 5-V Adapter	500mA	0x4

7.3.3.4 Input Voltage Limit Threshold Setting (VINDPM Threshold)

The CX25601N supports a wide range of input voltage limit (3.8 V – 13.2 V). Its POR default VINDPM threshold is set at 4.6 V. The device also supports dynamic VINDPM tracking, which tracks the battery voltage to ensure a sufficient margin between input and battery voltages for proper operation of the buck converter. This function is enabled via the VINDPM_BAT_TRACK register bit. When enabled, the actual input voltage limit is the higher of the VINDPM register or $V_{INDPM_BAT_TRACK}$ (VBAT + 400-mV typical offset.)

7.3.3.5 Converter Power-Up

After the input current and voltage limits are set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, the BATFET turns off. Otherwise, the BATFET stays on to charge the battery. Converter startup requires the following conditions:

- VBUS has passed poor source qualification
- VBUS > V_{BAT} + V_{SLEEPZ}
- V_{VBUS} < V_{VBUS_OVP}
- EN_HIZ = 0
- V_{SYS} < V_{SYS_OVP}
- T_J < T_{SHUT}

The CX25601N provides soft start when the system rail is ramped up by setting IINDPM to its lowest programmable value and stepping up through each available setting until reaching the value set by IINDPM register. Concurrently, the system short protection limits the output current to approximately 0.5 A when the system rail is below V_{SYS_SHORT}.

The device uses a highly efficient 1.1-MHz, fixed frequency pulse width modulated (PWM) step-down

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switching regulator. The internally compensated feedback loop keep tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

The device switches to pulse frequency modulation (PFM) control at light load condition. The PFM_FWD_DIS and PFM_OTG_DIS bits can be used to disable the PFM operation in buck and boost respectively.

7.3.4 Boost Mode Operation From Battery

CX25601N supports boost converter operation to deliver power from the battery to VBUS. The output voltage and maximum current are set in the VOTG and IOTG registers, respectively. VBUS_STAT is set to 111 upon a successful entry into boost OTG. The boost operation is enabled when the following conditions are met:

1. BAT above V_{BAT_OTG}
2. VBUS less than V_{BAT} +V_{SLEEP}
3. Boost mode operation is enabled (EN_OTG = 1)
4. $V_{TS_OTG_HOT} < V_{TS} < V_{TS_OTG_COLD}$
5. $V_{REGN} > V_{REGN_OK}$
6. 30 ms delay after EN_OTG = 1
7. Boost mode regulation voltage in REG0x0C is greater than 105% of battery voltage.

7.3.5 Host Mode and Standalone Power Management

7.3.5.1 Host Mode and Default Mode

The device is a host controlled charger, but it can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode. When the charger is in default mode, WD_STAT bit becomes HIGH, WD_FLAG is set to 1, and an nINT is asserted low to alert the host (unless masked by WD_MASK). The WD_FLAG bit would read as 1 upon the first read and then 0 upon subsequent reads. When the charger is in host mode, WD_STAT bit is LOW.

After power-on-reset, the device starts in default mode with watchdog timer expired. All the registers are in the default settings.

In default mode, the device keeps charging the battery with default 1-hour trickle charging safety timer, 2-hour pre-charging safety timer and the 12-hour fast charging safety timer. At the end of the 1-hour or 2-hour or 12-hour timer expired, the charging is stopped and the buck converter continues to operate to supply system load.

A write to any I^2C register transitions the charger from default mode to host mode, and initiates the watchdog timer. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires (WD_STAT bit is set), or disable watchdog timer by setting WATCHDOG bits = 00.

When the watchdog expires, the device returns to default mode. The ICHG value is divided in half when the watchdog timer expires, and a number of other fields are reset to their POR default values as shown in the notes column of the register tables. When watchdog timer expires, WD_STAT and WD_FLAG is set to 1, and an nINT is asserted low to alert the host (unless masked by WD_MASK).

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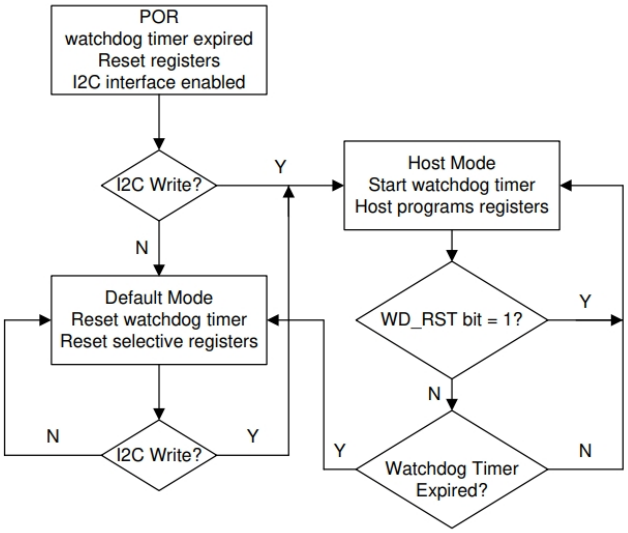


Figure 7-2. Watchdog Timer Flow Chart

7.3.5.2 Register Bit Reset

Beside a register reset by the watchdog timer in default mode, the register and the timer can be reset to the default value by writing the REG_RST bit to 1. The register bits, which can be reset by the REG_RST bit, are noted in the Register Map section. After the register reset, the REG_RST bit goes back from 1 to 0 automatically.

7.3.6 Power Path Management

The CX25601N accommodates a wide range of input sources from a USB, wall adapter, wireless charger, to car charger. They provide automatic power path selection to supply the system from an input source, battery, or both.

7.3.7 Battery Charging Management

The CX25601N charges a 1-cell Li-Ion battery with up to a 3-A charge current. The 20-mΩ BATFET improves charging efficiency and minimizes the voltage drop during discharging.

7.3.7.1 Autonomous Charging Cycle

When battery charging is enabled (EN_CHG bit = 1 and nCE pin is LOW), the CX25601N autonomously completes a charging cycle without host involvement. The device default charging parameters are listed in Table 7-3. The host can always control the charging operations and optimize the charging parameters by writing to the corresponding registers through I^2C.

Table 7-3. Charging Parameter Default Setting

	VREG	ITRICKLE	IPRECHG	ICHG	ITERM	TOPOFF TIMER
CX25601N	4.2 V	17 mA	100 mA	1040 mA	100 mA	Disabled

A new charge cycle starts when the following conditions are valid:

- Converter starts per the conditions in Section 7.3.3.5
- EN_CHG = 1
- nCE pin is low

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- No thermistor fault on TS
- No safety timer fault

The CX25601N automatically terminates the charging cycle when the charging current is below termination threshold, battery voltage is above recharge threshold, and device not is in DPM or thermal regulation. When a fully charged battery is discharged below VRECHG, the device automatically starts a new charging cycle. After charging terminates, toggling nCE pin or EN_CHG bit also initiates a new charging cycle.

The STAT output indicates the charging status. Refer to Section 7.4.5.1 for details of STAT pin operation. In addition, the status register (CHG_STAT) indicates the different charging phases: 00-charging disabled or terminated, 01-constant current, 10 constant voltage, 11-topoff charging.

7.3.7.2 Battery Charging Profile

The CX25601N charges the battery in five phases: trickle charge, pre-charge, constant current, constant voltage and an optional top-off charging phase. At the beginning of a charging cycle, the device checks the battery voltage and regulates current and voltage accordingly.

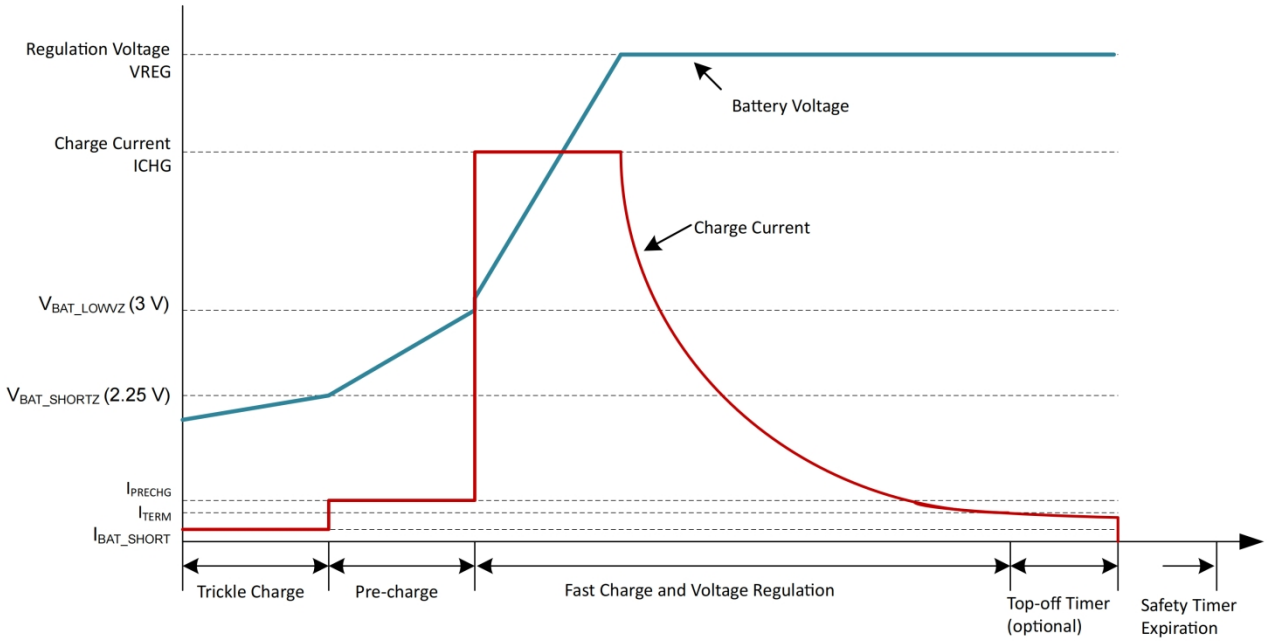


Figure 7-3. Battery Charging Profile

7.3.7.3 Charging Termination

The CX25601N terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below ITERM. To avoid early termination, the CX25601N do not terminate while IINDPM, VINDPM or thermal regulation loops are active. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system, and the BATFET can turn on again to engage supplement mode. Termination can be permanently disabled by writing 0 to EN_TERM bit prior to charge termination.

At low termination currents, due to the comparator offset, the actual termination current may be 10 mA to 20 mA higher than the termination target. In order to compensate for comparator offset, a programmable top-off timer can be applied after termination is detected. The top-off timer follows safety timer constraints, such that if the safety timers suspend, so does the top-off timer. Similarly, if the safety timers count at half-clock rate, so

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does the top-off timer.The host can read CHG_STAT to find out the termination status.

Top-off timer gets reset by any of the following conditions:

1. Charging cycle stop and restart (toggle nCE pin, toggle EN_CHG bit, charged battery falls below recharge threshold or adapter removed and replugged)
2. Termination status low to high
3. REG_RST register bit is set

The top-off timer settings are read in after is detected by the charger. Programming a top-off timer value after termination has no effect unless a recharge cycle is initiated. CHG_FLAG is set to 1 when entering top-off timer segment and again when the top-off timer expires.

7.3.7.4 Thermistor Qualification

The CX25601N provides a single thermistor input for battery temperature monitoring. The TS pin input of the battery temperature can be ignored by the charger if TS_IGNORE = 1. When the TS pin feedback is ignored, the charger considers the TS to always be valid for charging mode and OTG mode, and TS_STAT always reports 000. The TS pin may be left floating if TS_IGNORE is set to 1.

When TS_IGNORE = 0, the charger adjusts the charging profile based on the TS pin feedback information according to the configurable profile described in Section 7.3.7.5. When the battery temperature crosses from one temperature range to another, TS_STAT is updated accordingly, and the charger sets the FLAG bit for the newly-entered temperature range. If TS_MASK is set to 0, any change to TS_STAT, including a transition to TS_NORMAL, generates an nINT pulse.

7.3.7.5 Advanced Temperature Profile in Charge Mode

To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges. As battery technology continues to evolve, battery manufacturers have released temperature safety specifications that extend beyond the JEITA standard. The CX25601N features a highly flexible temperature-based charging profile to meet these advanced specifications while remaining backwards compatible with the original JEITA standard. Figure 7- 4 shows the programmability for charger behavior under different battery temperature (TS) operating regions.

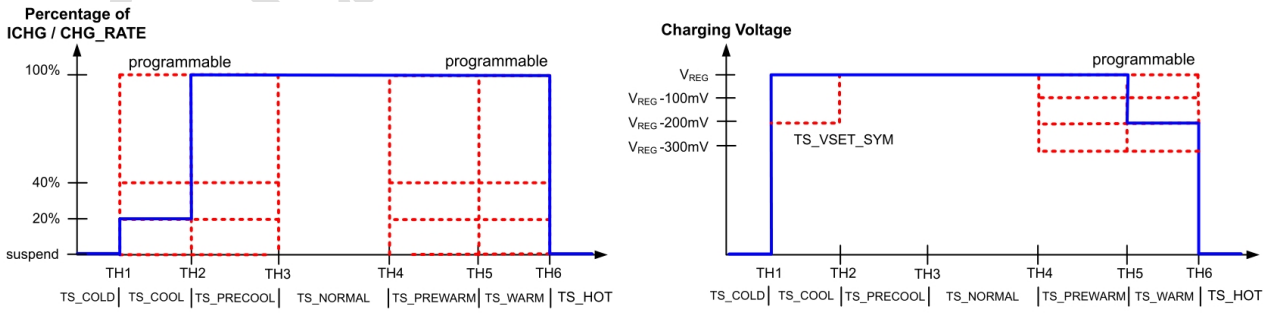


Figure 7 - 4 . TS Charging Value

Charging safety timer is adjusted within the temperature zones to reflect changes to the charging current. When IPRECHG and ICHG are reduced to 20% or 40% in the cool or warm temperature zones, the charging safety timer counts at half rate. If charging is suspended, the safety timer is suspended, the STAT pin blinks

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and CHG_STAT is set to 00 (not charging or charge terminated.)

The typical TS resistor network is illustrated below.

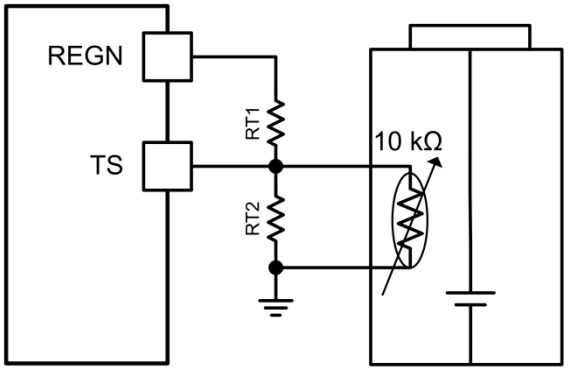


Figure 7-5. TS Resistor Network

The value of RT1 and RT2 are determined from the resistance of the thermistor at 0 and 60ºC (RTH_{0degC} and RTH_{60degC}) and the corresponding voltage thresholds V_{TS_0degC} and V_{TS_60degC} (expressed as percentage of REGN with value between 0 and 1). For the most accurate thermistor curve fitting, use the rising threshold for V_{TS_COLD} at 0ºC and the falling threshold for V_{TS_HOT} at 60ºC, regardless of the actual register settings for TS_TH1_TH2_TH3 and TS_TH4_TH5_TH6.

$$RT2 = \frac{RTH_{0\,deg\,C} \times RTH_{60\,deg\,C} \times \left(\frac{1}{V_{TS_0degC}} - \frac{1}{V_{TS_60degC}}\right)}{RTH_{60\,deg\,C} \times \left(\frac{1}{V_{TS_60degC}} - 1\right) - RTH_{0\,deg\,C} \times \left(\frac{1}{V_{TS_0degC}} - 1\right)} \quad (1)$$

$$RT1 = \frac{\frac{1}{V_{TS_0degC}} - 1}{\frac{1}{R_{T2}} + \frac{1}{RTH_{0degC}}} \quad (2)$$

Assuming a 103AT NTC thermistor on the battery pack, the RT1 and RT2 are calculated to be 5.23 kΩ and 30.1kΩ respectively.

7.3.7.6 Boost Mode Thermistor Monitor During Battery Discharge Mode

For battery protection during boost OTG, CX25601N monitor the battery temperature to be within the TS_TH_OTG_COLD to TS_TH_OTG_HOT register settings. For a 103AT NTC thermistor with RT1 of 5.23 kΩ and RT2 of 30.1 kΩ, TS_TH_OTG_COLD default is -10°C and TS_TH_OTG_HOT default is 60°C. When temperature is outside of this range, the OTG mode is suspended with REGN remaining on. In addition, VBUS_STAT bits are set to 000, TS_STAT is set to 001 (TS_OTG_COLD) or 010 (TS_OTG_HOT), and TS_FLAG is set. Once the battery temperature returns to normal temperature, the boost OTG is restarted and TS_STAT returns to 000 (TS_NORMAL).

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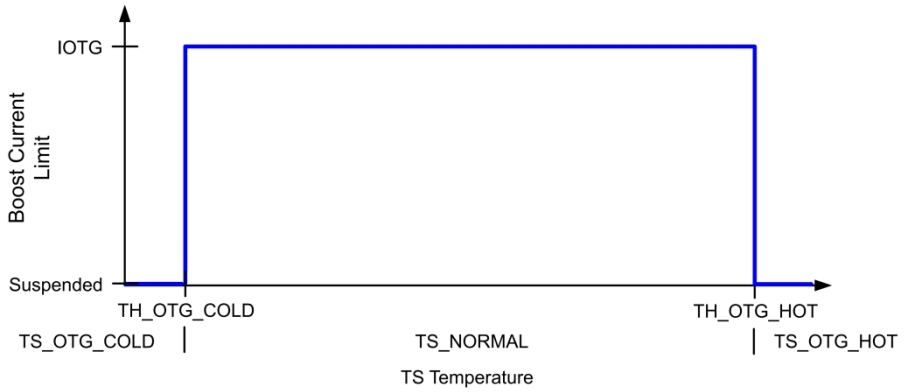


Figure 7-6. TS Pin Thermistor Sense Threshold in Boost Mode

7.3.7.7 Charging Safety Timers

The CX25601N has three built-in safety timers to prevent extended charging cycle due to abnormal battery conditions. The fast charge safety timer and pre-charge safety timers are set through I^2C CHG_TMR and PRECHG_TMR fields, respectively. The trickle charge timer is fixed at 1 hour.

The trickle charging, pre-charging and fast charging safety timers can be disabled by setting EN_SAFETY_TMRS = 0. EN_SAFETY_TMRS can be enabled anytime regardless of which charging stage the charger is in. Each timer starts to count as soon as the following two conditions are simultaneously true: EN_SAFETY_TMRS=1 and the corresponding charging stage is active.

When either the fast charging, trickle charging or pre-charging safety timer expires, the SAFETY_TMR_STAT and SAFETY_TMR_FLAG bits are set to 1.

Events that cause a reduction in charging current also cause the charging safety timer to count at half-clock rate if TMR2X_EN bit is set.

During faults which suspend charging, the charge, pre-charge and trickle safety timers are also suspended, regardless of the state of the TMR2X_EN bit. Once the fault goes away, charging resumes and the safety timer resumes from where it stopped.

The charging safety timer and the charging termination can be disabled at the same time. Under this condition, the charging keeps running until it is disabled by the host.

7.4 Device Functional Modes

7.4.1 Narrow VDC Architecture

The CX25601N uses the Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by VSYSMIN register setting. Even with a fully depleted battery, the system is regulated to the minimum system voltage. If charging is enabled, the BATFET operates in linear mode (LDO mode). The default minimum system voltage at POR is 3.52 V.

As the battery voltage rises above the minimum system voltage, the BATFET is turned fully on. When battery charging is disabled and V_{BAT} is above the minimum system voltage setting, or charging is terminated, the system is regulated 50 mV (typical) above battery voltage.

7.4.2 Dynamic Power Management

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To meet the USB maximum current limit and avoid overloading the adapter, the device features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage. When the input source is overloaded, either the current exceeds the input current limit (IINDPM) or the voltage falls below the input voltage limit (VINDPM). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage by V_{SUPP}, the device automatically enters the supplement mode where the BATFET turns on and the battery starts discharging so that the system is supported from both the input source and battery.

7.4.3 High Impedance Mode

The host may place the CX25601N into high impedance mode by writing EN_HIZ = 1. In high impedance mode, RBFET (Q1), HSFET (Q2) and LSFET (Q3) are turned off. The RBFET and HSFET block current flow to and from VBUS, putting the VBUS pin into a high impedance state. The BATFET (Q4) is turned on to connect the BAT to SYS. During high impedance mode, REGN is disabled and the digital clock is slowed to conserve power.

7.4.4 Shipping Mode and nQON Pin

7.4.4.1 Shipping Mode

The host may place the CX25601N into ship mode by setting BATFET_CTRL = 10. In ship mode, the BATFET is turned off to prevent the battery from powering the system, and the I^2C is disabled. Ship mode has slightly higher quiescent current than shutdown mode. The CX25601N is taken out of ship mode by either of these methods:

- Pulling the nQON pin low for t_{SM_EXIT}
- $V_{VBUS} > V_{VBUS_UVLOZ}$ (adapter plug-in)

When the CX25601N exits from ship mode, the registers are reset to their POR values.

Ship mode is only entered when the adapter is not present. Setting BATFET_CTRL = 10 while $V_{VBUS} > V_{VBUS_UVLOZ}$ (adapter present) either disables the BATFET or has no immediate effect depending on the setting of BATFET_CTRL_WVBUS.

When BATFET_CTRL_WVBUS is set to 0 and $V_{VBUS} > V_{VBUS_UVLO}$ (adapter present), setting BATFET_CTRL = 10 has no immediate effect. If the adapter is removed while BATFET_CTRL is set to 10, then the BATFET is disabled and the device enters ship mode. The BATFET turns off either after t_{BATFET_DLY} or when the adapter is removed, whichever comes later.

When BATFET_CTRL_WVBUS is set to 1 and $V_{VBUS} > V_{VBUS_UVLO}$ (adapter present), setting BATFET_CTRL = 10 turns off the BATFET after t_{BATFET_DLY}. The converter continues to run while the adapter is present, supplying SYS power from the adapter. If the adapter is removed while BATFET_CTRL is set to 10, the CX25601N enters ship mode. Ship mode is entered either after t_{BATFET_DLY} or when the adapter is removed, whichever comes later.

7.4.4.2 System Power Reset

The BATFET functions as a load switch between battery and system when the converter is not running. By changing the state of BATFET from on to off, systems connected to SYS can be power cycled. Any of the

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following conditions initiates a system power reset:

- BATFET_CTRL_WVBUS = 1 and nQON is pulled low for tQON_RST
- BATFET_CTRL_WVBUS = 1 and BATFET_CTRL = 11
- BATFET_CTRL_WVBUS = 0 and VBUS < V_{VBUS_UVLO} simultaneously with nQON pulled low for tQON_RST
- BATFET_CTRL_WVBUS = 0 and VBUS < V_{VBUS_UVLO} and BATFET_CTRL = 11

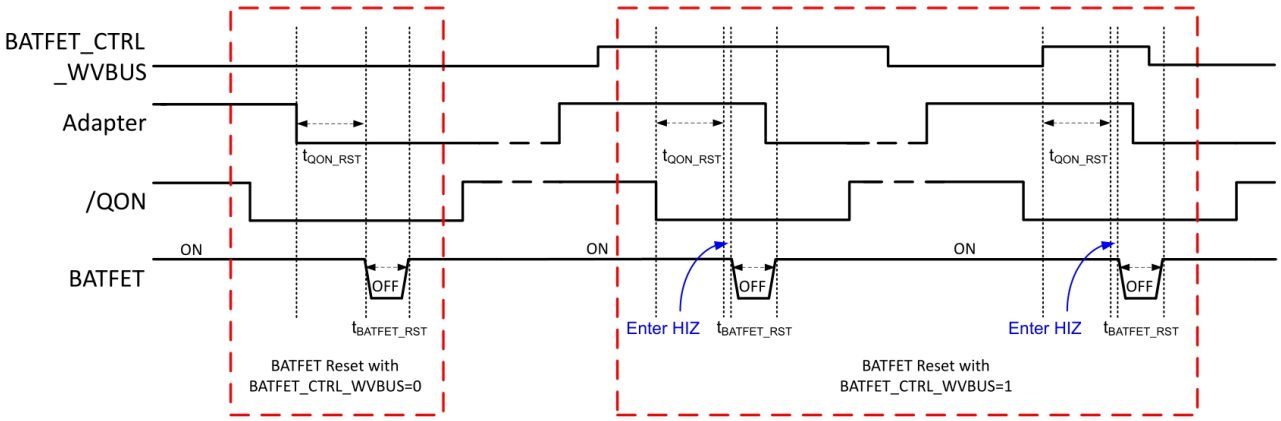


Figure 7-7. System Power Reset Timing

When BATFET_CTRL_WVBUS is set to 1, system power reset proceeds if either BATFET_CTRL is set to 11 or nQON is pulled low for tQON_RST , regardless of whether VBUS is present or not. There is a delay of t_{BATFET_DLY} before initiating the system power reset. If nQON is pulled low, there is no delay after the tQON_RST completes, regardless of BATFET_DLY setting.

The system power reset can be initiated from the battery only condition, from OTG mode or from the forward charging mode with adapter present. If the system power is reset when the charger is in boost OTG mode, the boost OTG mode is first stopped by setting EN_OTG = 0.

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7.4.4.3 BATFET Control

The CX25601N has an integrated, bi-directionally blocking BATFET that can be turned off to remove leakage current from the battery to the system. The BATFET is controlled by the BATFET_CTRL register bits, and supports shutdown mode, ship mode and system power reset.

Table 7-4. BATFET Control Modes

MODE	BATFET	I²C	ENTRY, NO ADAPTER	ENTRY, WITH ADAPTER, BATFET_CTRL_WVBUS = 0	ENTRY, WITH ADAPTER, BATFET_CTRL_WVBUS = 1	EXIT
Normal	On	Active	N/A	N/A	N/A	N/A
Ship mode	Off	Off	Writing BATFET_CTRL =10 turns off BATFET after BATFET_DLY and enters ship mode.	Writing BATFET_CTRL =10 has no effect while adapter is present. When both BATFET_DLY has expired and the adapter is removed, the device turns off BATFET and enters ship mode. Writing BATFET_CTRL = 00 before adapter is removed aborts ship mode.	Writing BATFET_CTRL =10 turns off BATFET after BATFET_DLY. When both BATFET_DLY has expired and adapter is removed, the device enters ship mode. Writing BATFET_CTRL = 00 before adapter is removed turns BATFET on and aborts ship mode.	nQON or adapter plug-in
System reset	On to Off to On	Active	Writing BATFET_CTRL= 11 initiates system reset after BATFET_DLY. Holding nQON low for t_{QON_RST} initiates immediate reset (BATFET_DLY is not applied.)	Writing BATFET_CTRL = 11 is ignored and BATFET_CTRL resets to 00. Holding nQON low for t_{QON_RST} is ignored.	Writing BATFET_CTRL = 11 initiates system reset after BATFET_DLY. Holding nQON low for t_{QON_RST} initiates immediate reset. Converter is placed in HIZ during system reset and exits HIZ when system reset completes.	N/A

7.4.5 Status Outputs (STAT, nINT)

7.4.5.1 Charging Status Indicator (STAT)

The CX25601N indicates charging state on the open drain STAT pin. The STAT pin can drive an LED. The STAT pin function can be disabled via the DIS_STAT bit.

Table 7-5. STAT Pin State

CHARGING STATE	STAT INDICATOR
Charging in progress (including recharge)	LOW
Not charging, no fault detected. (Includes charging complete, Charge Disabled, no adapter present, in OTG mode.)	HIGH
Charge suspend	Blinking at 1 Hz

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7.4.5.2 Interrupt to Host (nINT)

In many applications, the host does not continually poll the charger status registers. Instead, the INT pin may be used to notify the host of a status change with a 256-μs nINT pulse. Upon receiving the interrupt pulse, the host may read the flag registers (Charger_Flag_X and FAULT_Flag_X) to determine the event that caused the interrupt, and for each flagged event, read the corresponding status registers (Charger_Status_X and FAULT_Status_X) to determine the current state. Once set to 1, the flag bits remain latched at 1 until they are read by the host, which clears them. The status bits, however, are updated whenever there is a change to status and always represent the current state of the system.

All of the nINT events can be masked off to prevent nINT pulses from being sent out when they occur, with the exception of the initial power-up interrupt. Interrupt events are masked by setting their mask bit in registers (Charger_Mask_X and FAULT_Mask_X). Events always cause the corresponding flag bit to be set to 1, regardless of whether or not the interrupt pulse has been masked.

7.4.5.3 Interrupts and Status, Flag and Mask Bits

The device incorporates an interrupt pin (nINT) to inform a host microcontroller of status changes without requiring microcontroller polling. Each reported event has a status field, a flag bit and a mask bit. The status field reports the status at the time that it is read. The flag bit is latched and, once set to 1, will remain at 1 until the host reads the bit, which will clear it to 0. The mask bit determines whether or not an interrupt pulse will be generated when the flag bit is set.

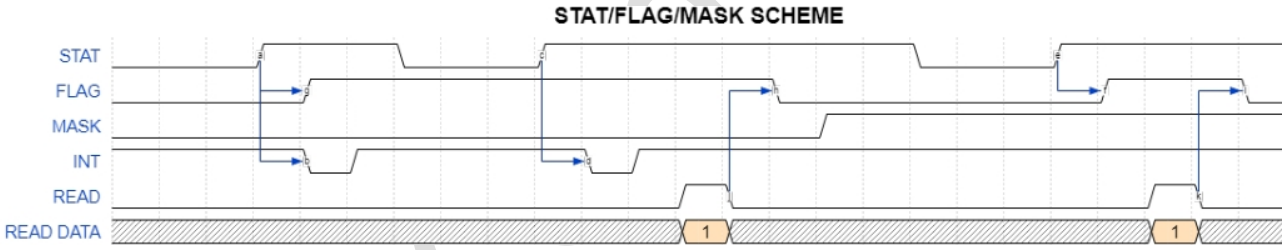


Figure 7-8. Relationship Between STAT, FLAG, and MASK

The flag bit is set upon certain transitions of the status field. These transitions also generate an nINT pulse if the associated mask bit is set to 0. Because the nINT is generated from the status field transition and not the flag bit, an INT pulse is sent to the host even if the associated flag is already set to 1 when the status transition occurs. Details of this behavior are shown in Figure 7-8.

The default behavior is to generate a 256-μs nINT pulse when any flag bit is set to 1. These pulses may be masked out on a flag-by-flag basis by setting a flag's mask bit to 1. Setting the mask bit does not affect the transition of the flag bit from 0 to 1, only the generation of the 256-μs nINT pulse.

7.5 Protections

7.5.1 Voltage and Current Monitoring in Battery Only and HIZ Modes

The CX25601N monitors a reduced set of voltages and currents when operating from battery without an adapter or when operating from battery in high impedance mode.

7.5.1.1 Battery Undervoltage Lockout

In battery-only mode, the CX25601N disables the BATFET if VBAT falls below V_{BAT_UVLO}, separating the system from the battery. I^2C is disabled as well. Upon exit from the undervoltage lockout condition when either

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VBAT rises above V_{BAT_UVLOZ} or V_{VBUS} rises above V_{VBUS_UVLOZ}, I^2C will be re-enabled and the registers are reset to their POR values.

7.5.1.2 Battery Overcurrent Protection

The CX25601N has a two-level battery overcurrent protection. The I_{BAT_PK} threshold is set by IBAT_PK and provides a fast (100 μs) protection for the battery discharging. I_{BATFET_OCP} provides a slower (50 ms), fixed-threshold protection for the BATFET. If the battery discharge current becomes higher than either threshold for its protection timer, the BAT_FAULT_STAT and BAT_FAULT_FLAG fault register bits are set to 1, and the BATFET enters hiccup mode with 100-ms off-time and ~1% on-time. The BAT_FAULT_STAT will return to 0 once the BATFET is disabled for the hiccup mode. Once the BATFET is turned back on, the I_{BAT_PK} and I_{BATFET_OCP} thresholds are re-evaluated. In boost OTG mode, if the battery discharging current is higher than either I_{BAT_PK} or I_{BATFET_OCP} for their respective protection timers, the charger exits OTG mode by clearing the EN_OTG bit.

7.5.2 Voltage and Current Monitoring in Buck Mode

7.5.2.1 Input Overvoltage

If VBUS voltage rises above V_{VBUS_OVP}, the converter stops switching to protect the internal power MOSFETs and I_{PMID_LOAD} discharge current is applied to bring down VBUS voltage. VBUS_FAULT_FLAG and VBUS_FAULT_STAT are set to 1. When VBUS falls back below V_{VBUS_OVPZ}, VBUS_FAULT_STAT will transition to 0 and the converter will resume switching.

7.5.2.2 System Overvoltage Protection (SYSOVP)

When VSYS rises above the V_{SYS_OVP} threshold (around 250 mV above VBAT when not charging) in forward converter operation, the converter stops switching to limit voltage overshoot and applies I_{SYS_LOAD} to pull down the system voltage. VSYS_FAULT_FLAG and VSYS_FAULT_STAT are set to 1. Once VSYS drops below V_{SYS_OVP}, the converter resumes switching, the 15 mA discharge current is removed and VSYS_FAULT_STAT transitions to 0.

7.5.2.3 Forward Converter Cycle-by-Cycle Current Limit

The converter has cycle-by-cycle peak overcurrent protection in the switching MOSFETs. In forward mode, if the current through Q2 exceeds I_{HSFET_OCP}, the converter will immediately turn off the high-side gate drive for the remainder of the switching cycle. Normal switching resumes on the next switching cycle.

7.5.2.4 Battery Overvoltage Protection (BATOVP)

When VBAT transitions above VBAT_OVP , the CX25601N disables charging by disabling the BATFET and applies IBAT_LOAD current source to discharge excess BAT voltage. If battery voltage remains above the threshold , BAT_FAULT_FLAG is set to 1 and BAT_FAULT_STAT transitions to 1. Once VBAT falls below VBAT_OVPZ , charging resumes and BAT_FAULT_STAT transitions back to 0.

7.5.2.5 Sleep and Poor Source Comparators

The sleep comparator is used to suspend the converter if the adapter voltage is insufficient to maintain buck converter operation while charging the battery. If V_{VBUS} falls below V_{BAT} + V_{SLEEP} , the converter stops switching, VBUS_FAULT_STAT and VBUS_FAULT_FLAG are set to 1. If V_{VBUS} rises back above V_{BAT} + V_{SLEEPZ}, the converter restarts.

If V_{VBUS} falls below $V_{POORSRC}$, the converter stops switching and the VBUS_STAT transitions to 000 and the

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device transitions to battery-only mode. If V_{VBUS} rises above $V_{POORSRC}$, it is a new adapter attach, and poor source qualification will be run in addition to D+/D- detection if enabled. VBUS_STAT will be determined by the adapter attach sequence as outlined in Section 7.3.3.

7.5.3 Voltage and Current Monitoring in Boost Mode

CX25601N closely monitors VBUS, SYS and BAT voltages, as well as VBUS, BAT and LSFET currents to ensure safe boost mode operation.

7.5.3.1 Boost Mode Overvoltage Protection

During OTG operation, CX25601N uses two comparators to sense output overvoltage at VBUS and PMID. If either VBUS or PMID voltage rises above their OVP threshholds, the converter stops switching and attempts to discharge the voltage.

If the OVP condition persists (200 μs), OTG_FAULT_FLAG is set to 1, OTG_FAULT_STAT transitions to 1 and the converter powers down into a fault condition.

7.5.3.2 Boost Mode Duty Cycle Protection

After an initial startup blanking period, CX25601N monitors the PMID voltage during boost OTG mode to ensure

that PMID voltage remains sufficiently above VSYS to maintain the minimum duty cycle. If VPMID falls below V_{BOOST_DUTY} (105% V SYS typical), the converter stops and enters hiccup mode.

If the boost converter cannot recover from hiccup mode, EN_OTG bit is cleared and the device exits boost mode. The host may attempt to restart boost OTG mode by setting EN_OTG = 1.

7.5.3.3 Boost Mode PMID Undervoltage Protection

During boost OTG mode, CX25601N converter monitors PMID for undervoltage. If the PMID voltage falls below V_{OTG_UVP}, the converter stops and enters hiccup mode.

If the boost converter cannot recover from hiccup mode, EN_OTG bit is cleared and the device exits boost mode. The host may attempt to restart boost OTG mode by setting EN_OTG = 1.

7.5.3.4 Boost Mode Battery Undervoltage

If V_{BAT} falls below V_{BAT_OTGZ} during OTG mode, the charger exits OTG mode by setting EN_OTG = 0, and BAT_FAULT_STAT and BAT_FAULT_FLAG are set to 1. Setting EN_OTG = 1 while $V_{BAT} < V_{BAT_OTG}$ will not enter OTG and the EN_OTG bit will be cleared to 0. When the battery is charged above V_{BAT_OTG}, OTG mode may be entered by setting EN_OTG = 1.

7.5.3.5 Boost Converter Cycle-by-Cycle Current Limit

The converter has cycle-by-cycle peak overcurrent protection in the switching MOSFETs. In OTG mode, if the current through Q3 exceeds I_{LSFET_OCP}, the converter will immediately turn off the low-side gate drive for the remainder of the switching cycle. Normal switching resumes on the next switching cycle.

7.5.3.6 Boost Mode SYS Short

If VSYS falls below VSYS_SHORT in boost OTG mode, CX25601N immediately stops the boost converter, enters hiccup mode, and sets SYS_FAULT_FLAG to 1.

If the boost converter cannot recover from hiccup mode, EN_OTG bit is cleared and the device exits boost

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mode. The host may attempt to restart boost OTG mode by setting EN_OTG = 1.

7.5.4 Thermal Regulation and Thermal Shutdown

7.5.4.1 Thermal Protection in Buck Mode

The CX25601N monitors the internal junction temperature TJ to avoid overheating the chip and limits the IC junction temperature in buck mode. When the internal junction temperature exceeds the TREG thermal regulation limit (TREG register configuration), the device lowers the charging current. During thermal regulation, the safety timer runs at half the clock rate, and the TREG_FLAG and TREG_STAT bits are set to 1.In this state, the input current limit (IINDPM) setting is temporarily bypassed by the thermal management lo op, and the charging current (ICHG) becomes the dominant variable for thermal foldback control. Adjusting I CHG in real time allows responsive temperature regulation. Additionally, the device has thermal shutdown to turn off the converter and BATFET when IC junction temperature exceeds TSHUT. The fault bit TSHUT_FLAG is set to 1 and TSHUT_STAT transitions to 1. The BATFET and converter are re-enabled when IC temperature is TSHUT_HYS below TSHUT, and TSHUT_STAT transitions to 0.

7.5.4.2 Thermal Protection in Boost Mode

The device monitors the internal junction temperature to provide thermal shutdown during boost mode. When IC junction temperature exceeds T_{SHUT}, the boost mode is disabled by setting EN_OTG bit low and BATFET is turned off, and TSHUT_FLAG is set to 1. When IC junction temperature is below T_{SHUT} - T_{SHUT_HYS}, the BATFET is enabled automatically to allow system to restore and the host can re-enable EN_OTG bit to recover.

7.5.4.3 Thermal Protection in Battery-Only Mode

The CX25601N monitors the internal junction temperature T_J to avoid overheating the chip and limits the IC junction temperature in battery-only mode. The device has thermal shutdown to turn off the BATFET when IC junction temperature exceeds T_{SHUT}. The fault bit TSHUT_FLAG is set to 1 and TSHUT_STAT transitions to 1.The BATFET is re-enabled when IC temperature is T_{SHUT_HYS} below T_{SHUT}, and TSHUT_STAT transitions to 0.

7.6 Programming

7.6.1 Serial Interface

The CX25601N uses an I^2C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I^2C is a bi-directional 2-wire serial interface. Only two open-drain bus lines are required: a serial data line (SDA), and a serial clock line (SCL).

The device has 7-bit I^2C address 0x6B, receiving control inputs from a host device such as a micro-controller or digital signal processor through register addresses 0x02–0x38. The host device initiates all transfers and the charger responds. Register reads outside of these addresses return 0xFF. When the bus is free, both SDA and SCL lines are HIGH.

The I^2C interface supports standard mode (up to 100 kbits/s), fast mode (up to 400 kbits/s) and fast mode plus (up to 1 Mbits/s.) These lines are pulled up to a reference voltage via pull-up resistor. The device I^2C detection thresholds support a communication reference voltage from 1.2 V to 5 V.

Due to the ultra low I_Q when the device operates in low power mode, it is necessary ensure a minimum of 90μs between a START command and any subsequent START command on the I^2C bus. The recommended

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minimum t_{buf} (bus free time between a STOP and START condition) depends on the I^2C mode:

- Standard mode (100 kbits/s):
  - No additional requirements
- Fast mode (400 kbits/s):
  - Increase I^2C t_{buf} to at least 68 µs
  - If using repeated start commands, ensure I^2C tsu:STA is at least 68 µs
- Fast mode plus (1 Mbits/s):
  - Increase I^2C t_{buf} to at least 81 µs
  - If using repeated start commands, ensure I^2C tsu:STA is at least 81 µs

These recommendations assume a successful I^2C transaction. It is also necessary to ensure a minimum 90µs time between two START commands in the case of a NACK.

7.6.1.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

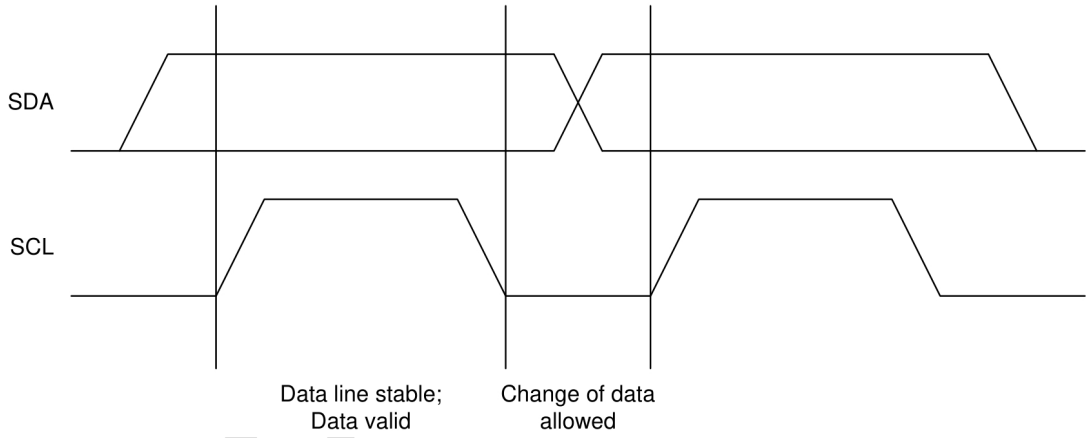


Figure 7-9. Bit Transfer on the I^2C Bus

7.6.1.2 START and STOP Conditions

All transactions begin with a START (S) and are terminated with a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the host. The bus is considered busy after the START condition, and free after the STOP condition.

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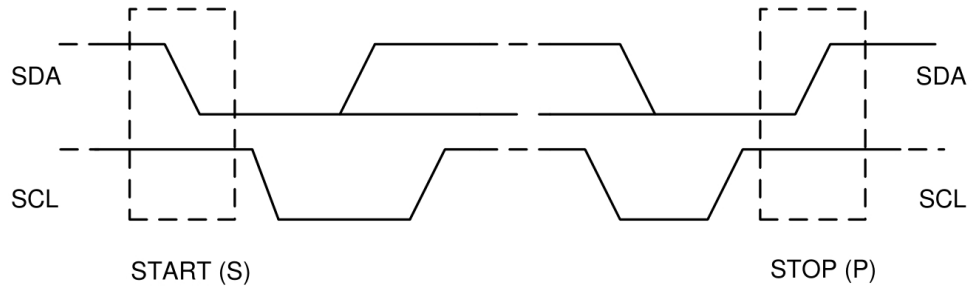


Figure 7-10. START and STOP Conditions on the I²C Bus

7.6.1.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an ACKNOWLEDGE (ACK) bit. Data is transferred with the Most Significant Bit (MSB) first. If target cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the SCL line low to force the host into a wait state (clock stretching). Data transfer then continues when the target is ready for another byte of data and releases the SCL line.

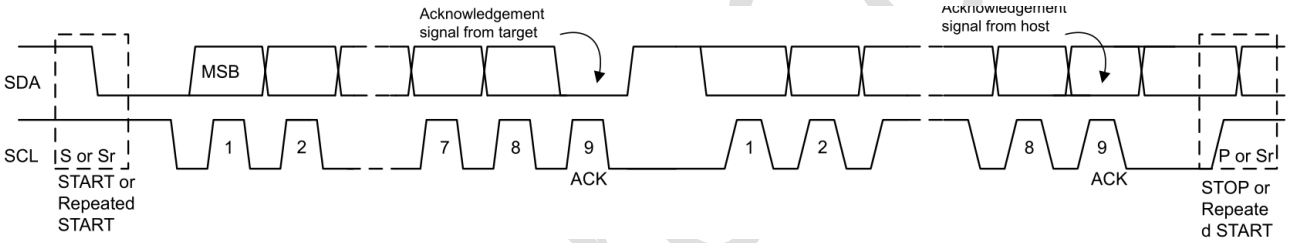


Figure 7-11. Data Transfer on the I²C Bus

7.6.1.4 Acknowledge (ACK) and Not Acknowledge (NACK)

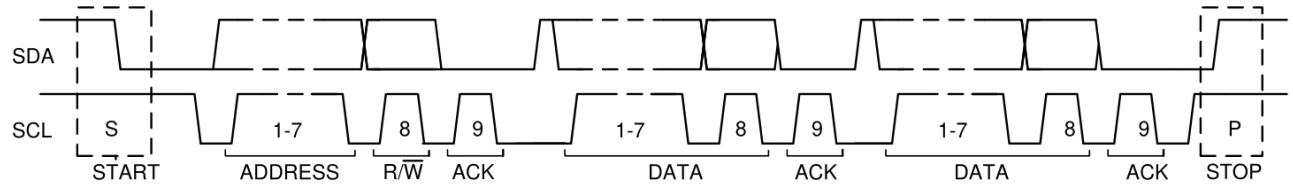
The ACK signaling takes place after each transmitted byte. The ACK bit allows the target to signal the host that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the host.

The host releases the SDA line during the acknowledge clock pulse so the target can pull the SDA line LOW and it remains stable LOW during the HIGH period of this 9th clock pulse.

A NACK is signaled when the SDA line remains HIGH during the 9th clock pulse. The host can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

7.6.1.5 Target Address and Data Direction Bit

After the START signal, a target address is sent. This address is 7 bits long, followed by the 8 bit as a data direction bit (bit R/nW). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ). The device 7-bit address is defined as 1101 011' (0x6B).



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Figure 7-12. Complete Data Transfer on the I²C Bus

7.6.1.6 Single Write and Read

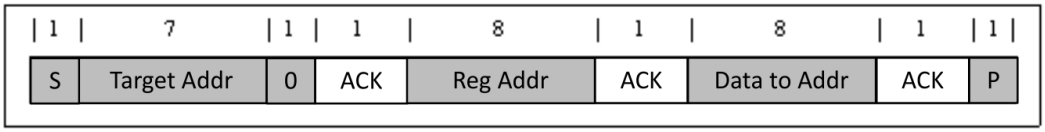


Figure 7-13. Single Write

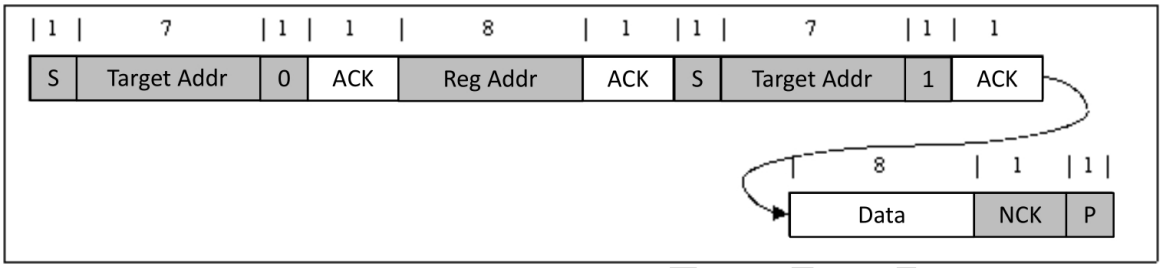


Figure 7-14. Single Read

If the register address is not defined, the charger IC sends back NACK and returns to the idle state.

7.6.1.7 Multi-Write and Multi-Read

The charger device supports multi-byte read and multi-byte write of all registers. These multi-byte operations are allowed to cross register boundaries. For instance, the entire register map may be read in a single operation with a 39-byte read that starts at register address 0x01.

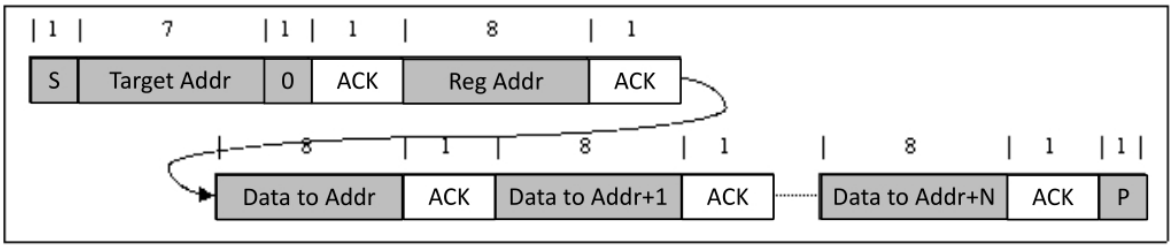


Figure 7-15. Multi-Write

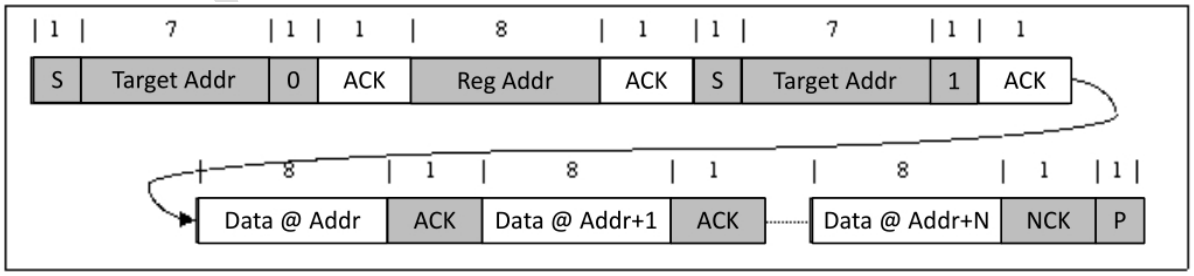


Figure 7-16. Multi-Read

7.7 Register Maps

I²C Device Address: 0x6B.

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7.7.1 Register Programming

The CX25601N contains 8-bit and 16-bit registers. When writing to 16-bit registers, I²C transactions follow the little endian format, starting at the address of the least significant byte and writing both register bytes in a single 16-bit transaction.

7.7.2 CX25601N Registers

Table 7-6 lists the memory-mapped registers for the CX25601N registers. All register offset addresses not listed in Table 7-6 should be considered as reserved locations and the register contents should not be modified.

Table 7-6. CX25601N Registers

Address	Acronym	Register Name
2h	REG0x02_Charge_Current_Limit	Charge Current Limit
4h	REG0x04_Charge_Voltage_Limit	Charge Voltage Limit
6h	REG0x06_Input_Current_Limit	Input Current Limit
8h	REG0x08_Input_Voltage_Limit	Input Voltage Limit
Ah	REG0x0A_IOTG_regulation	IOTG regulation
Ch	REG0x0C_VOTG_regulation	VOTG regulation
Eh	REG0x0E_Minimal_System_Voltage	Minimal System Voltage
10h	REG0x10_Pre-charge_Control	Pre-charge Control
12h	REG0x12_Termination_Control	Termination Control
14h	REG0x14_Charge_Control_0	Charge Control 0
15h	REG0x15_Charge_Timer_Control	Charge Timer Control
16h	REG0x16_Charger_Control_1	Charger Control 1
17h	REG0x17_Charger_Control_2	Charger Control 2
18h	REG0x18_Charger_Control_3	Charger Control 3
19h	REG0x19_Charger_Control_4	Charger Control 4
1Ah	REG0x1A_NTC_Control_0	NTC Control 0
1Bh	REG0x1B_NTC_Control_1	NTC Control 1
1Ch	REG0x1C_NTC_Control_2	NTC Control 2
1Dh	REG0x1D_Charger_Status_0	Charger Status 0
1Eh	REG0x1E_Charger_Status_1	Charger Status 1
1Fh	REG0x1F_FAULT_Status_0	FAULT Status 0
20h	REG0x20_Charger_Flag_0	Charger Flag 0
21h	REG0x21_Charger_Flag_1	Charger Flag 1
22h	REG0x22_FAULT_Flag_0	FAULT Flag 0
23h	REG0x23_Charger_Mask_0	Charger Mask 0
24h	REG0x24_Charger_Mask_1	Charger Mask 1
25h	REG0x25_FAULT_Mask_0	FAULT Mask 0
38h	REG0x38_Part_Information	Part Information

Complex bit access types are encoded to fit into small table cells. Table 7-7 shows the codes that are used for access types in this section.

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Table 7-7. CX25601N Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

Register Maps

REG0x02_Charge_Current_Limit Register

Bit	Field	Type	Reset	Notes	Description
15:12	RESERVED	R	0h		Reserved
11:6	ICHG	R/W	0Dh	WATCHDOG Timer Expiration sets ICHG to 1/2 its previous value (rounded down) Reset by: REG_RESET	Charge Current Regulation Limit: This 16-bit register follows the little-endian convention. ICHG[5:2] falls in REG0x03[3:0], and ICHG[1:0] falls in REG0x02[7:6]. POR: 1040mA (Dh) Range: 80mA-3040mA (1h-26h) Clamped Low Clamped High Bit Step: 80mA (1h)
5:0	RESERVED	R	0h		Reserved

REG0x04_Charge_Voltage_Limit Register

Bit	Field	Type	Reset	Notes	Description
15:12	RESERVED	R	0h		Reserved
11:3	VREG	R/W	1A4h	Reset by: REG_RESET	Battery Voltage Regulation Limit: This 16-bit register follows the little-endian convention. VREG[8:5] falls in REG0x05[3:0], and VREG[4:0] falls in REG0x04[7:3]. POR: 4200mV (1A4h) Range: 3840mV-4800mV (180h-1E0h) Clamped Low Clamped High Bit Step: 10mV
2:0	RESERVED	R	0h		Reserved

REG0x06_Input_Current_Limit Register

Bit	Field	Type	Reset	Notes	Description
15:12	RESERVED	R	0h		Reserved

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11:4	IINDPM	R/W	96h	Reset by: REG_RESET Adapter Removal	Input Current Regulation Limit: This 16-bit register follows the little-endian convention. IINDPM[7:4] falls in REG0x07[3:0], and IINDPM[3:0] falls in REG0x06[7:4]. CX25601N: Based on D+/D- detection results: USB SDP = 500mA USB CDP = 1.5A USB DCP = 1.5A USB HVDCP = 1.5A Unknown Adapter = 500mA Non-Standard Adapter = 1A/2.1A/2.4A POR: 3000mA (96h) Range: 100mA-3000mA (5h-96h) Clamped Low Clamped High Bit Step: 20mA When the adapter is removed, IINDPM is reset to its POR value of 3.0 A
3:0	RESERVED	R	0h		Reserved

REG0x08_Input_Voltage_Limit Register

Bit	Field	Type	Reset	Notes	Description
15:14	RESERVED	R	0h		Reserved
13:5	VINDPM	R/W	73h		Absolute Input Voltage Regulation Limit: This 16-bit register follows the little-endian convention. VINDPM[8:3] falls in REG0x09[5:0], and VINDPM[2:0] falls in REG0x08[7:5]. POR: 4600mV (73h) Range: 3800mV-13200mV (5Fh-14Ah) Clamped Low Clamped High Bit Step: 40mV
4:0	RESERVED	R	0h		Reserved

REG0x0A_IOTG_regulation Register

Bit	Field	Type	Reset	Notes	Description
15:12	RESERVED	R	0h		Reserved
11:4	IOTG	R/W	32h	Reset by: REG_RESET WATCHDOG	OTG mode current regulation limit: This 16-bit register follows the little-endian convention. IOTG[7:4] falls in REG0x0B[3:0], and IOTG[3:0] falls in REG0x0A[7:4]. POR: 1000mA (32h) Range: 100mA-1200mA (5h-3Ch) Clamped Low

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					Clamped High Bit Step: 20mA
3:0	RESERVED	R	0h		Reserved

REG0x0C_VOTG_regulation Register

Bit	Field	Type	Reset	Notes	Description
15:13	RESERVED	R	0h		Reserved
12:6	VOTG	R/W	3Fh	Reset by: REG_RESET	OTG mode regulation voltage: This 16-bit register follows the little-endian convention. VOTG[6:2] falls in REG0x0D[4:0], and VOTG[1:0] falls in REG0x0C[7:6]. POR: 5040mV (3Fh) Range: 3840mV-5280mV (30h-42h) Clamped Low Clamped High Bit Step: 80mV
	RESERVED	R	0h		Reserved

REG0x0E_Minimal_System_Voltage Register

Bit	Field	Type	Reset	Notes	Description
15:12	RESERVED	R	0h		Reserved
11:6	VSYSMIN	R/W	2Ch	Reset by: REG_RESET	Minimal System Voltage: This 16-bit register follows the little-endian convention. VSYSMIN[5:2] falls in REG0x0F[3:0], and VSYSMIN[1:0] falls in REG0x0E[7:6]. POR: 3520mV (2Ch) Range: 2560mV-3840mV (20h-30h) Clamped Low Clamped High Bit Step: 80mV
5:0	RESERVED	R	0h		Reserved

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REG0x10_Pre-charge_Control Register

Bit	Field	Type	Reset	Notes	Description
15:9	RESERVED	R	0h		Reserved
8:4	IPRECHG	R/W	5h	Reset by: REG_RESET	Pre-charge current regulation limit: This 16-bit register follows the little-endian convention. IPRECHG[4] falls in REG0x11[0], and IPRECHG[3:0] falls in REG0x10[7:4] POR: 100mA (5h) Range: 100mA-620mA (5h-1Fh) Clamped Low Bit Step: 20mA (1h)
3:0	RESERVED	R	0h		Reserved

REG0x12_Termination_Control Register

Bit	Field	Type	Reset	Notes	Description
15:9	RESERVED	R	0h		Reserved
8:3	ITERM	R/W	0Ah	Reset by: REG_RESET	Termination Current Threshold: This 16-bit register follows the little-endian convention.ITERM[5] falls in REG0x13[0], and ITERM[4:0] falls in REG0x12[7:3]. POR: 100mA (Ah) Range: 60mA-620mA (6h-3Eh) Clamped Low Bit Step: 10mA (1h)
2:0	RESERVED	R	0h		Reserved

REG0x14_Charge_Control_0 Register

Bit	Field	Type	Reset	Notes	Description
7	Q1_FULLON	R/W	0h		Forces RBFET (Q1) into low resistance state (30 mOhm) , regardless of IINDPM setting. 0b = RBFET RDSON determined by IINDPM setting(default) 1b = RBFET RDSON is always 30 mOhm
6	Q4_FULLON	R/W	0h		Forces BATFET (Q4) into low resistance state (15 mOhm), regardless of ICHG setting. (Only applies when VBAT > VSYSMIN. Otherwise BATFET operates in linear mode.) 0b = BATFET RDSON determined by charge current (default) 1b = BATFET RDSON is always 20 mOhm
5	ITRICKLE	R/W	0h	Reset by: REG_RESET	Trickle charging current setting: 0b = 17mA (default) 1b = 65mA

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4:3	TOPOFF_TMR	R/W	0h	Reset by: REG_RESET	Top-off timer control: 00b = Disabled (default) 01b = 15 mins 10b = 30 mins 11b = 45 mins
2	EN_TERM	R/W	1h	Reset by: REG_RESET WATCHDOG	Enable termination 0b = Disable 1b = Enable (default)
1	VINDPM_BAT_TRACK	R/W	1h	Reset by: REG_RESET	Sets VINDPM to track BAT voltage. Actual VINDPM is higher of the VINDPM register value and VBAT + VINDPM_BAT_TRACK. 0b = Disable function (VINDPM set by register) 1b = VBAT + 400 mV (default)
0	RESERVED	R	0h		Reserved

REG0x15_Charge_Timer_Control Register

Bit	Field	Type	Reset	Notes	Description
7	DIS_STAT	R/W	0h	Reset by: REG_RESET	Disable the STAT pin output 0b = Enable (default) 1b = Disable
6	EN_AUTO_INDET	R/W	1h	Reset by: REG_RESET WATCHDOG	Automatic D+/D- Detection Enable 0b = Disable DPDM detection when VBUS is plugged-in 1b = Enable DPDM detection when VBUS is plugged-in (default)
5	FORCE_INDET	R/W	0h	Reset by: REG_RESET WATCHDOG	Force D+/D- detection 0b = Do not force DPDM detection (default) 1b = Force DPDM algorithm, when DPDM detection is done, this bit is reset to 0
4	EN_DCP_BIAS	R/W	1h	Reset by: REG_RESET WATCHDOG	Enable 600 mV bias on D+ pin whenever DCP is detected by BC1.2 detection algorithm (VBUS_STAT= 011b.) 0b = Disable 600 mV bias on D+ pin 1b = Enable 600 mV bias on D+ pin if DCP detected
3	TMR2X_EN	R/W	1h	Reset by: REG_RESET	2X charging timer control 0b = Trickle charge, pre-charge and fast charge timer not slowed by 2X during input DPM or thermal regulation. 1b = Trickle charge, pre-charge and fast charge timer slowed by 2X during input DPM or thermal regulation (default)
2	EN_SAFETY_TMRS	R/W	1h	Reset by: REG_RESET WATCHDOG	Enable fast charge, pre-charge and trickle charge timers 0b = Disable 1b = Enable (default)
1	PRECHG_TMR	R/W	0h	Reset by:	Pre-charge safety timer setting

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				REG_RESET	0b = 2 hrs (default) 1b = 0.5 hrs
0	CHG_TMR	R/W	0h	Reset by: REG_RESET	Fast charge safety timer setting 0b = 12 hrs (default) 1b = 24 hrs

REG0x16_Charger_Control_1 Register

Bit	Field	Type	Reset	Notes	Description
7	EN_AUTO_IBATDIS	R/W	1h	Reset by: REG_RESET	Enable the auto battery discharging during the battery OVP fault 0b = The charger does NOT apply a discharging current on BAT during battery OVP triggered 1b = The charger does apply a discharging current on BAT during battery OVP triggered (default)
6	RESERVED	R	0h		Reserved
5	EN_CHG	R/W	1h	Reset by: REG_RESET WATCHDOG	Charger enable configuration 0b = Charge Disable 1b = Charge Enable (default)
4	EN_HIZ	R/W	0h	Reset by: REG_RESET WATCHDOG Adapter Plug In	Enable HIZ mode. 0b = Disable (default) 1b = Enable
3	RESERVED	R	0h		Reserved
2	WD_RST	R/W	0h	Reset by: REG_RESET	I^2C watch dog timer reset 0b = Normal (default) 1b = Reset (this bit goes back to 0 after timer reset)
1:0	WATCHDOG	R/W	1h	Reset by: REG_RESET	Watchdog timer setting 00b = Disable 01b = 50s (default) 10b = 100s 11b = 200s

REG0x17_Charger_Control_2 Register

Bit	Field	Type	Reset	Notes	Description
7	REG_RST	R/W	0h	REG_RESET	Reset registers to default values and reset timer Value resets to 0 after reset completes. 0b = Not reset (default) 1b = Reset
6	TREG	R/W	1h	Reset by: REG_RESET	Thermal regulation thresholds. 0b = 60℃ 1b = 120℃ (default)
5:4	SET_CONV_FREQ	R/W	0h	Reset by: REG_RESET	Adjust switching frequency of the converter 00b = Nominal, 1.1 MHz (default)

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					01b = - 10%, 0.99 MHz 10b = + 10%, 1.21 MHz 11b = RESERVED
3:2	SET_CONV_STRN	R/W	3h	Reset by: REG_RESET	Adjust the high side and low side drive strength of the converter to adjust efficiency versus EMI. 00b = weak 01b = normal 10b = RESERVED 11b = strong (default)
1	RESERVED	R	0h		Reserved
0	VBUS_OVP	R/W	1h	Reset by: REG_RESET	Sets VBUS overvoltage protection threshold 0b = 6.4 V 1b = 13 V (default)

REG0x18_Charger_Control_3 Register

Bit	Field	Type	Reset	Notes	Description
7	RESERVED	R	0h		Reserved
6	EN_OTG	R/W	0h	Reset by: REG_RESET WATCHDOG	OTG mode control 0b = OTG Disable (default) 1b = OTG Enable
5	PFM_OTG_DIS	R/W	0h	Reset by: REG_RESET	Disable PFM in OTG boost mode 0b = Enable (default) 1b = Disable
4	PFM_FWD_DIS	R/W	0h	Reset by: REG_RESET	Disable PFM in forward buck mode 0b = Enable (default) 1b = Disable
3	BATFET_CTRL_WVBUS	R/W	0h		Optionally allows BATFET off or system power reset with adapter present. 0b = Allow BATFET off or system power reset only if VBUS < VVBUS_UVLO. (default) 1b = Allow BATFET off or system power reset whether or not VBUS < VVBUS_UVLO.
2	BATFET_DLY	R/W	1h	Reset by: REG_RESET	BATFET_CTRL [1:0] Additional Delay Time Introduced by the Operation 0h = 24 ms additional delay
1:0	BATFET_CTRL	R/W	0h	Reset by: REG_RESET	BATFET control The control logic of the BATFET to force the device enter different modes. 00b = Normal (default) 01b = Shutdown Mode 10b = Ship Mode 11b = System Power Reset

REG0x19_Charger_Control_4 Register

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Bit	Field	Type	Reset	Notes	Description
7:6	IBAT_PK	R/W	3h	Reset by: REG_RESET	Battery discharging peak current protection threshold setting 00b = RESERVED 01b = RESERVED 10b = 6A 11b = 13A (default)
5	VBAT_UVLO	R/W	0h	Reset by: REG_RESET	Select the VBAT_UVLO falling threshold and VBAT_SHORT threshold 0b = VBAT_UVLO 2.2V, VBAT_SHORT 2.05V (default) 1b = VBAT_UVLO 1.8V, VBAT_SHORT 1.85V
4	VBAT_OTG_MIN	R/W	0h	Reset by: REG_RESET	Select the minimal battery voltage to start the OTG mode 0b = 3V rising / 2.8V falling (default) 1b = 2.6V rising / 2.4V falling
3	EN_9V	R/W	0h	Reset by: REG_RESET	Enable 9V adapter detection 0b = Disabled (default) 1b = Enabled
2	RESERVED	R	0h		Reserved
1:0	CHG_RATE	R/W	0h	Reset by: REG_RESET	The charge rate definition for the fast charge stage. The charging current fold back value is equal to ICHG register setting times the fold back ratio, then divided by the charge rate. 00b = 1C (default) 01b = 2C 10b = 4C 11b = 6C

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REG0x1A_NTC_Control_0 Register

Bit	Field	Type	Reset	Notes	Description
7	TS_IGNORE	R/W	0h	Reset by: REG_RESET WATCHDOG	Ignore the TS feedback: the charger considers the TS is always good to allow charging and OTG modes, TS_STAT reports TS_NORMAL condition. 0b = Not ignore (Default) 1b = Ignore
6:5	TS_TH_OTG_HOT	R/W	1h	Reset by: REG_RESET	OTG Mode TS_HOT rising temperature threshold to transition from normal operation into suspended OTG mode when a 103AT NTC thermistor is used, RT1=5.23kΩ and RT2=30.1kΩ. 00b = 55°C 01b = 60°C (default) 10b = 65°C 11b = Disable
4	TS_TH_OTG_COLD	R/W	1h	Reset by: REG_RESET	OTG Mode TS_COLD falling temperature threshold to transition from normal operation into suspended OTG mode when a 103AT NTC thermistor is used, RT1=5.23kΩ and RT2=30.1kΩ. 0b = -20°C 1b = -10°C (default)
3:2	TS_ISET_WARM	R/W	3h	Reset by: REG_RESET	TS_WARM Current Setting 00b = Charge Suspend 01b = Set ICHG to 20% 10b = Set ICHG to 40% 11b = ICHG unchanged (default)
1:0	TS_ISET_COOL	R/W	1h	Reset by: REG_RESET	TS_COOL Current Setting 00b = Charge Suspend 01b = Set ICHG to 20% (default) 10b = Set ICHG to 40% 11b = ICHG unchanged

REG0x1B_NTC_Control_1 Register

Bit	Field	Type	Reset	Notes	Description
7:5	TS_TH1_TH2_TH3	R/W	1h	Reset by: REG_RESET	TH1, TH2 and TH3 comparator falling temperature thresholds when a 103AT NTC thermistor is used, RT1=5.23kΩ and RT2=30.1kΩ. 000b = TH1 is 0°C, TH2 is 5°C, TH3 is 15°C 001b = TH1 is 0°C, TH2 is 10°C, TH3 is 15°C (default) 010b = TH1 is 0°C, TH2 is 15°C, TH3 is 20°C 011b = TH1 is 0°C, TH2 is 20°C, TH3 20°C 100b = TH1 is -5°C, TH2 is 5°C, TH3 is 15°C 101b = TH1 is -5°C, TH2 is 10°C, TH3 is 15°C

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					110b = TH1 is -5°C, TH2 is 10°C, TH3 is 20°C 111b = TH1 is 0°C, TH2 is 10°C, TH3 is 20°C
4:2	TS_TH4_TH5_TH6	R/W	1h	Reset by: REG_RESET	TH4, TH5 and TH6 comparator rising temperature thresholds when a 103AT NTC thermistor is used, RT1=5.23kΩ and RT2=30.1kΩ. 000b = TH4 is 35°C, TH5 is 40°C, TH6 is 60°C 001b = TH4 is 35°C, TH5 is 45°C, TH6 is 60°C (default) 010b = TH4 is 35°C, TH5 is 50°C, TH6 is 60°C 011b = TH4 is 40°C, TH5 is 55°C, TH6 is 60°C 100b = TH4 is 35°C, TH5 is 40°C, TH6 is 50°C 101b = TH4 is 35°C, TH5 is 45°C, TH6 is 50°C 110b = TH4 is 40°C, TH5 is 45°C, TH6 is 60°C 111b = TH4 is 40°C, TH5 is 50°C, TH6 is 60°C
1:0	TS_VSET_WARM	R/W	1h	Reset by: REG_RESET	TS_WARM Voltage Setting 00b = Set VREG to VREG-300mV 01b = Set VREG to VREG-200mV (default) 10b = Set VREG to VREG-100mV 11b = VREG unchanged

REG0x1C_NTC_Control_2 Register

Bit	Field	Type	Reset	Notes	Description
7	RESERVED	R	0h		Reserved
6	TS_VSET_SYM	R/W	0h	Reset by: REG_RESET	When this bit is set to 0, the voltage regulation for TS_PRECOOL and TS_COOL is unchanged. When this bit is set to 1, TS_PRECOOL uses the TS_VSET_PREWARM setting of TS_PREWARM and TS_COOL uses the TS_VSET_WARM setting of TS_WARM . 00b = VREG unchanged (default) 01b = TS_COOLx matches TS_WARMx
5:4	TS_VSET_PREWARM	R/W	3h	Reset by: REG_RESET	Advanced temperature profile voltage setting for TS_PREWARM (TH4 - TH5) 00b = Set VREG to VREG-300mV 01b = Set VREG to VREG-200mV 10b = Set VREG to VREG-100mV 11b = VREG unchanged (default)
3:2	TS_ISET_PREWARM	R/W	3h	Reset by: REG_RESET	Advanced temperature profile current setting for TS_PREWARM zone(TH4 - TH5) 00b = Charge Suspend 01b = Set ICHG to 20% 10b = Set ICHG to 40% 11b = ICHG unchanged (default)

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1:0	TS_ISET_PRECOOL	R/W	3h	Reset by: REG_RESET	Advanced temperature profile current setting for TS_PRECOOL zone (TH2 - TH3) 00b = Charge Suspend 01b = Set ICHG to 20% 10b = Set ICHG to 40% 11b = ICHG unchanged (default)

REG0x1D_Charger_Status_0 Register

Bit	Field	Type	Reset	Notes	Description
7:6	RESERVED	R	0h		Reserved
5	TREG_STAT	R	0h		IC Thermal regulation status 0b = Normal 1b = Device in thermal regulation
4	VSYS_STAT	R	0h		VSYS Regulation Status (forward mode) 0b = Not in VSYSMIN regulation (BAT>VSYSMIN) 1b = In VSYSMIN regulation (BAT<VSYSMIN)
3	IINDPM_STAT	R	0h		In forward mode, indicates that either IINDPM regulation is active or ILIM pin regulation is active In OTG mode, indicates that IOTG regulation is active 0b = Normal 1b = In IINDPM/ILIM regulation or IOTG regulation
2	VINDPM_STAT	R	0h		VINDPM status (forward mode) or VOTG status (OTG mode, backup mode) 0b = Normal 1b = In VINDPM regulation or VOTG regulation
1	SAFETY_TMR_STAT	R	0h		Fast charge, trickle charge and pre-charge timer status 0b = Normal 1b = Safety timer expired
0	WD_STAT	R	0h		I^2C watch dog timer status 0b = Normal 1b = WD timer expired

REG0x1E_Charger_Status_1 Register

Bit	Field	Type	Reset	Notes	Description
7:5	RESERVED	R	0h		Reserved
4:3	CHG_STAT	R	0h		Charge Status bits 00b = Not Charging or Charge Terminated 01b = Trickle Charge, Pre-charge or Fast charge (CC mode) 10b = Taper Charge (CV mode) 11b = Top-off Timer Active Charging

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2:0	VBUS_STAT	R	0h		VBUS status bits 000b = No qualified adapter, or EN_AUTO_INDET = 0. 001b = USB SDP Adapter (500mA) 010b = USB CDP Adapter (1.5A) 011b = USB DCP Adapter (1.5A) 100b = Unknown Adapter (500mA) 101b = Non-Standard Adapter (1A/2.1A/2.4A) 110b = HVDCP adapter (1.5A) 111b = In boost OTG mode

REG0x1F_FAULT_Status_0 Register

Bit	Field	Type	Reset	Notes	Description
7	VBUS_FAULT_STAT	R	0h		VBUS fault status, VBUS OVP and sleep comparator 0b = Normal 1b = Device not switching due to over voltage protection or sleep comparator
6	BAT_FAULT_STAT	R	0h		BAT fault status, IBAT OCP and VBAT OVP 0b = Normal 1b = Device in battery over current protection or battery overvoltage protection
5	SYS_FAULT_STAT	R	0h		VSYS under voltage and over voltage status 0b = Normal 1b = SYS in SYS short circuit or over voltage
4	OTG_FAULT_STAT	R	0h		Reverse-current or undervoltage or overvoltage fault detected at PMID or VBUS during boost OTG 0b = Normal 1b = Reverse-current fault or PMID or VBUS in over voltage or under voltage during OTG
3	TSHUT_STAT	R	0h		IC temperature shutdown status 0b = Normal 1b = Device in thermal shutdown protection
2:0	TS_STAT	R	0h		The TS temperature zone. 000b = TS_NORMAL 001b = TS_COLD or TS_OTG_COLD or TS resistor string power rail is not available. 010b = TS_HOT or TS_OTG_HOT 011b = TS_COOL 100b = TS_WARM 101b = TS_PRECOOL 110b = TS_PREWARM 111b = TS pin bias reference fault

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REG0x20_Charger_Flag_0 Register

Bit	Field	Type	Reset	Notes	Description
7:6	RESERVED	R	0h		RESERVED
5	TREG_FLAG	R	0h		IC Thermal regulation flag 0b = Normal 1b = TREG signal rising threshold detected
4	VSYS_FLAG	R	0h		VSYS min regulation flag 0b = Normal 1b = Entered or existed VSYS min regulation
3	IINDPM_FLAG	R	0h		Indicates that either the IINDPM regulation loop, ILIM pin regulation or IOTG regulation loop has been entered. 0b = Normal 1b = IINDPM, ILIM or IOTG regulation signal rising edge detected
2	VINDPM_FLAG	R	0h		VINDPM or VOTG flag 0b = Normal 1b = VINDPM or VOTG regulation signal rising edge detected
1	SAFETY_TMR_FLAG	R	0h		Fast charge, trickle charge and pre-charge timer flag 0b = Normal 1b = Fast charge timer expired rising edge detected
0	WD_FLAG	R	0h		I^2C watchdog timer flag 0b = Normal 1b = WD timer signal rising edge detected

REG0x21_Charger_Flag_1 Register

Bit	Field	Type	Reset	Notes	Description
7:4	RESERVED	R	0h		Reserved
3	CHG_FLAG	R	0h		Charge status flag 0b = Normal 1b = Charge status changed
2:1	RESERVED	R	0h		Reserved
0	VBUS_FLAG	R	0h		VBUS status flag 0b = Normal 1b = VBUS status changed

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REG0x22_FAULT_Flag_0 Register

Bit	Field	Type	Reset	Notes	Description
7	VBUS_FAULT_FLAG	R	0h		VBUS over-voltage or sleep flag 0b = Normal 1b = Entered VBUS OVP or sleep
6	BAT_FAULT_FLAG	R	0h		IBAT over-current and VBAT over-voltage flag 0b = Normal 1b = Entered battery discharged OCP or VBAT OVP
5	SYS_FAULT_FLAG	R	0h		VSYS over voltage and SYS short flag 0b = Normal 1b = Stopped switching due to system over-voltage or SYS short fault
4	OTG_FAULT_FLAG	R	0h		OTG PMID and VBUS reverse-current, under voltage and over voltage flag 0b = Normal 1b = Stopped OTG due to reverse-current fault, PMID under voltage or over voltage fault
3	TSHUT_FLAG	R	0h		IC thermal shutdown flag 0b = Normal 1b = TS shutdown signal rising threshold detected
2:1	RESERVED	R	0h		Reserved
0	TS_FLAG	R	0h		TS status flag 0b = Normal 1b = A change to TS status was detected

REG0x23_Charger_Mask_0 Register

Bit	Field	Type	Reset	Notes	Description
7:6	RESERVED	R	0h		Reserved
5	TREG_MASK	R/W	0h	Reset by: REG_RESET	IC thermal regulation mask flag 0b = Entering TREG does produce nINT 1b = Entering TREG does not produce nINT
4	VSYS_MASK	R/W	0h	Reset by: REG_RESET	VSYS min regulation mask flag 0b = Enter or exit VSYSMIN regulation does produce nINT pulse 1b = Enter or exit VSYSMIN regulation does not produce nINT pulse
3	IINDPM_MASK	R/W	0h	Reset by: REG_RESET	IINDPM, ILIM or IOTG mask 0b = Enter IINDPM, ILIM or IOTG does produce nINT pulse 1b = Enter IINDPM, ILIM or IOTG does not produce nINT pulse
2	VINDPM_MASK	R/W	0h	Reset by: REG_RESET	VINDPM or VOTG mask 0b = Enter VINDPM or VOTG does produce nINT pulse

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					1b = Enter VINDPM or VOTG does not produce nINT pulse
1	SAFETY_TMR_MASK	R/W	0h	Reset by: REG_RESET	Fast charge, trickle charge and pre-charge timer mask flag 0b = Fast charge, trickle charge or pre-charge timer expiration does produce nINT 1b = Fast charge, trickle charge or pre-charge timer expiration does not produce nINT
0	WD_MASK	R/W	0h	Reset by: REG_RESET	I^2C watch dog timer mask 0b = I^2C watch dog timer expired does produce nINT pulse 1b = I^2C watch dog timer expired does not produce nINT pulse

REG0x24_Charger_Mask_1 Register

Bit	Field	Type	Reset	Notes	Description
7:4	RESERVED	R	0h		Reserved
3	CHG_MASK	R/W	0h	Reset by: REG_RESET	Charge status mask flag 0b = Charging status change does produce nINT 1b = Charging status change does not produce nINT
2:1	RESERVED	R	0h		Reserved
0	VBUS_MASK	R/W	0h	Reset by: REG_RESET	VBUS status mask flag 0b = VBUS status change does produce nINT 1b = VBUS status change does not produce nINT

REG0x25_FAULT_Mask_0 Register

Bit	Field	Type	Reset	Notes	Description
7	VBUS_FAULT_MASK	R/W	0h	Reset by: REG_RESET	VBUS over-voltage and sleep comparator mask flag 0b = Entering VBUS OVP or sleep does produce nINT 1b = Entering VBUS OVP or sleep does not produce nINT
6	BAT_FAULT_MASK	R/W	0h	Reset by: REG_RESET	IBAT over current and VBAT overvoltage mask flag 0b = IBAT OCP fault or VBAT OVP fault does produce nINT 1b = Neither IBAT OCP fault nor VBAT OVP fault produces nINT
5	SYS_FAULT_MASK	R/W	0h	Reset by: REG_RESET	SYS over voltage and SYS short mask 0b = System over-voltage or SYS short fault does produce nINT 1b = Neither system over voltage nor SYS short fault produces nINT

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4	OTG_FAULT_MASK	R/W	0h	Reset by: REG_RESET	OTG VBUS and PMID reverse-current, under voltage and over voltage mask 0b = OTG VBUS or PMID reverse-current, under voltage fault or over voltage fault does produce nINT 1b = Neither reverse-current fault, OTG PMID or VBUS under voltage nor over voltage fault produces nINT
3	TSHUT_MASK	R/W	0h	Reset by: REG_RESET	IC thermal shutdown mask flag 0b = TSHUT does produce nINT 1b = TSHUT does not produce nINT
2:1	RESERVED	R	0h		Reserved
0	TS_MASK	R/W	0h	Reset by: REG_RESET	Temperature charging profile interrupt mask 0b = A change to TS temperature zone does produce nINT 1b = A change to the TS temperature zone does not produce nINT

REG0x38_Part_Information Register

Bit	Field	Type	Reset	Notes	Description
7:6	RESERVED	R	0h		Reserved
5:3	PN	R	0h		Device Part number All the other options are reserved 0h = CX25601N
2:0	DEV_REV	R	2h		Device Revision

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8 Application and Implementation

8.1 Application information

A typical application consists of the device configured as an I2C controlled power path management device and a single cell battery charger for Li-Ion and Li-polymer batteries used in a wide range of smartphone and other portable devices. It integrates an input reverse-block FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET Q4) between the system and battery. The device also integrates a bootstrap diode for the high-side gate drive.

8.2 Typical Application

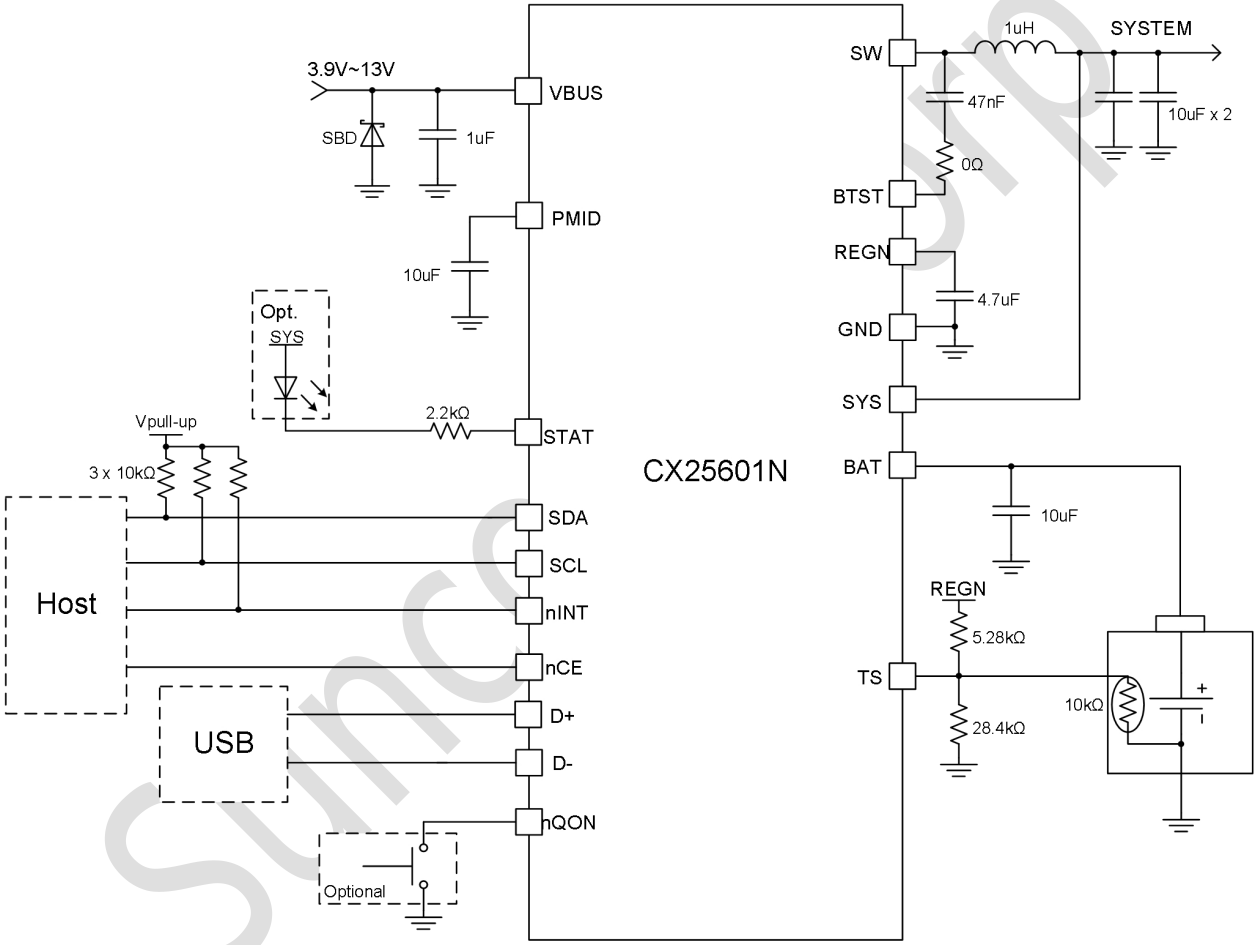


Figure 8-1. CX25601N Application Diagram

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8.2.1 Design Requirements

Table 8-1. Design Requirements

PARAMETERS	VALUES
VBUS range	3.9 -13 V
Input current limit	3000mA
Fast charge current	3040 mA
Minimum system voltage	3520 mV
Battery regulation voltage	4200 mV

8.2 2 Detailed Design Procedure

8.2.2.1 Inductor Selection

The device has 1.1 MHz switching frequency to allow the use of small inductor and capacitor value to maintain an inductor saturation current higher than the charging current (ICHG) plus half the ripple current (IRIPPLE):

$$I_{SAT} \geq I_{CHG} + (1/2)\ I_{RIPPLE} \quad (3)$$

The inductor ripple current depends on the input voltage (VVBUS), the duty cycle (D = VBAT/VVBUS), the switching frequency (fS) and the inductance (L):

$$I_{RIPPLE} = \frac{V_{BUS} \times D \times (1-D)}{fs \times L} \quad (4)$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. Usually inductor ripple is designed in the range of (20–40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design.

8.2.2.2 Input Capacitor

Input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current IPMID occurs where the duty cycle is closest to 50% and can be estimated by Equation 5:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1-D)} \quad (5)$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed as close as possible to the drain of the high-side MOSFET (PMID) and source of the low-side MOSFET (GND). Voltage rating of the capacitor must be higher than normal input voltage level. A rating of 25-V or higher capacitor is preferred for 13 V input voltage. 10-μF ceramic capacitor is suggested for typical of 3A charging current.

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8.2.2.3 Output Capacitor

Output capacitor also should have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current ICOUT is given:

$$I_{COUT} = \frac{I_{RIPPLE}}{2\times\sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (6)$$

The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_{SYS} = \frac{V_{SYS}}{8LC_{SYS}fs^2}\left(1 - \frac{V_{SYS}}{V_{VBUS}}\right) \quad (7)$$

At certain input/output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

The charger device has internal loop compensator optimized for ≥ 10-μF ceramic output capacitor. The preferred ceramic capacitor is 10-V rating, X7R or X5R.

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9 Power Supply Recommendations

In order to provide an output voltage on SYS, the device requires a power supply between 3.9 V and 13.0 V input with at least 100-mA current rating connected to VBUS or a single-cell Li-Ion battery with voltage > V BATUVLO connected to BAT.

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10 Layout

10.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see Figure 10-1) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

1. For lowest switching noise during forward/charge mode, place the decoupling capacitor CPMID1 and then bulk capacitor CPMID2 positive terminals as close as possible to PMID pin. Place the capacitor ground terminal close to the GND pin using the shortest copper trace connection or GND plane on the same layer as the IC.
2. For lowest switching noise during reverse/OTG mode, place the CSYS1 and CSYS2 output capacitors' positive terminals near the SYS pin. The capacitors' ground terminals must be via'd down through multiple vias to an all ground internal layer that returns to IC GND pin through multiple vias under the IC.
3. Since REGN powers the internal gate drivers, place the CREGN capacitor positive terminal close to REGN pin to minimize switching noise. The capacitor's ground terminal must be via'd down through multiple vias to an all ground internal layer that returns to IC GND pin through multiple vias under the IC.
4. Place the CVBUS and CBAT capacitors positive terminals as close to the VBUS and BAT pins as possible. The capacitors' ground terminals must be via'd down through multiple vias to an all ground internal layer that returns to IC GND pin through multiple vias under the IC.
5. Place the inductor input pin near the positive terminal of the SYS pin capacitors. Due to the PMID capacitor placement requirements, the inductor's switching node terminal must be via'd down with multiple via's to a second internal layer with a wide trace that returns to the SW pin with multiple vias. Using multiple vias ensures that the via's additional resistance is negligible compared to the inductor's dc resistance and therefore does not impact efficiency. The vias additional series inductance is negligible compared to the inductor's inductance.
6. Place the BTST capacitor on the opposite side from the IC using vias to connect to the BTST pin and SW node.
7. A separate analog GND plane for non-power related resistors and capacitors is not required if those components are placed away from the power components traces and planes.
8. Ensure that the I2C SDA and SCL lines are routed away from the SW node.

Additionally, it is important that the PCB footprint and solder mask for the CX25601N cover the entire length of each of the pins. GND, SW, PMID, SYS and BAT pins extend further into the package than the other pins. Using the entire length of these pins reduces parasitic resistance and increases thermal conductivity from the package into the board.

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10.2 Layout Example

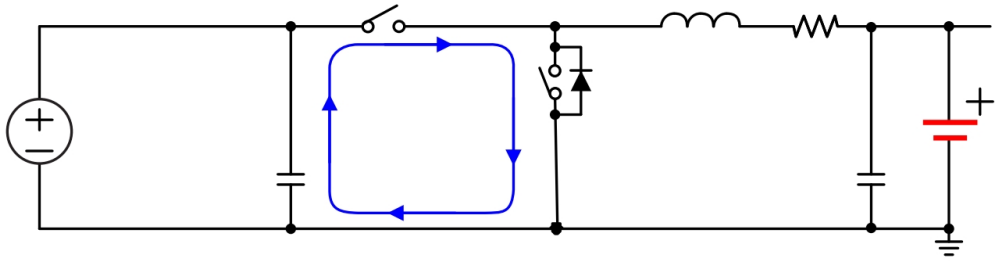
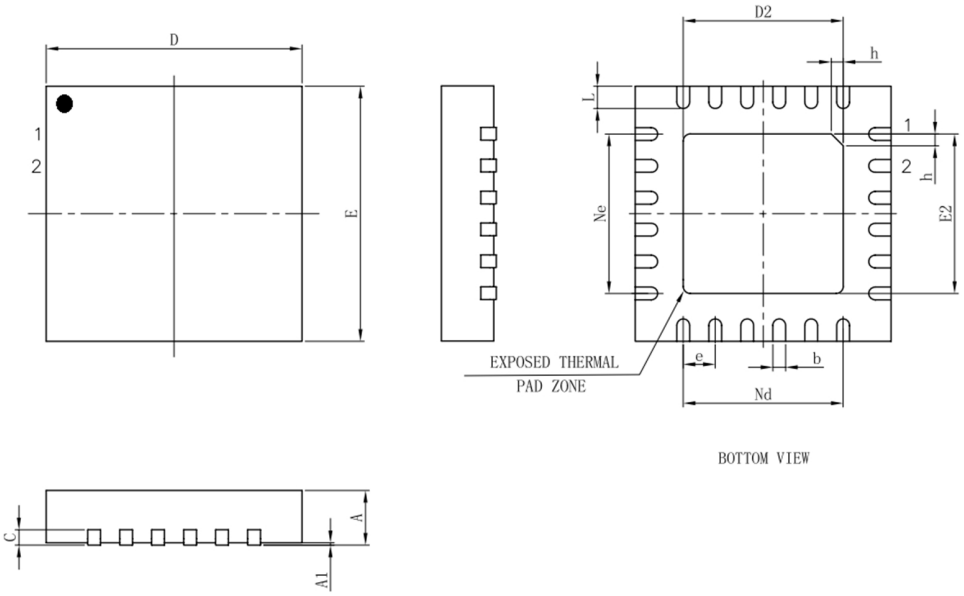


Figure 10-1. High Frequency Current Path

PACKAGE OUTLINE DIMENSIONS



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.60	2.70	2.80
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.60	2.70	2.80
L	0.35	0.40	0.45
h	0.30	0.35	0.40

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