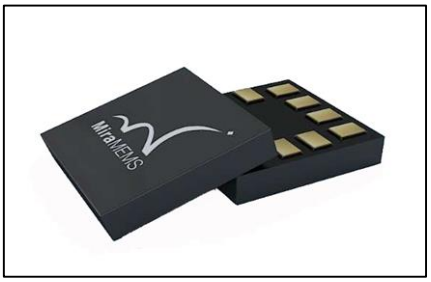
da217

MEMS digital output motion sensor

Ultra-low-power high performance 3-axes “DSC-XYZ” accelerometer



Key Features

- Supply voltage, 1.62V to 3.6V
- For 2x2x0.9 mm LGA-12 package
- User selectable range, ±2g, ±4g, ±8g, ±16g
- User selectable data output rate
- Digital I^2C/SPI output interface
- 14 bit resolution
- Ultra-low power consumption
- Embedded 32-level FIFO
- Internal step counter
- 2 Programmable interrupt generators with independent function for motion detection
- Factory programmable offset and sensitivity
- RoHS compliant

Applications

- User interface for mobile phone and PMP
- Display orientation
- Gesture recognition
- Active monitoring
- Free-fall detection
- Double/single Click recognition
- Power management
- Vibration monitoring
- Step counter
- Tilt
- Significant motion

Product Overview

The da217 sensor is ultra-low power high performance capacitive three-axis linear accelerometer developed by micro-machined technology. The device is available in a 2x2x0.9mm land grid array (LGA) and it is guaranteed to operate over an extended temperature range from -40 ℃ to +85 ℃.

The sensor element is fabricated by single crystal silicon with DRIE process and is protected by hermetically sealed silicon cap from the environment.

The device features user selectable full scale of ±2g/ ±4g/ ±8g/ ±16g measurement range with data output rate from 1Hz to 500Hz with signal condition, temperature compensation, motion detection, step counter and step detection along with significant motion detection embedded.

The da217 has an integrated 32-level first-in, first-out (FIFO) buffer allowing the user to store data in order to limit intervention by the host processor.

Two independent and flexible interrupts provided greatly simplify the algorithm for various motion status detections. Standard I^2C and SPI interfaces are used to communicate with the chip.

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Content

1. Block diagram and pin description 9
   1.1. Block diagram 9
   1.2. Pin description 9
2. Mechanical and electrical specifications 11
   2.1. Mechanical characteristics 11
   2.2. Electrical characteristics 12
   2.3. Absolute maximum ratings 12
3. Communication interface 13
   3.1. Communication interface Electrical specification 13
      3.1.1. SPI Electrical specification 13
      3.1.2. I2C Electrical specification 14
   3.2. Digital interface operation 15
      3.2.1. SPI Operation 15
      3.2.2. I2C Operation 16
4. Terminology and functionality 18
   4.1. Terminology 18
      4.1.1. Sensitivity 18
      4.1.2. Zero-*g* level 18
   4.2. Functionality 18
      4.2.1. Power mode 18
      4.2.2. Sensor data 19
      4.2.3. Factory calibration 19
   4.3. Interrupt controller 20
      4.3.1. General features 20
      4.3.2. Mapping 21
      4.3.3. Electrical behavior (INT1/INT2 to open-drive or push-pull) 21
      4.3.4. New data interrupt 21
      4.3.5. Active detection 21
      4.3.6. Tap detection 22
      4.3.7. Orientation recognition 23
      4.3.8. Freefall interrupt 25
5. Digital blocks 26
   5.1. FIFO 26
      5.1.1. Bypass Mode 26
      5.1.2. FIFO Mode 26
      5.1.3. Stream Mode 26
      5.1.3. Trigger Mode 26
      5.1.4 Retrieving Data from FIFO 26
   5.2. Embedded functions 27
      5.2.1. Step counter 27
      5.2.2. Step detector 27

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5.2.3. Significant motion 27
5.2.4. Tilt 27
6. Application hints 28
7. Register mapping 29
8. Registers description 31
8.1. SPI_CONFIG (00H) 31
8.2. CHIP_ID (01H) 31
8.3. ACC_X_LSB (02H), ACC_X_MSB (03H) 31
8.4. ACC_Y_LSB (04H), ACC_Y_MSB (05H) 31
8.5. ACC_Z_LSB (06H), ACC_Z_MSB (07H) 32
8.6. FIFO_STATUS (08H) 32
8.7. MOTION_FLAG (09H) 33
8.8. NEWDATA_FLAG (0AH) 33
8.9. TAP_ACTIVE_STATUS (0BH) 34
8.10. ORIENT_STATUS (0CH) 35
8.11. STEPS_MSB (0DH), STEPS_LSB (0EH) 35
8.12. RESOLUTION_RANGE (0FH) 36
8.13. ODR_AXIS (10H) 37
8.14. MODE_BW (11H) 38
8.15. SWAP_POLARITY (12H) 38
8.16. FIFO_CTRL (14H) 39
8.17. INT_SET0 (15H) 39
8.18. INT_SET1 (16H) 40
8.19. INT_SET2 (17H) 40
8.20. INT_MAP1 (19H) 41
8.21. INT_MAP2 (1AH) 41
8.22. INT_MAP3 (1BH) 42
8.23. INT_CONFIG (20H) 42
8.24. INT_LATCH (21H) 43
8.25. FREEFALL_DUR (22H) 44
8.26. FREEFALL_THS (23H) 44
8.27. FREEFALL_HYST (24H) 44
8.28. ACTIVE_DUR (27H) 45
8.29. ACTIVE_THS (28H) 45
8.30. TAP_DUR (2AH) 46
8.31. TAP_THS (2BH) 46
8.32. ORIENT_HYST (2CH) 47
8.33. Z_BLOCK (2DH) 47
8.34. RESET_STEP (2EH) 47
8.35. STEP_FILTER (33H) 48
8.36. SM_THRESHOLD (34H) 48
9. Package information 49
9.1. Outline dimensions 49
9.2. Landing pattern recommendation 50

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9.3. Tape and reel specification 51
10. Reliability 52
11. Revision history 53

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List of tables

Table 1.Pin description 10
Table 2.Mechanical characteristic 11
Table 3.Electrical characteristics 12
Table 4.Absolute maximum ratings 12
Table 5.Electrical specification of the SPI interface pins 13
Table 6.Electrical specification of the I2C interface pins 14
Table 7.Mapping of the interface pins 15
Table 8.W1 and W0 settings 15
Table 9.I2C Address 16
Table 10.SAD+Read/Write patterns 16
Table 11.Transfer when master is writing one byte to slave 17
Table 12.Transfer when master is writing multiple bytes to slave 17
Table 13.Transfer when master is receiving (reading) one byte of data from slave 17
Table 14.Transfer when master is receiving (reading) multiple bytes of data from slave 17
Table 15.Interrupt mode selection 20
Table 16.meaning of 'orient' bits in symmetric mode 24
Table 17.meaning of 'orient' bits in high-asymmetric mode 24
Table 18.meaning of 'orient' bits in low-asymmetric mode 24
Table 19.blocking conditions for orientation recognition 24
Table 20.Register address map 29
Table 21.SPI_CONFIG register 31
Table 22.SPI_CONFIG description 31
Table 23.CHIP_ID register 31
Table 24.ACC_X_LSB register 31
Table 25.ACC_X_MSB register 31
Table 26.ACC_Y_LSB register 32
Table 27.ACC_Y_MSB register 32
Table 28.ACC_Z_LSB register 32
Table 29.ACC_Z_MSB register 32
Table 30.FIFO_STATUS register 32
Table 31.MOTION_FLAG register description 32
Table 32.MOTION_FLAG register 33
Table 33.MOTION_FLAG register description 33
Table 34.NEWDATA_FLAG register 33
Table 35.NEWDATA_FLAG register description 33
Table 36.TAP_ACTIVE_STATUS register 34
Table 37.TAP_ACTIVE_STATUS register description 34
Table 38.ORIENT_STATUS register 35
Table 39.ORIENT_STATUS register description 35
Table 40.STEPS_MSB register 35
Table 41.STEPS_LSB register 35
Table 42.RESOLUTION_RANGE register 36

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Table 43.RESOLUTION_RANGE register description....36
Table 44.ODR_AXIS register....37
Table 45.ODR_AXIS register description....37
Table 46.MODE_BW register....38
Table 47.MODE_BW register description....38
Table 48.SWAP_POLARITY register....38
Table 49.SWAP_POLARITY register description....38
Table 50.FIFO_CTRL register....39
Table 51.FIFO_CTRL register description....39
Table 52.INT_SET0 register....39
Table 53.INT_SET01 register description....39
Table 54.INT_SET1 register....40
Table 55.INT_SET1 register description....40
Table 56.INT_SET2 register....40
Table 57.INT_SET2 register description....40
Table 58.INT_MAP1 register....41
Table 59.INT_MAP1 register description....41
Table 60.INT_MAP2 register....41
Table 61.INT_MAP2 register description....41
Table 62.INT_MAP3 register....42
Table 63.INT_MAP3 register description....42
Table 64.INT_CONFIG register....42
Table 65.INT_CONFIG register description....42
Table 66.INT_LATCH register....43
Table 67.INT_LATCH register description....43
Table 68.FREEFALL_DUR register....44
Table 69.FREEFALL_DUR register description....44
Table 70.FREEFALL_THS register....44
Table 71.FREEFALL_THS register description....44
Table 72.FREEFALL_HYST register....44
Table 73.FREEFALL_HYST register description....44
Table 74.ACTIVE_DUR register....45
Table 75.ACTIVE_DUR register description....45
Table 76.ACTIVE_THS register....45
Table 77.ACTIVE_THS register description....45
Table 78.TAP_DUR register....46
Table 79.TAP_DUR register description....46
Table 80.TAP_THS register....46
Table 81.TAP_THS register description....46
Table 82.ORIENT_HYST register....47
Table 83.ORIENT_HYST register description....47
Table 84.Z_BLOCK register....47
Table 85.Z_BLOCK register description....47
Table 86.RESET_STEP register....47

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Table 87.Z_BLOCK register description....47
Table 88.STEP_FILTER register....48
Table 89.STEP_CONFIG4 register description....48
Table 90.SM_THRESHOLD register....48
Table 91.SM_THRESHOLD register description....48
Table 92.Accelerated Life Tests....52
Table 93.Component Level Tests....52
Table 94.Document revision history....53

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List of figures

Figure 1 Block Diagram 9
Figure 2 Pin description 9
Figure 3 SPI slave timing diagram 13
Figure 4 I2C Slave timing diagram 14
Figure 5 Instruction Phase Bit Field 15
Figure 6 MSB First and LSB First Instruction and Data Phases 16
Figure 7 I2C Protocol 17
Figure 8 power mode 18
Figure 9 Interrupt mode 21
Figure 10 Timing of tap detection 22
Figure 11 Definition of vector components 23
Figure 12 da217 I2C electrical connect 28
Figure 13 da217 SPI electrical connect 28
Figure 14 12Pin LGA Mechanical data and package dimensions 49
Figure 15 landing patterns; dimensions in mm 50
Figure 16 Tape and reel dimension in mm 51

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1. Block diagram and pin description

1.1. Block diagram

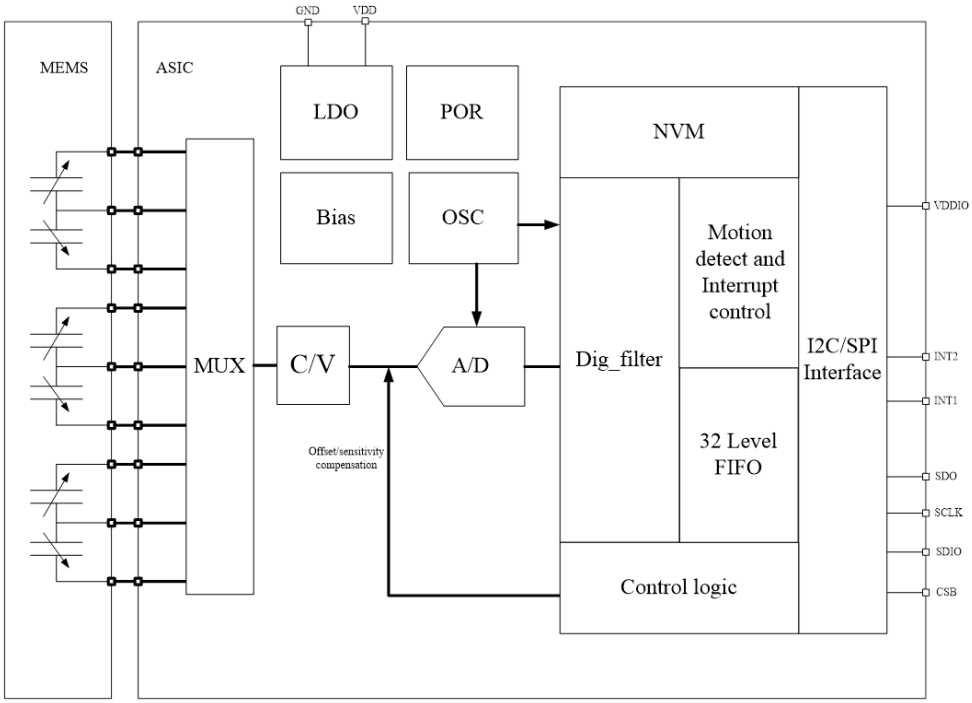


Figure 1 Block Diagram

1.2. Pin description

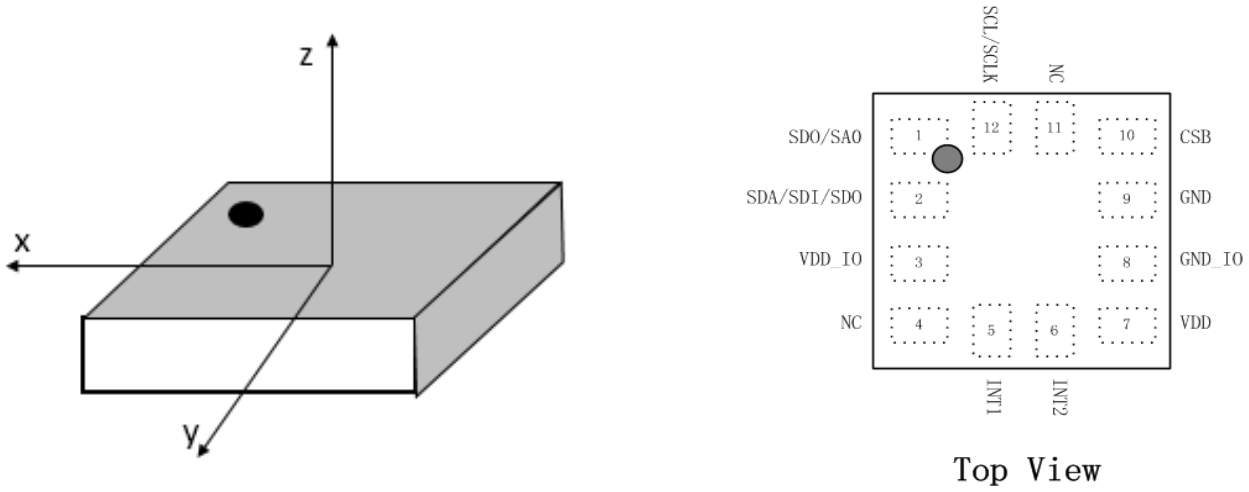


Figure 2 Pin description

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Table 1.Pin description

Pin#	Name	I/O Type	Function
1	SDO SA0	Digital out Digital in	SPI(4-wire mode) serial data output (SDO) I2C less significant bit of the device address (SA0) When using the I2C communication, SA0 pin must be connected to VDDIO or GND
2	SDA SDI SDO	Digital in/out	I2C serial data input/output(SDA) SPI(4-wire mode) serial data input (SDI) 3-wire interface serial data input/output (SDO)
3	VDD_IO	Supply	Power supply for I/O pins
4	NC	--	Not connected
5	INT1	Digital out	Interrupt pin1
6	INT2	Digital out	Interrupt pin2
7	VDD	Supply	Power supply
8	GND_IO	Ground	Ground supply for I/O pins
9	GND	Ground	Ground supply
10	CSB	Digital in	Chip select for SPI When using the I2C communication, CSB pin must be connected to VDDIO
11	NC	--	Not connected
12	SCL SCLK	Digital in	I2C serial clock (SCL) SPI serial clock (SCLK)

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2. Mechanical and electrical specifications

2.1. Mechanical characteristics

VDD = 2.5 V, T = 25 ℃ unless otherwise noted.

Table 2.Mechanical characteristic

Symbol	Parameter	Test conditions	Min	Type	Max	Unit
FS	Measurement range	FS bit set to 00		±2		g
		FS bit set to 01		±4		g
		FS bit set to 10		±8		g
		FS bit set to 11		±16		g
So	Sensitivity	FS bit set to 00		4096		LSB/g
		FS bit set to 01		2048		LSB/g
		FS bit set to 10		1024		LSB/g
		FS bit set to 11		512		LSB/g
TCSo	Sensitivity change vs. temperature	FS bit set to 00		±0.01		%/℃
Tyoff	Typical zero-g level offset accuracy			±70		mg
Tcoff	Zero-g level change vs. temperature	Max delta from 25℃		±0.6		mg/℃
Noise	XYZ RMS noise	FS bit set to 00, normal mode，BW = 100Hz		1		mg
Top	Operation temperature range		-40		85	℃

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2.2. Electrical characteristics

Vdd = 2.5 V, T = 25 ℃ unless otherwise noted

Table 3.Electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
VDD	Supply voltage		1.62	2.5	3.6	V
VDD_IO	I/O Pins supply voltage		1.62		VDD	V
IDD	current consumption in normal mode	Top=25℃, ODR=125Hz,		95		uA
IDD_SM	current consumption in suspend mode	Top=25℃		1		uA
VIH	Digital high level input voltage	SPI&I2C	0.7*Vdd_IO			V
VIL	Digital low level input voltage	SPI&I2C			0.3*Vdd_IO	V
VOH	high level output voltage		0.9*Vdd_IO			V
VOL	Low level output voltage				0.1*Vdd_IO	V
BW	System bandwidth		100		500	Hz
ODR	Output data rate		1		500	Hz
TWU	Wake-up time	From stand-by		1		ms
TSU	Start-up time	From power off		3		ms
PSRR	Power Supply Rejection Rate	Top=25℃			20	mg/V

2.3. Absolute maximum ratings

Stresses below those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 4.Absolute maximum ratings

Parameter	Test conditions	Min	Max	Unit
Storage Temperature		-45	125	℃
Supply Voltage VDD	Supply pins	-0.3	4.25	V
Supply Voltage VDD_IO	Logic pins	-0.3	Vdd_IO+0.3	V
ESD Rating	HMB,R=1.5k,C=100pF		±2	kV
Mechanical Shock	Duration<200us		10,000	g

Note: *Supply voltage on any pin should never exceed 4.25V*


This is a mechanical shock sensitive device, improper handling can cause permanent damages to the part.


This is an ESD sensitive device, improper handling can cause permanent damages to the part.

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3. Communication interface

3.1. Communication interface Electrical specification

3.1.1. SPI Electrical specification

Table 5.Electrical specification of the SPI interface pins

Symbol	Parameter	Condition	Min	Max	Unit
fsclk	Clock frequency	Max load on SDIO or SDO = 25pF		10	MHz
t_{SCKL}	SLCK low pulse		20		
t_{SCKH}	SLCK high pulse		20		
t_{SDI_setup}	SDI setup time		20		ns
t_{SDI_hold}	SDI hold time		20		ns
t_{SDO_OD}	SDO/SDI output delay	Load = 25pF		30	ns
		Load = 250pF		40	ns
t_{CSB_setup}	CSB setup time		20		ns
t_{CSB_hold}	CSB hold time		40		ns

The figure below shows the definition of the SPI timing given in the above table:

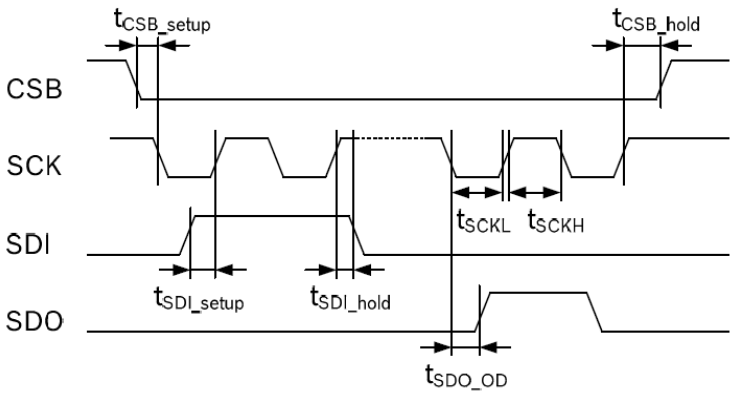


Figure 3 SPI slave timing diagram

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3.1.2.I2C Electrical specification

Table 6.Electrical specification of the I2C interface pins

Symbol	Parameter	Min	Max	Unit
fscl	Clock frequency		400	kHz
t_{LOW}	SCL low pulse	1.3		us
t_{HIGH}	SCL high pulse	0.6		us
t_{SUDAT}	SDA setup time	0.1		us
t_{HDDAT}	SDA hold time	0.0		us
t_{SUSTA}	Setup Time for a repeated start condition	0.6		us
t_{HDSTA}	Hold time for a start condition	0.6		us
t_{SUSTO}	Setup Time for a stop condition	0.6		us
t_{BUF}	Time before a new transmission can start	1.3		us

The figure below shows the definition of the I2C timing given in the above table:

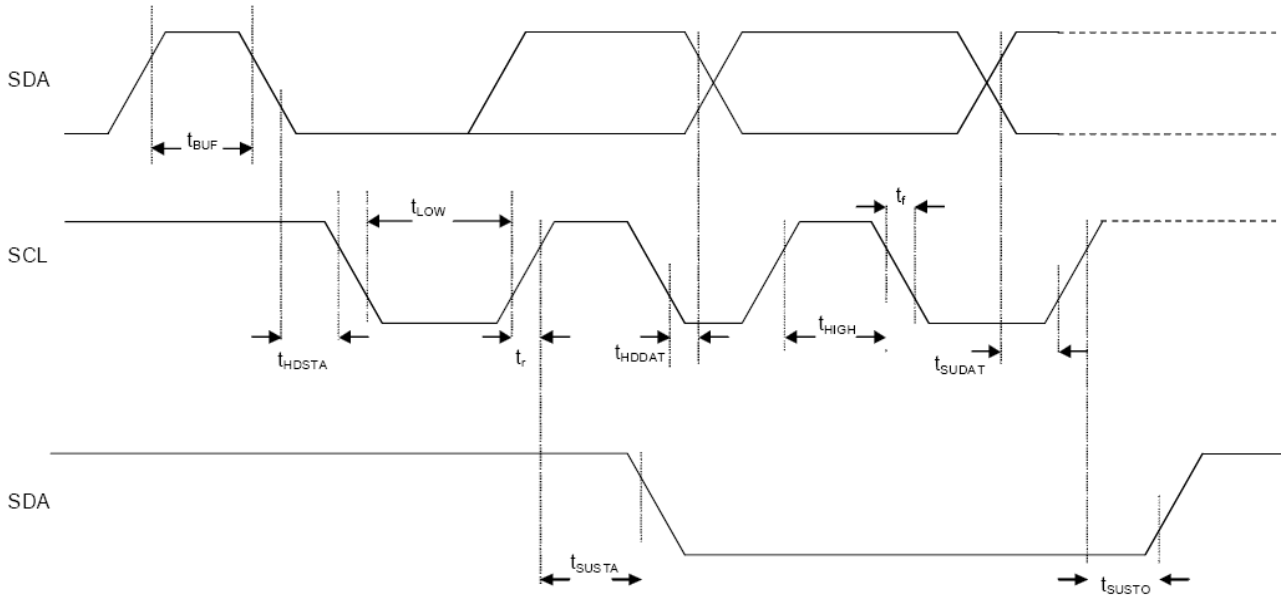


Figure 4 I2C Slave timing diagram

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3.2. Digital interface operation

The da217 supports two serial digital interface protocols for communications as slave with a host device: SPI and I2C. The active interface is selected by the state of the pin CS, 0 selects SPI and 1 selects I2C. By default, SPI operates in 3-wire mode and it can be re-configured by writing 1 to bit 'SDO_active' to work in 4-wire mode. Both interfaces share the same pins. The mapping for each interface is given in the following table:

Table 7.Mapping of the interface pins

PIN name	I2C	SPI
SCL/SCLK	Serial clock	Serial clock
SDA/SDI	Serial Data	Data input (4-wire mode). Data input/output (3-wire mode)
SA0/SDO	Used to set LSB of I2C address	Data output (4-wire mode)
CSB	Unused	Chip select

3.2.1.SPI Operation

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of framing. Once the beginning of the frame has been determined, timing is straightforward. The first phase of the transfer is the instruction phase, which consists of 16 bits followed by data that can be of variable lengths in multiples of 8 bits. If the device is configured with CSB tied low, framing begins with the first rising edge of SCLK.

The instruction phase is the first 16 bits transmitted. As shown in the following figure, the instruction phase is divided into a number of bit fields.

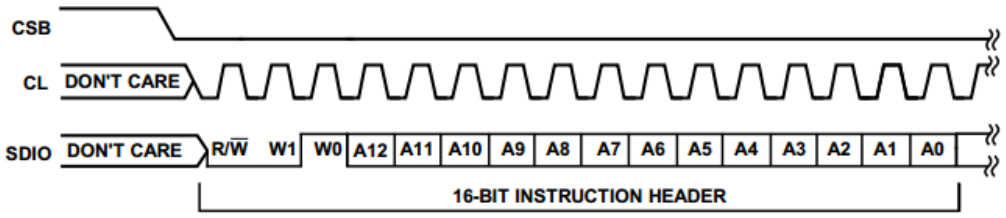


Figure 5 Instruction Phase Bit Field

The first bit in the stream is the read/write indicator bit (R/W). When this bit is high, a read is being requested, otherwise indicates it is a write operation.

W1 and W0 represent the number of data bytes to transfer for either read or write as shown in the following table (W1 and W0 setting table). If the number of bytes to transfer is three or less (00, 01, or 10), CSB can stall high on byte boundaries. Stalling on a non-byte boundary terminates the communications cycle. If these bits are 11, data can be transferred until CSB transitions high. CSB is not allowed to stall during the streaming process.

The remaining 13 bits represent the starting address of the data sent. If more than one word is being sent, sequential addressing is used, starting with the one specified, and it either increments (LSB first) or decrements (MSB first) based on the mode setting.

Table 8.W1 and W0 settings

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W1:W0	Action	CSB stalling
00	1 byte of data can be transferred.	Optional
01	2 bytes of data can be transferred.	Optional
10	3 bytes of data can be transferred.	Optional
11	4 or more bytes of data can be transferred. CSB must be held low for entire sequence; otherwise, the cycle is terminated.	No

Data follows the instruction phase. The amount of data sent is determined by the word length (Bit W0 and Bit W1). This can be one or more bytes of data. All data is composed of 8-bit words.

Data can be sent in either MSB-first mode or LSB-first mode (by setting 'LSB_first' bit). On power up, MSB-first mode is the default. This can be changed by programming the configuration register. In MSB-first mode, the serial exchange starts with the highest-order bit and ends with the LSB. In LSB-first mode, the order is reversed. The detail is shown in the below figure.

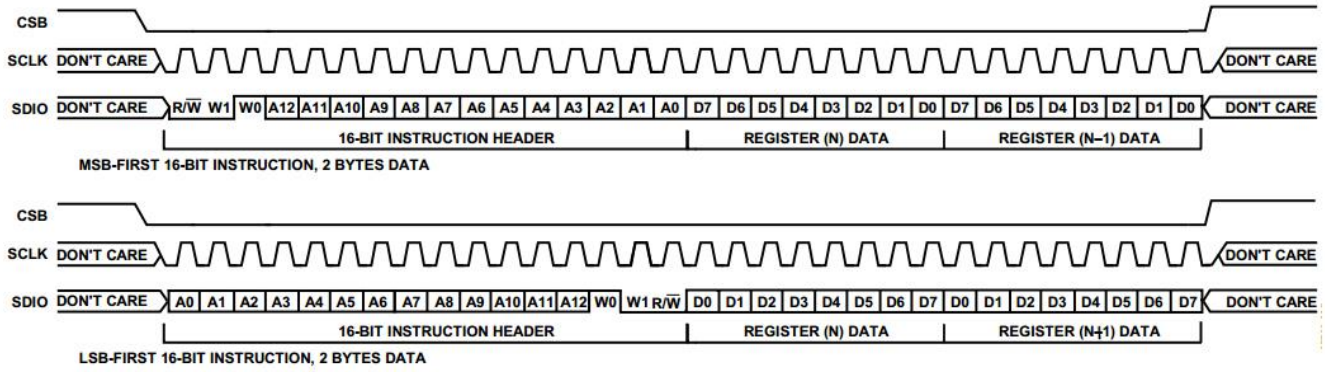


Figure 6 MSB First and LSB First Instruction and Data Phases

Register bit 'SDO_active' is responsible for activating SDO on devices. If this bit is cleared, then SDO is inactive and read data is routed to the SDI pin. If this bit is set, read data is placed on the SDO pin. The default for this bit is low, making SDO inactive.

3.2.2.I2C Operation

I2C bus uses SCL and SDA as signal lines. Both lines are connected to VDDIO externally via pull-up resistors so that they are pulled high when the bus is free. The I2C device address of da217 is shown below. The LSB bit of the 7bits device address is configured via SA0 pin.

Table 9.I2C Address

SAD6	SAD5	SAD4	SAD3	SAD2	SAD1	SAD0	W/R
0	1	0	0	1	1	SA0	0/1

Table 10.SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0]=SA0	R/W	SAD+R/W
Read	010011	0	1	01001101(4dh)
Write	010011	0	0	01001100(4ch)
Read	010011	1	1	01001111(4fh)
Write	010011	1	0	01001110(4eh)

The I2C interface protocol has special bus signal conditions. Start (S), stop (P) and binary data conditions are shown below. At start condition,

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SCL is high and SDA has a falling edge. Then the slave address is sent. After the 7 address bits, the direction control bit R/W selects the read or write operation. When a slave device recognizes that it is being addressed, it should acknowledge by pulling SDA low in the ninth SCL (ACK) cycle.

At stop condition, SCL is also high, but SDA has a rising edge. Data must be held stable at SDA when SCL is high. Data can change value at SDA only when SCL is low.

In order to prevent the I2C slave of the device to lock-up the I2C bus, a watchdog timer (WDT) is implemented. The WDT observes internal I2C signals and resets the I2C interface if the bus is locked-up by the sensor. The activity and the timer period of the WDT can be configured trough the bits “wdt_en” and “wdt_time” of “RESOLUTION_RANGE” (0fH) register.

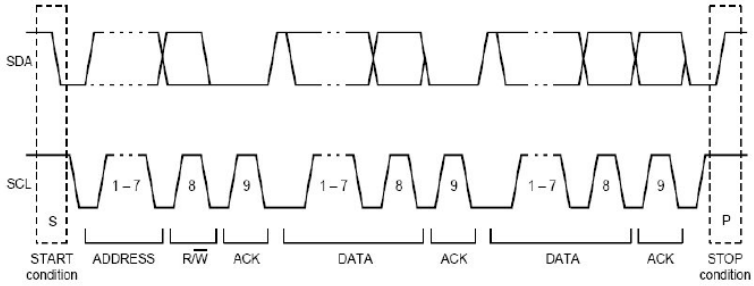


Figure 7 I2C Protocol

Table 11.Transfer when master is writing one byte to slave

Master	S	SAD+W		SUB		DATA		P
Slave			SAK		SAK		SAK	

Table 12.Transfer when master is writing multiple bytes to slave

Master	S	SAD+W		SUB		DATA		DATA		P
Slave			SAK		SAK		SAK		SAK	

Table 13.Transfer when master is receiving (reading) one byte of data from slave

Master	S	SAD+W		SUB		SR	SAD+R			NMASK	P
Slave			SAK		SAK			SAK	DATA		

Table 14.Transfer when master is receiving (reading) multiple bytes of data from slave

Master	S	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMASK	P
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Note：

Symbol	Symbol explain	Symbol	Symbol explain
SAD	slave address	SAK	slave acknowledge
W	write	MAK	master acknowledge
R	read	NMASK	no master acknowledge
S	start	SUB	Sub-address(register address)
P	stop	DATA	Read or write data
SR	start		

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4. Terminology and functionality

4.1. Terminology

4.1.1. Sensitivity

Sensitivity describes the gain of the sensor and can be determined e.g. by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtract the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and also time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

4.1.2. Zero-*g* level

Zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface measure 0 *g* in X axis and 0 *g* in Y axis whereas the Z axis measure 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of output data registers are 00h, data expressed as 2's complement number). A deviation from ideal value in this case is called Zero-*g* offset. Offset is to some extent a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature; see "Zero-*g* level change vs. temperature". The Zero-*g* level tolerance (TyOff) describes the standard deviation of the range of Zero-*g* levels of a population of sensors.

4.2. Functionality

4.2.1. Power mode

The da217 has two different power modes: normal and suspend mode.

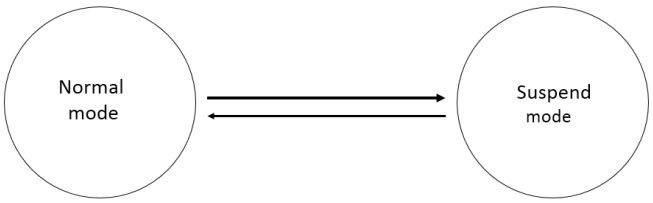


Figure 8 power mode

In the normal mode, the device is periodically switching between a sleep phase and a wake-up phase. The wake-up phase essentially corresponding to operation in measure state with complete power-up of the circuitry at the current setting ODR when "autosleep_en"bit of "MODE_BW" (11H) register is set to 0, but "autosleep_en"bit is set to 1, the measure state works at 12.5hz in inactive state and auto switched to operation mode during active state. During the sleep phase the analog part except the oscillator is powered down.

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During the wake-up phase, if an enabled interrupt is detected, the device stays in the wake-up phase as long as the interrupt condition endures (non-latched interrupt), or until the latch time expires (temporary latched interrupt), or until the interrupt is reset (latched interrupt). If no interrupt detected, the device enters the sleep phase.

Suspend mode: power-down mode, which is only support I2C and SPI interface.

4.2.2.Sensor data

The width of acceleration data is 14bits given in two's complement representation. The 14bits for each axis are split into an MSB part (one byte containing bits 13 to 6) and an LSB lower part (one byte containing bits 5 to 0)

4.2.3.Factory calibration

The IC is factory calibrated for sensitivity (So) and Zero-*g* level (TyOff). The trimming values are stored inside the chip's nonvolatile memory. The trimming parameters are loaded to registers while da217 reset (POR or software reset). This allows using the device without further calibration.

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4.3. Interrupt controller

Interrupt engines are integrated in the da217. Each interrupt can be independently enabled and configured. If the condition of an enabled interrupt is fulfilled, the corresponding status bit is set to 1 and the selected interrupt pin is activated. There are two interrupt pins, INT1 and INT2; interrupts can be freely mapped to any of these two pins. The pin state is a logic 'or' combination of all mapped interrupts.

4.3.1. General features

An interrupt is cleared depending on the selected interrupt mode, which is common to all interrupts. There are three different interrupt modes: non-latched, latched and temporary. The mode is selected by the 'latch_int' bits according to the following table.

Table 15.Interrupt mode selection

latch_int1/2	Interrupt mode
0000	non-latched
0001	temporary latched 250ms
0010	temporary latched 500ms
0011	temporary latched 1s
0100	temporary latched 2s
0101	temporary latched 4s
0110	temporary latched 8s
0111	latched
1000	non-latched
1001	temporary latched 1ms
1010	temporary latched 1ms
1011	temporary latched 2ms
1100	temporary latched 25ms
1101	temporary latched 50ms
1110	temporary latched 100ms
1111	latched

An interrupt is generated if its activation condition is met. It can't be cleared as long as the activation condition is fulfilled. In the non-latched mode the interrupt status bit and the selected pin (INT1 or INT2) are cleared as soon as the activation condition is no more valid. Exceptions to this behavior are the new data and orientation, which are automatically reset after a fixed time.

In the latched mode an asserted interrupt status and the selected pin are cleared by writing 1 to (0x20) 'reset_int' bit. If the activation condition still holds when it is cleared, the interrupt status is asserted again with the next change of the acceleration registers.

In the temporary mode an asserted interrupt and selected pin are cleared after a defined period of time. The behavior of the different interrupt modes is shown in the following figure.

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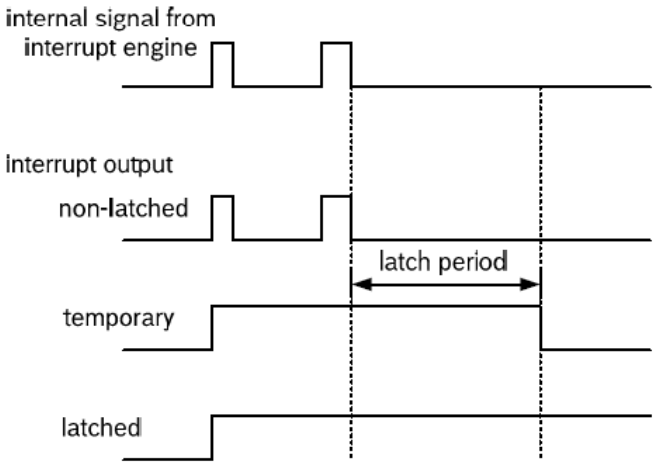


Figure 9 Interrupt mode

4.3.2.Mapping

The mapping of interrupts to the interrupt pins is done by registers 'INT_MAP' (0x19 0x1a and 0x1b), setting *int1_inttype* (e.g. int1_freefall) to 1 can map this type of interrupt to INT1 pin and setting int2_inttyp to 1 can map this type interrupt to INT2 pin.

4.3.3.Electrical behavior (INT1/INT2 to open-drive or push-pull)

Both interrupt pins can be configured to show desired electrical behavior. The active level for each pin is set by register bit int1_lvl (int2_lvl), if int1_lvl (int2_lvl) = 0 (1), then the pin INT1 (INT2) is 0 (1) active.
Also the electric type of the interrupt pin can be selected. By setting int1_od (int2_od) = 1 (0), the interrupt pin output type can be set to be open-drive (push-pull).

4.3.4.New data interrupt

This interrupt serves for synchronous reading of acceleration data. It is generated after an acceleration data was calculated. The interrupt is cleared automatically before the next acceleration data is ready.

4.3.5.Active detection

Active detection uses the slope between successive acceleration signals to detect changes in motion. An interrupt is generated when the slope (absolute value of acceleration difference) exceeds a preset threshold. The threshold is set with the value of 28H register with the LSB corresponding to 255LSB of acceleration data that is 3.9mg in 2g-range, 7.8mg in 4g-range, 15.6mg in 8g-range and 31.3mg in 16g-range. And the maximum value is 1g in 2g-range, 2g in 4g-range, 4g in 8g-range and 8g in 16g-range.

The time difference between the successive acceleration signals depends is fixed to (1/ODR) ms.
Active detection can be enabled (disabled) for each axis separately by writing '1' to bits 'active_int_en_x/y/z'. The active interrupt is generated if the slope of any of the enabled axes exceeds the threshold for ['active_dur'+1] consecutive times. As soon as the slopes of all

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enabled axes fall below this threshold for [‘active_dur’+1] consecutive times, the interrupt is cleared unless the interrupt signal is latched.

The interrupt status is stored in the (0x09) ‘active_int’ bit. The (0x0b) bit ‘active_first_x/y/z’ records which axis triggered the active interrupt first and the sign of this acceleration data that triggered the interrupt is recorded in the (0x0b) bit ‘active_sign’.

4.3.6.Tap detection

Tap detection has a functional similarity with a common laptop touch-pad or clicking keys of a computer mouse. A tap event is detected if a pre-defined pattern of the acceleration slope is fulfilled at least for one axis. Two different tap events are distinguished: A single tap is a single event within a certain time, followed by a certain quiet time. A double tap consist a first such event followed by a second event within a defined time.

Single tap interrupt is enabled by writing 1 to the (0x16) ‘s_tap_int_en’ bit and double tap interrupt is enabled by writing 1 to the (0x16) ‘d_tap_int_en’ bit. The status of the single tap interrupt is stored in the (0x09) ‘s_tap_int’ bit and the status of the double tap interrupt is stored in the (0x09) ‘d_tap_int’ bit.

The slope threshold for detecting a tap event is set by the (0x2b) “tap_th” bits with the LSB corresponding to 31LSB of acceleration data that is 62.5mg in 2g-range, 125mg in 4g-range, 250mg in 8g-range, 500mg in 16g-range. And the maximum value equals to the full scale in each range.

The following figure meaning of different timing parameter is visualized.

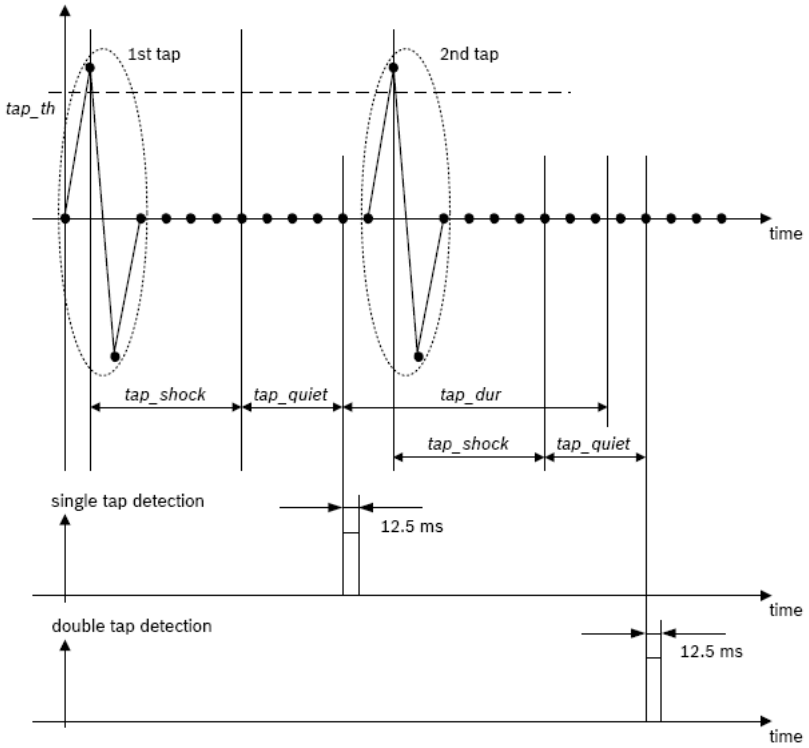


Figure 10 Timing of tap detection

The parameter ‘tap_shock’ and ‘tap_quiet’ apply to both single and double tap detection, while ‘tap_dur’ applies to double detection only. Within the duration of ‘tap_shock’ any slope exceeding ‘tap_th’ after the first event is ignored, within the duration of ‘tap_quiet’ there must

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be no slope exceeding ‘tap_th’, otherwise the first event will be cancelled.
A single tap is detected and the single tap interrupt is generated after the combination durations of ‘tap_shock’ and ‘tap_quiet’, if the corresponding slope conditions are fulfilled. The interrupt is cleared after a delay of 12.5ms in non-latched mode.

A double tap is detected and the double tap interrupt is generated if an event fulfilling the conditions for a single tap occurs within the set duration in ‘tap_dur’ after the completion of the first tap event. The interrupt is cleared after a delay in non-latched mode.

The sign of the slope of the first tap which triggered the interrupt is stored in the (0x0b) ‘tap_sign’ bit (0 means positive, 1 means negative). The axis which triggered the interrupt is indicated by the (0x0b) ‘tap_first_x/y/z’ bit.

Note: ‘tap_shock’ ‘tap_quiet’ ‘tap_dur’ ‘tap_th’ can be set by modifying register 0x2a and 0x2b

4.3.7.Orientation recognition

The orientation recognition feature informs on an orientation change of sensor with respect to the gravitation field vector ‘g’. The measured acceleration vector components with respect to the gravitation field are defined as shown in the following figure.

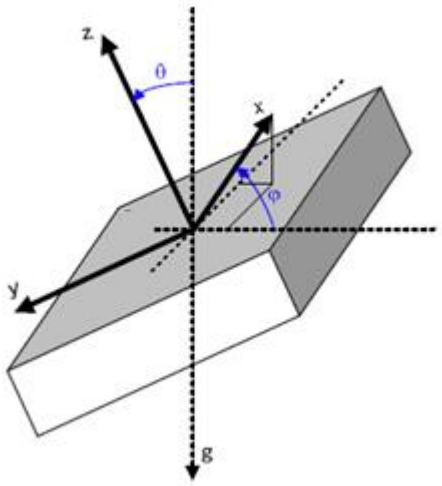


Figure 11 Definition of vector components

Therefore, the magnitudes of the acceleration vectors are calculated as follows:

$$acc_x = 1g.\sin\theta\cdot\cos\varphi$$
$$acc_y = -1g.\sin\theta\cdot\sin\varphi$$
$$acc_z = 1g\cdot\cos\theta$$

Depending on the magnitudes of the acceleration vectors the orientation of the device in the space is determined and stored in the (0x09) ‘orient_int’ bit. There are three orientation calculation modes with different thresholds for switching between different orientations: symmetrical, high-asymmetrical and low-asymmetrical. The mode is selected by setting the (0x2c) ‘orient_mode’ bit. For each orientation mode, the ‘orient’ bits have a different meaning as show in the following tables.

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Table 16.meaning of 'orient' bits in symmetric mode

Orient	Name	Angle	Condition
X00	Portrait upright	$315^o < \varphi < 45^o$	|acc_y| < |acc_x| - 'hyst' &acc_x>= 0
X01	Portrait upside down	$135^o < \varphi < 225^o$	|acc_y| < |acc_x| - 'hyst' &acc_x< 0
X10	Landscape left	$45^o < \varphi < 135^o$	|acc_y| >= |acc_x| + 'hyst' & acc_y < 0
X11	Landscape right	$225^o < \varphi < 315^o$	|acc_y| >= |acc_x| + 'hyst' & acc_y >= 0

Table 17.meaning of 'orient' bits in high-asymmetric mode

Orient	Name	Angle	Condition
X00	Portrait upright	$297^o < \varphi < 63^o$	|acc_y| < 2*|acc_x| - 'hyst' &acc_x>= 0
X01	Portrait upside down	$117^o < \varphi < 243^o$	|acc_y| < 2*|acc_x| - 'hyst' &acc_x< 0
X10	Landscape left	$63^o < \varphi < 117^o$	|acc_y| >= 2*|acc_x| + 'hyst' & acc_y < 0
X11	Landscape right	$243^o < \varphi < 297^o$	|acc_y| >= 2*|acc_x| + 'hyst' & acc_y >= 0

Table 18.meaning of 'orient' bits in low-asymmetric mode

Orient	Name	Angle	Condition
X00	Portrait upright	$333^o < \varphi < 27^o$	|acc_y| < 0.5*|acc_x| - 'hyst' &acc_x>= 0
X01	Portrait upside down	$153^o < \varphi < 207^o$	|acc_y| < 0.5*|acc_x| - 'hyst' &acc_x< 0
X10	Landscape left	$27^o < \varphi < 153^o$	|acc_y| >= 0.5*|acc_x| + 'hyst' & acc_y < 0
X11	Landscape right	$207^o < \varphi < 333^o$	|acc_y| >= 0.5*|acc_x| + 'hyst' & acc_y >= 0

In the preceding tables, the parameter 'hyst' stands for a hysteresis which can be selected by the (0x2c) 'orient_hyst' bit. 1LSB of 'orient_hyst' always corresponds to 62.5mg in any g-range. The MSB of 'orient' bits contains information about the direction of the z-axis. It is set to 0(1) if acc_z>=0 (acc_z<0). The hysteresis for z axis is fixed to 0.2g.

The orient interrupt is enabled by writing the (0x16) 'orient_int_en' bit. The interrupt is generated if the value of 'orient' has changed. It is automatically cleared after one stable period of the orient value in non-latched mode. In temporary latched or latched mode, the orient value is kept fixed as long as the interrupt persists. After cleaning the interrupt, the 'orient' will updated with the next following value change.

The change of the 'orient' value and the generation of the interrupt can be blocked according to conditions selected by setting the value of the (0x2c) 'orient_block' bit as described by the following table.

Table 19.blocking conditions for orientation recognition

Orient_block	Conditions
00b	No blocking
01b	Z blocking
10b	Z blocking or acceleration slope in any axis > 0.2g
11b	No blocking

The Z blocking is defined by the following inequality:

$$|acc_z| > z_blocking$$

The parameter z_blocking of the above given equation stands for the contents of the (0x2d) 'z_blocking' bit. Hereby it is possible to define a blocking value between 0g and 0.9375g with an LSB = 0.0625g.

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4.3.8.Freefall interrupt

This interrupt is based on the comparison of acceleration data against a low-g threshold. The interrupt is enabled by writing 1 to the (0x17) 'freefall_int_en' bit. There are two modes available: single mode and sum mode. In single mode the acceleration of each axis is compared with the threshold. In sum mode, the sum of absolute values of all accelerations |acc_x| + |acc_y| + |acc_z| is compared with the threshold. The mode is selected by the (0x24) 'freefall_mode' bit. The free fall threshold is set through the (0x23) 'freefall_th' bits with 1 LSB corresponding to an acceleration of 7.81mg. A hysteresis can be selected by setting the (0x24) 'freefall_hy' bits with 1 LSB corresponding to 125mg.

The freefall interrupt is generated if the absolute values of the acceleration of all axes or their sum are lower than the threshold for at least the time defined by the (0x22) 'freefall_dur' bits. The interrupt is reset if the absolute value of at least one axis or the sum is higher than the threshold plus the hysteresis for at least one data acquisition. The interrupt status is stored in the (0x09) 'freefall_int' bit.

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5. Digital blocks

5.1. FIFO

The da217 embeds 32-level of 12-bit data FIFO for each of the three output channels, X, Y and Z of the acceleration module that can be used to minimize host processor burden. This buffer has four modes: bypass, FIFO, stream, and trigger. Each mode is selected by the settings of the 'FIFO_mode' bits.

5.1.1. Bypass Mode

In bypass mode, FIFO is not operational and, therefore, remains empty.

5.1.2. FIFO Mode

In FIFO mode, acceleration data of the x, y, and z-axes are stored in FIFO. When the number of samples in FIFO equals the level specified in the "watermark_samples" bits, the watermark interrupt is set. FIFO continues accumulating samples until it is full and then stops collecting data. After FIFO stops collecting data, the device continues to operate; therefore, features such as tap detection can be used after FIFO is full. The watermark interrupt continues to occur until the number of samples in FIFO is less than the value stored in the samples bits of the "watermark_samples" bits.

5.1.3. Stream Mode

In stream mode, acceleration data of the x, y, and z-axes are stored in FIFO. When the number of samples in FIFO equals the level specified in the "watermark_samples" bits, the watermark interrupt is set. FIFO continues accumulating samples and holds the latest 32 samples from measurements of the x, y, and z-axes, discarding older data as new data arrives. The watermark interrupt continues occurring until the number of samples in FIFO is less than the value stored in the samples bits of the "watermark_samples" bits.

5.1.3. Trigger Mode

In trigger mode, FIFO accumulates samples, holding the latest 32 samples from measurements of the x, y, and z-axes. After an enable interrupt event occurs, FIFO keeps the last n samples (where n is the value specified by the 'watermark_samples' bits) and then operates in FIFO mode, collecting new samples only when FIFO is not full. Additional trigger events cannot be recognized until the trigger mode is reset. To reset the trigger mode, set the device to bypass mode and then set the device back to trigger mode. Note that the FIFO data should be read first because placing the device into bypass mode clears FIFO.

5.1.4 Retrieving Data from FIFO

The FIFO data is read through the 'acc_x', 'acc_y', and 'acc_z' registers. When the FIFO is in FIFO, stream, or trigger mode, reads to the 'acc_x', 'acc_y', and 'acc_z' registers read data stored in the FIFO. Each time data is read from the FIFO, the oldest x, y, and z-axes data are placed into the 'acc_x', 'acc_y', and 'acc_z' registers.

If a single-byte read operation is performed, the remaining bytes of data for the current FIFO sample are lost. Therefore, all axes of interest should be read in a burst (or multiple-byte) read operation. To ensure that the FIFO has completely popped (that is, that new data has

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completely moved into the ‘acc_x’, ‘acc_y’, and ‘acc_z’ registers), the end of reading a data register is signified by reading the register 0x07.

5.2. Embedded functions

The da217 embeds internal logic able to implement the following functions:

- Step counter
- Step detector
- Significant motion
- Tilt

5.2.1. Step counter

When step counter is enable by set “step_en”, the step counter counts the number of the steps, and recognize out the current status of walk or run.

5.2.2.Step detector

When step counter is enable and step detector interrupt is enable by set “step_int_en”, the step detector function generates an interrupt when a step is recognized.

5.2.3.Significant motion

When step counter is enable and significant motion interrupt is enable by set “SM_int_en”, the significant motion generates an interrupt when a ‘significant motion’, that could be due to a change in user location, is detected.
If the change in user is valid which is judged by the steps difference between its initialization steps and current steps that is higher or equal than the steps threshold of “SM_THRESHOLD” (34H) register.

5.2.4.Tilt

When tilt is enable by set “tilt_int_en”, the tilt function generates an interrupt when an activity change occurs that is the device is tilted by an angle greater than “tilt_threshold” from the start position. The start position is defined as the position of the device when tilt detection is enabled or position of the device when the last tilt interrupt was generated.

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6. Application hints

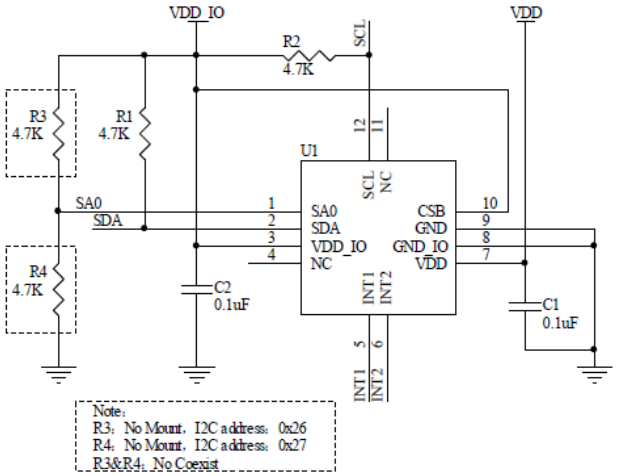


Figure 12 da217 I2C electrical connect

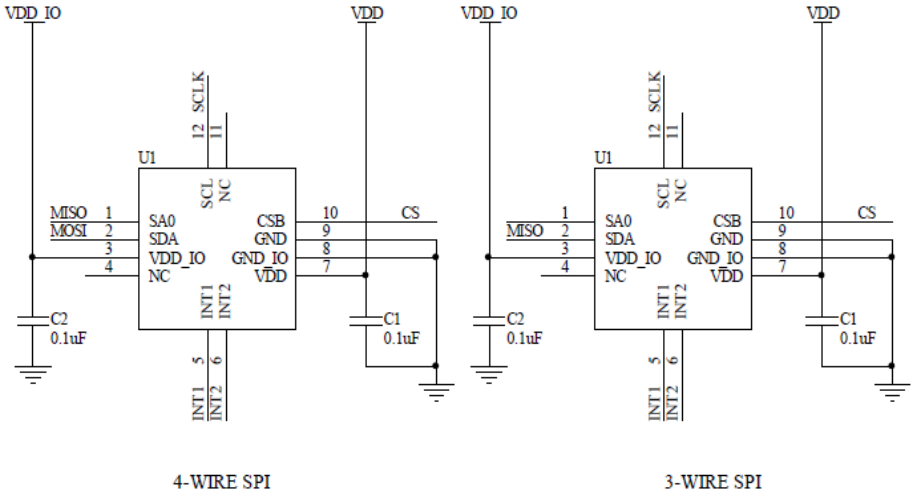


Figure 13 da217 SPI electrical connect

The device core is supplied through VDD line while the I/O pads are supplied through VDD_IO line. Power supply decoupling capacitors (100 nF ceramic) should be placed as near as possible to the pin 7 and pin 3 of the device (common design practice).

The functionality of the device and the measured acceleration data is selectable and accessible through the I2C or SPI interfaces. When using the I2C, CS must be tied high. The functions, the threshold and the timing of the two interrupt pins (INT1 and INT2) can be completely programmed by the user through the I2C/SPI interface.

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7. Register mapping

The table given below provides a listing of the 8 bit registers embedded in the device and the related addresses:

Table 20.Register address map

Name	Type	Register address	Default	Soft Reset
SPI_CONFIG	RW	0x00	81H	NO
CHIP_ID	R	0x01	13H	NO
ACC_X_LSB	R	0x02	00H	YES
ACC_X_MSB	R	0x03	00H	YES
ACC_Y_LSB	R	0x04	00H	YES
ACC_Y_MSB	R	0x05	00H	YES
ACC_Z_LSB	R	0x06	00H	YES
ACC_Z_MSB	R	0x07	00H	YES
FIFO_STATUS	R	0x08	00H	YES
MOTION_FLAG	R	0x09	00H	YES
NEWDATA_FLAG	R	0x0A	00H	YES
TAP_ACTIVE_STATUS	R	0x0B	00H	YES
ORIENT_STATUS	R	0x0C	00H	YES
STEPS_MSB	R	0x0D	00H	YES
STEPS_LSB	R	0x0E	00H	YES
RESOLUTION_RANGE	RW	0x0F	40H	YES
ODR_AXIS	RW	0x10	0FH	YES
MODE_BW	RW	0x11	9EH	YES
SWAP_POLARITY	RW	0x12	0EH	YES
FIFO_CTRL	RW	0x14	00H	YES
INT_SET0	RW	0x15	00H	YES
INT_SET1	RW	0x16	00H	YES
INT_SET2	RW	0x17	00H	YES
INT_MAP1	RW	0x19	00H	YES
INT_MAP2	RW	0x1A	00H	YES
INT_MAP3	RW	0x1B	00H	YES
INT_CONFIG	RW	0x20	00H	YES
INT_LATCH	RW	0x21	00H	YES
FREEFALL_DUR	RW	0x22	09H	YES
FREEFALL_THS	RW	0x23	30H	YES
FREEFALL_HYST	RW	0x24	01H	YES
ACTIVE_DUR	RW	0x27	00H	YES
ACTIVE_THS	RW	0x28	14H	YES
TAP_DUR	RW	0x2A	04H	YES
TAP_THS	RW	0x2B	0AH	YES
ORIENT_HYST	RW	0x2C	18H	YES

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Z_BLOCK	RW	0x2D	88H	YES
RESET_STEP	RW	0x2E	00H	YES
STEP_FILTER	RW	0x33	22H	YES
SM_THRESHOLD	RW	0x34	00H	YES

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8. Registers description

8.1. SPI_CONFIG (00H)

Table 21.SPI_CONFIG register

Default data: 0x81 Type: RW

SDO Active	LSB First	Soft Reset	Unused	Unused	Soft Reset	LSB First	SDO Active

Table 22.SPI_CONFIG description

SDO Active	0:3-wire SPI 1:4-wire SPI
LSB First	0:MSB First 1:LSB First
Soft Reset	1: soft reset

8.2. CHIP_ID (01H)

Table 23.CHIP_ID register

Default data: 0x13 Type: R

0	0	0	1	0	0	1	1

8.3. ACC_X_LSB (02H), ACC_X_MSB (03H)

X-axis acceleration data, the value is expressed in two complement byte and are left justified.

Table 24.ACC_X_LSB register

Default data: 0x00 Type: R

D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Unused	Unused

Table 25.ACC_X_MSB register

Default data: 0x00 Type: R

D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]

8.4. ACC_Y_LSB (04H), ACC_Y_MSB (05H)

Y-axis acceleration data, the value is expressed in two complement byte and are left justified.

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Table 26.ACC_Y_LSB register

Default data: 0x00 Type: R

D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Unused	Unused

Table 27.ACC_Y_MSB register

Default data: 0x00 Type: R

D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]

8.5. ACC_Z_LSB (06H), ACC_Z_MSB (07H)

Z-axis acceleration data, the value is expressed in two complement byte and are left justified.

Table 28.ACC_Z_LSB register

Default data: 0x00 Type: R

D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Unused	Unused

Table 29.ACC_Z_MSB register

Default data: 0x00 Type: R

D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]

8.6. FIFO_STATUS (08H)

Table 30.FIFO_STATUS register

Default data: 0x00 Type: R

Watermark_int	FIFO_full_int	FIFO_entries[5]	FIFO_entries[4]	FIFO_entries[3]	FIFO_entries[2]	FIFO_entries[1]	FIFO_entries[0]

Table 31.MOTION_FLAG register description

Watermark_int	1: the FIFO entries exceed the watermark level
FIFO_full_int	1: the FIFO is full
FIFO_entries[5:0]	FIFO_entries[5:0] reports how many data stored in the FIFO

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8.7. MOTION_FLAG (09H)

Table 32.MOTION_FLAG register

Default data: 0x00 Type: R

Step_int	Orient_int	S_tap_int	D_tap_int	SM_int	Active_int	Tilt_int	Freefall_int

Table 33.MOTION_FLAG register description

Step_int	0: no step 1: one step detected
Orient_int	0:no orient interrupt 1:orient interrupt has occurred
S_tap_int	0:no single tap interrupt 1: single tap interrupt has occurred
D_tap_int	0:no double tap interrupt 1: double tap interrupt has occurred
SM_int	0: no significant motion 1: significant montion has be detected
Active_int	0:no active interrupt 1: active interrupt has occurred
Tilt_int	0: no tilt interrupt 1: tilt interrupt has occurred
Freefall_int	0:no freefall interrupt 1: freefall interrupt has occurred

8.8. NEWDATA_FLAG (0AH)

Table 34.NEWDATA_FLAG register

Default data: 0x00 Type: R

unused	unused	unused	unused	unused	unused	unused	New_data_int

Table 35.NEWDATA_FLAG register description

New_data_int	0: no new_data interrupt 1: new_data interrupt has occurred

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8.9. TAP_ACTIVE_STATUS (0BH)

Table 36.TAP_ACTIVE_STATUS register

Default data: 0x00 Type: R

Tap_sign	Tap_first_x	Tap_first_y	Tap_first_z	Active_sign	Active_first_x	Active_first_y	Active_first_z

Table 37.TAP_ACTIVE_STATUS register description

Tap_sign	Sign of the first tap that triggered interrupt 0: positive 1: negative
Tap_first_x	0: X is not the triggering axis of the tap interrupt 1: indicate X is the triggering axis of the tap interrupt.
Tap_first_y	0: Y is not the triggering axis of the tap interrupt 1: indicate Y is the triggering axis of the tap interrupt.
Tap_first_z	0: Z is not the triggering axis of the tap interrupt 1: indicate Z is the triggering axis of the tap interrupt.
Active_sign	active_sign: Sign of the first active interrupt. 0: positive, 1: negative
Active_first_x	0: X is not the triggering axis of the active interrupt 1: indicate X is the triggering axis of the active interrupt.
Active_first_y	0: Y is not the triggering axis of the active interrupt 1: indicate Y is the triggering axis of the active interrupt.
Active_first_z	0: Z is not the triggering axis of the active interrupt 1: indicate Z is the triggering axis of the active interrupt.

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8.10. ORIENT_STATUS (0CH)

Table 38.ORIENT_STATUS register

Default data: 0x00 Type: R

unused	Orient[2]	Orient[1]	Orient[0]	unused	unused	Step_stauts[1]	Step_stauts[0]

Table 39.ORIENT_STATUS register description

Orient[2]	orientation value of ‘z’ axis 0: upward looking, 1: downward looking
Orient[1:0]	orientation value of ‘x’, ‘y’ axes 00: portrait upright 01: portrait upside down 10: landscape left 11:landscape right
Step_status[1:0]	00/11: idle 01: walk 10: run

8.11. STEPS_MSB (0DH), STEPS_LSB (0EH)

Table 40.STEPS_MSB register

Default data: 0x00 Type: R

Steps[15]	Steps [14]	Steps [13]	Steps [12]	Steps [11]	Steps [10]	Steps [9]	Steps [8]

Table 41.STEPS_LSB register

Default data: 0x00 Type: R

Steps [7]	Steps [6]	Steps [5]	Steps [4]	Steps [3]	Steps [2]	Steps [1]	Steps [0]

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8.12. RESOLUTION_RANGE (0FH)

Table 42.RESOLUTION_RANGE register

Default data: 0x40 Type: RW

HP_en	Wdt_en	Wdt_time	unused	Resolution[1]	Resolution[0]	FS[1]	FS[0]

Table 43.RESOLUTION_RANGE register description

HP_en	0:disable high pass filter 1:enable
Wdt_en	0: disable watch dog 1: enable watch dog
Wdt_time	0: 1ms 1: 50ms
Resolution[1:0]	00:14bit 01:12bit 10:10bit 11:8bit
FS[1:0]	full scale 00: +/-2g 01: +/-4g 10:+/-8g 11:+/-16g

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8.13. ODR_AXIS (10H)

Table 44.ODR_AXIS register

Default data: 0x0F Type: RW

X-axis_disable	Y-axis_disable	Z-axis_disable	unused	ODR[3]	ODR[2]	ODR[1]	ODR[0]

Table 45.ODR_AXIS register description

X-axis_disable	0: enable X axis 1: disable X axis
Y-axis_disable	0: enable Y axis 1: disable Y axis
Z-axis_disable	0: enable Z axis 1: disable Z axis
ODR[3:0]	0000: 1Hz 0001: 1.95Hz 0010: 3.9Hz 0011: 7.81Hz 0100: 15.63Hz 0101: 31.25Hz 0110: 62.5Hz 0111: 125Hz 1000: 250Hz 1001: 500Hz 1010-1111: unused

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8.14. MODE_BW (11H)

Table 46.MODE_BW register

Default data: 0x9E Type: RW

PWR_OFF	unused	unused	unused	unused	BW[1]	BW[0]	autosleep_en

Table 47.MODE_BW register description

PWR_OFF	0: normal mode 1: suspend mode
BW[1:0]	Bandwidth 00/11:500hz 01:250 10:100
Autosleep_en	0: working the current ODR state all the way 1: Working at 12.5hz in inactive state, automatic switched to normal mode during active state

8.15. SWAP_POLARITY (12H)

Table 48.SWAP_POLARITY register

Default data: 0x0E Type: RW

Swap & Polarity register is OTP register too, OTP address: 0x13

unused	unused	unused	unused	X_polarity	Y_polarity	Z_polarity	X_Y_swap

Table 49.SWAP_POLARITY register description

X_polarity	0: remain the polarity of X-axis. 1: reverse the polarity of X-axis.
Y_polarity	0: remain the polarity of Y-axis. 1: reverse the polarity of Y-axis.
Z_polarity	0: remain the polarity of Z-axis. 1: reverse the polarity of Z-axis.
X_Y_swap	0: Don’t need swap the output data for X/Y axis 1: swap the output data for X/Y axis.

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8.16. FIFO_CTRL (14H)

Table 50.FIFO_CTRL register

Default data: 0x00 Type: RW

FIFO_mode[1]	FIFO_mode[0]	unused	Watermark_ samples[4]	Watermark_ samples[3]	Watermark_ samples[2]	Watermark_ samples[1]	Watermark_ samples[0]

Table 51.FIFO_CTRL register description

FIFO_mode[1:0]	00: bypass mode 01: FIFO mode 10: stream mode 11: trigger mode
Watermark_ samples[4:0]	Indicate how many data entries needed to trig a watermark interrupt

8.17. INT_SET0 (15H)

Table 52.INT_SET0 register

Default data: 0x00 Type: RW

unused	unused	unused	Tilt_int_en	Watermark_int_en	FIFO_full_int_en	SM_int_en	Step_int_en

Table 53.INT_SET01 register description

Tilt_int_en	0: disable 1: enable tilt interrupt
Watermark_int_en	0:disable 1:enable watermark interrupt
FIFO_full_int_en	0:disable 1:enable FIFO_full interrupt
SM_int_en	0: disable 1: enable SM(significant motion) interrupt
Step_int_en	0: disable 1:emable step counter interrupt

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8.18. INT_SET1 (16H)

Table 54.INT_SET1 register

Default data: 0x00 Type: RW

INT_source[1]	INT_source[0]	S_tap_int_en	D_tap_int_en	Orient_int_en	Active_int_en_z	Active_int_en_y	Active_int_en_x

Table 55.INT_SET1 register description

INT_source[1:0]	00: oversampling data (ODR_period =ODR*OSR) 01: unfiltered data (ODR_period =ODR) 10/11: filtered data (ODR_period =ODR IIR)
S_tap_int_en	0: disable the single tap interrupt. 1: enable the single tap interrupt.
D_tap_int_en	0: disable the double tap interrupt. 1: enable the double tap interrupt.
Orient_int_en	0: disable the orient interrupt. 1: enable the orient interrupt.
Active_int_en_z	0: disable the active interrupt for the z axis. 1: enable the active interrupt for the z axis.
Active_int_en_y	0: disable the active interrupt for the y axis. 1: enable the active interrupt for the y axis.
Active_int_en_x	0: disable the active interrupt for the x axis. 1: enable the active interrupt for the x axis.

8.19. INT_SET2 (17H)

Table 56.INT_SET2 register

Default data: 0x00 Type: RW

Temporary_dis	Temp_dis_time[1]	Temp_dis_time[0]	New_data_int_en	Freefall_int_en	unused	unused	unused

Table 57.INT_SET2 register description

Temporary_dis	temporary disable all interrupts for a short time(configured by temp_dis_time)
Temp_dis_time[1:0]	00:100ms 01:1s 10:2s 11:4s
New_data_int_en	0: disable the new data interrupt. 1: enable the new data interrupt.
Freefall_int_en	0: disable the freefall interrupt. 1: enable the freefall interrupt

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8.20. INT_MAP1 (19H)

Table 58.INT_MAP1 register

Default data: 0x00 Type: RW

Int1_SM	Int1_orient	Int1_s_tap	Int1_d_tap	Int1_tilt	Int1_active	Int1_step	Int1_freefall

Table 59.INT_MAP1 register description

Int1_SM	0: doesn't mapping SM interrupt to INT1 1: mapping SM interrupt to INT1
Int1_orient	0: doesn't mapping orient interrupt to INT1 1: mapping orient interrupt to INT1
Int1_s_tap	0: doesn't mapping single tap interrupt to INT1 1: mapping single tap interrupt to INT1
Int1_d_tap	0: doesn't mapping double tap interrupt to INT1 1: mapping double tap interrupt to INT1
Int1_tilt	0: doesn't mapping tilt interrupt to INT1 1: mapping tilt interrupt to INT1
Int1_active	0: doesn't mapping active interrupt to INT1 1: mapping active interrupt to INT1
Int1_step	0: doesn't mapping step counter interrupt to INT1 1: mapping step counter interrupt to INT1
Int1_freefall	0: doesn't mapping freefall interrupt to INT1 1: mapping freefall interrupt to INT1

8.21. INT_MAP2 (1AH)

Table 60.INT_MAP2 register

Default data: 0x00 Type: RW

Int2_new_data	Int2_watermark	Int2_FIFO_full	unused	unused	Int1_FIFO_full	Int1_watermark	Int1_new_data

Table 61.INT_MAP2 register description

Int2_new_data	0: doesn't mapping new data interrupt to INT2 1: mapping new data interrupt to INT2
Int2_watermark	0: doesn't mapping watermark interrupt to INT2 1: mapping watermark interrupt to INT2
Int2_FIFO_full	0: doesn't mapping FIFO full interrupt to INT2 1: mapping FIFO full interrupt to INT2
Int1_FIFO_full	0: doesn't mapping FIFO full interrupt to INT1 1: mapping FIFO full interrupt to INT1
Int1_watermark	0: doesn't mapping watermark interrupt to INT1 1: mapping watermark interrupt to INT1
Int1_new_data	0: doesn't mapping new data interrupt to INT1 1: mapping new data interrupt to INT1

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8.22. INT_MAP3 (1BH)

Table 62.INT_MAP3 register

Default data: 0x00 Type: RW

Int2_SM	Int2_orient	Int2_s_tap	Int2_d_tap	Int2_tilt	Int2_active	Int2_step	Int2_freefall

Table 63.INT_MAP3 register description

Int2_SM	0: doesn't mapping SM interrupt to INT2 1: mapping SM interrupt to INT2
Int2_orient	0: doesn't mapping orient interrupt to INT2 1: mapping orient interrupt to INT2
Int2_s_tap	0: doesn't mapping single tap interrupt to INT2 1: mapping single tap interrupt to INT2
Int2_d_tap	0: doesn't mapping double tap interrupt to INT2 1: mapping double tap interrupt to INT2
Int2_tilt	0: doesn't mapping tilt interrupt to INT2 1: mapping tilt interrupt to INT2
Int2_active	0: doesn't mapping active interrupt to INT2 1: mapping active interrupt to INT2
Int2_step	0: doesn't mapping step counter interrupt to INT2 1: mapping step counter interrupt to INT2
Int2_freefall	0: doesn't mapping freefall interrupt to INT2 1: mapping freefall interrupt to INT2

8.23. INT_CONFIG (20H)

Table 64.INT_CONFIG register

Default data: 0x00 Type: RW

Reset_int	unused	unused	unused	Int2_od	Int2_lvl	Int1_od	Int1_lvl

Table 65.INT_CONFIG register description

Reset_int	Write'1'to reset all latched int.
Int2_od	0: select push-pull output for INT2 1: selects OD output for INT2
Int2_lvl	0: selects active level high for pin INT2 1: selects active level low for pin INT2
Int1_od	0: select push-pull output for INT1 1: selects OD output for INT1
Int1_lvl	0: selects active level high for pin INT1 1: selects active level low for pin INT1

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8.24. INT_LATCH (21H)

Table 66.INT_LATCH register

Default data: 0x00 Type: RW

Latch_int2[3]	Latch_int2[2]	Latch_int2[1]	Latch_int2[0]	Latch_int1[3]	Latch_int1[2]	Latch_int1[1]	Latch_int1[0]

Table 67.INT_LATCH register description

Latch_int2[3:0]	0000: non-latched 0001: temporary latched 250ms 0010: temporary latched 500ms 0011: temporary latched 1s 0100: temporary latched 2s 0101: temporary latched 4s 0110: temporary latched 8s 0111: latched 1000: non-latched 1001: temporary latched 1ms 1010: temporary latched 1ms 1011: temporary latched 2ms 1100: temporary latched 25ms 1101: temporary latched 50ms 1110: temporary latched 100ms 1111: latched
Latch_int1[3:0]	0000: non-latched 0001: temporary latched 250ms 0010: temporary latched 500ms 0011: temporary latched 1s 0100: temporary latched 2s 0101: temporary latched 4s 0110: temporary latched 8s 0111: latched 1000: non-latched 1001: temporary latched 1ms 1010: temporary latched 1ms 1011: temporary latched 2ms 1100: temporary latched 25ms 1101: temporary latched 50ms 1110: temporary latched 100ms 1111: latched

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8.25. FREEFALL_DUR (22H)

Table 68.FREEFALL_DUR register

Default data: 0x09 Type: RW

Freefall_dur[7]	Freefall_dur[6]	Freefall_dur[5]	Freefall_dur[4]	Freefall_dur[3]	Freefall_dur[2]	Freefall_dur[1]	Freefall_dur[0]

Table 69.FREEFALL_DUR register description

Freefall_dur[7:0]	Delay time for freefall delay_time = (freefall_dur + 1) * 2ms range from 2ms to 512ms default: 20ms

8.26. FREEFALL_THS (23H)

Table 70.FREEFALL_THS register

Default data: 0x30 Type: RW

Freefall_th[7]	Freefall_th[6]	Freefall_th[5]	Freefall_th[4]	Freefall_th[3]	Freefall_th[2]	Freefall_th[1]	Freefall_th[0]

Table 71.FREEFALL_THS register description

Freefall_th[7:0]	freefall threshold = freefall_th * 7.81mg LSB = 7.81mg default is 375mg

8.27. FREEFALL_HYST (24H)

Table 72.FREEFALL_HYST register

Default data: 0x01 Type: RW

unused	unused	unused	unused	unused	Freefall_mode	Freefall_hy[1]	fFreefall_hy[0]

Table 73.FREEFALL_HYST register description

Freefall_mode	0: single mode. 1: sum mode.
Freefall_hy[1:0]	Set the hysteresis for freefall detection. Free fall hysteresis time = freefall_hy* 125mg LSB = 125mg

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8.28. ACTIVE_DUR (27H)

Table 74.ACTIVE_DUR register

Default data: 0x00 Type: RW

Inactive_dur[3]	Inactive_dur[2]	Inactive_dur[1]	Inactive_dur[0]	Active_dur[3]	Active_dur[2]	Active_dur[1]	Active_dur[0]

Table 75.ACTIVE_DUR register description

Inactive_dur[4:0]	inactive duration time = (Inactive_dur + 1)* ODR_period
Active_dur[4:0]	Active duration time = (Active_dur + 1)* ODR_period

8.29. ACTIVE_THS (28H)

Table 76.ACTIVE_THS register

Default data: 0x14 Type: RW

Active_th[7]	Active_th [6]	Active_th [5]	Active_th[4]	Active_th [3]	Active_th [2]	Active_th [1]	Active_th [0]

Table 77.ACTIVE_THS register description

Active_th[7:0]	Threshold of active interrupt=Active_th*K(mg) K = 3.91(2g range), K =7.81(4g range), K=15.625(8g range), K=31.25(16g range).

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8.30. TAP_DUR (2AH)

Table 78.TAP_DUR register

Default data: 0x04 Type: RW

Tap_quiet	Tap_shock	unused	unused	unused	Tap_dur[2]	Tap_dur[1]	Tap_dur[0]

Table 79.TAP_DUR register description

Tap_quiet	0: tap quiet duration 30ms. 1: tap quiet duration 20ms.
Tap_shock	0: tap shock duration 50ms. 1: tap shock duration 70ms.
Tap_dur[2:0]	Tap duration selects the length of the time window for the second shock. 000: 50ms 001: 100ms 010: 150ms 011: 200ms 100: 250ms 101: 375ms 110: 500ms 111: 700ms

8.31. TAP_THS (2BH)

Table 80.TAP_THS register

Default data: 0x0a Type: RW

Tilt_time[2]	Tilt_time[1]	Tilt_time[0]	Tap_th [4]	Tap_th [3]	Tap_th [2]	Tap_th [1]	Tap_th [0]

Table 81.TAP_THS register description

Tilt_time[2:0]	stable time for tilt detection 00:32*ODR_period 01:96* ODR_period 00:160*ODR_period 01:224* ODR_period
Tap_th [4:0]	Threshold of tap interrupt=Tap_th*K(mg) K = 62.5(2g range) K = 125(4g range) K = 250(8g range) K = 500 (16g range)

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8.32. ORIENT_HYST (2CH)

Table 82.ORIENT_HYST register

Default data: 0x18 Type: RW

unused	Orient_hyst[2]	Orient_hyst[1]	Orient_hyst[0]	Orient_block[1]	Orient_block [0]	Orient_mode [1]	Orient_mode [0]

Table 83.ORIENT_HYST register description

Orient_hyst[2:0]	Set the hysteresis of the orientation interrupt 1LSB = 62.5mg.
Orient_block[1:0]	00: no blocking 01: z blocking 10: z blocking or slope in any axis > 0.2g 11: no blocking
Orient_mode [1:0]	00: symmetrical 01: high-asymmetrical 10: low-asymmetrical 11:synmmetrical

8.33. Z_BLOCK (2DH)

Table 84.Z_BLOCK register

Default data: 0x88 Type: RW

Tilt_th[3]	Tilt_th[2]	Tilt_th[1]	Tilt_th[0]	Z_blocking[3]	Z_blocking[2]	Z_blocking[1]	Z_blocking[0]

Table 85.Z_BLOCK register description

Tilt_th[3:0]	Set the tilt threshold 0-480mg with LSB=32mg
Z_blocking[3:0]	Defines the blocking acc_z between 0g to 0.9375g. 1LSB=62.5mg

8.34. RESET_STEP (2EH)

Table 86.RESET_STEP register

Default data: 0x00 Type: RW

Reset_steps	unused	unused	unused	unused	unused	unused	unused

Table 87.Z_BLOCK register description

Reset_steps	Write 1 to reset step counter

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8.35. STEP_FILTER (33H)

Table 88.STEP_FILTER register

Default data: 0x22 Type: RW

Step_en	unused	unused	unused	unused	unused	unused	unused

Table 89.STEP_CONFIG4 register description

Step_en	0:disable 1:Enable step detect function

8.36. SM_THRESHOLD (34H)

Table 90.SM_THRESHOLD register

Default data: 0x00 Type: RW

SM_threshold[7]	SM_threshold[6]	SM_threshold[5]	SM_threshold[4]	SM_threshold[3]	SM_threshold[2]	SM_threshold[1]	SM_threshold[0]

Table 91.SM_THRESHOLD register description

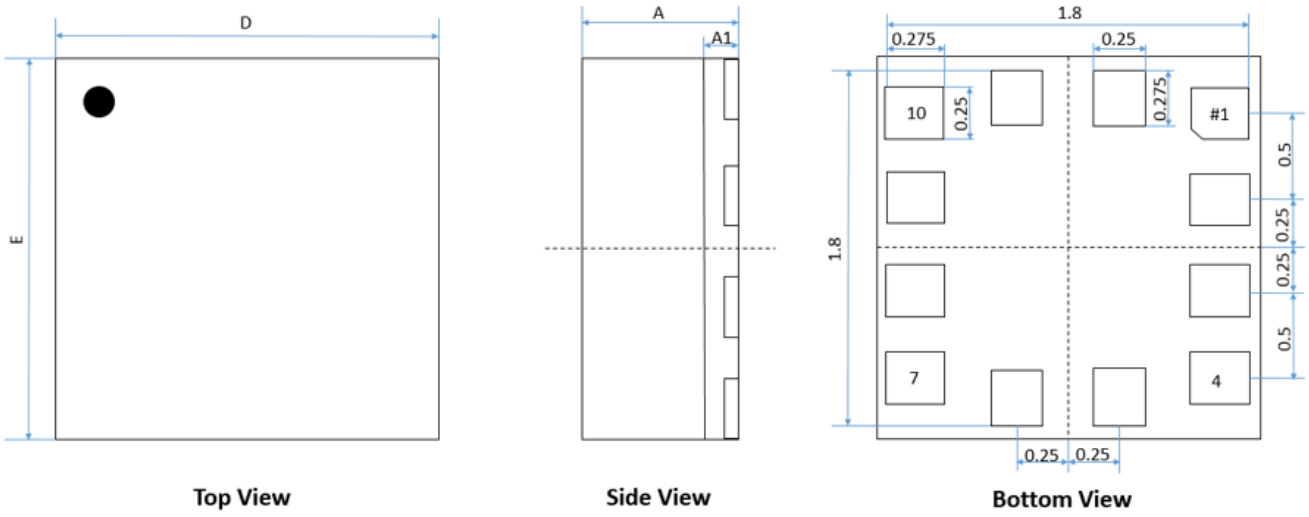
SM_threshold[7:0]	0-255 step

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9. Package information

9.1. Outline dimensions

The sensor housing is a standard LGA package. Its dimensions are the following.



COMMON DIMENSIONS(MM)			
PKG.	W:VERYVERY THIN		
REF.	MIN.	NOM.	MAX
A	0.82	0.9	0.98
A1(SUBSTRATE)	200 REF.		
D	1.9	2	2.1
E	1.9	2	2.1

Figure 14 12Pin LGA Mechanical data and package dimensions

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9.2. Landing pattern recommendation

For the design of the landing patterns, we recommend the following dimensioning:

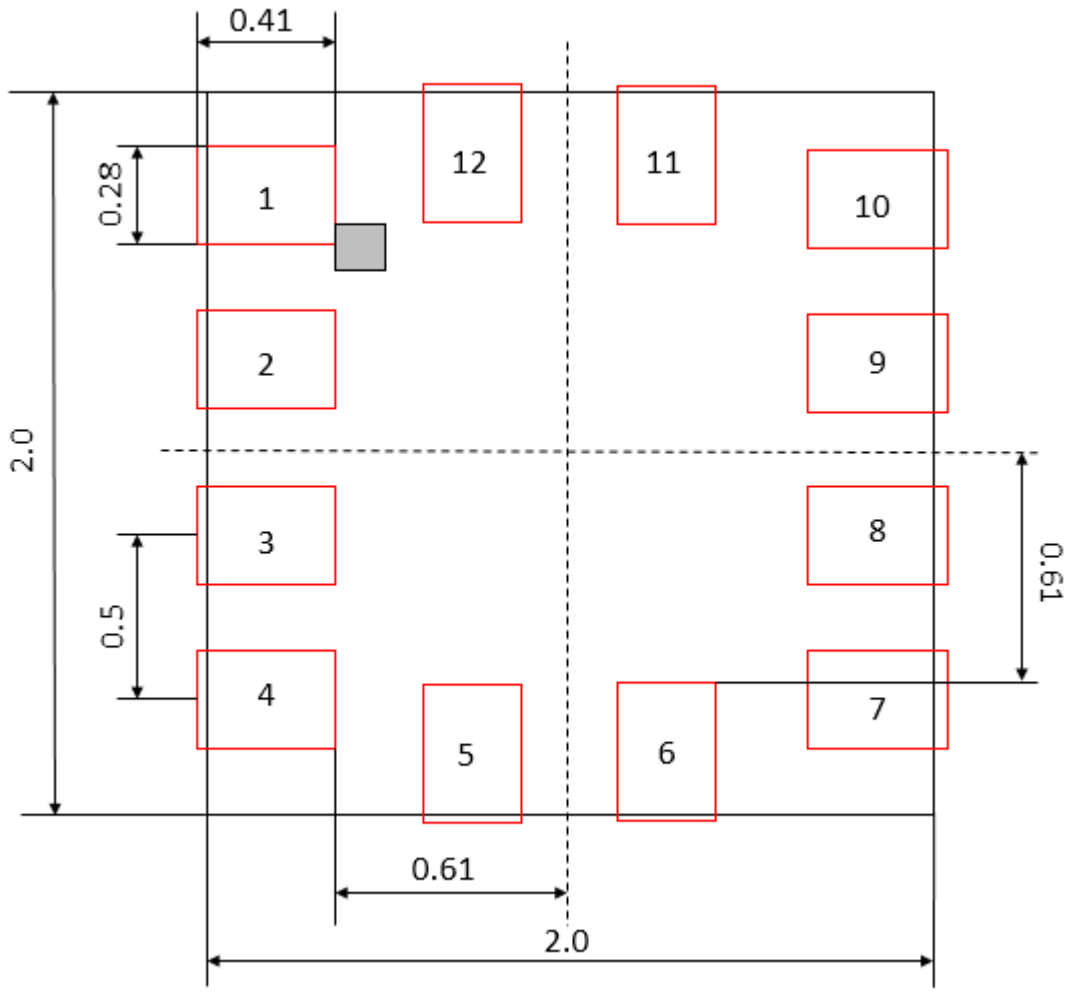


Figure 15 landing patterns; dimensions in mm

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9.3. Tape and reel specification

The da217 is shipped in a standard pizza box

The box dimension for 1 reel is: L x W x H = 35cm x 35cm x 5cm

The da217 quantity: 5000pcs per reel, please handle with care.

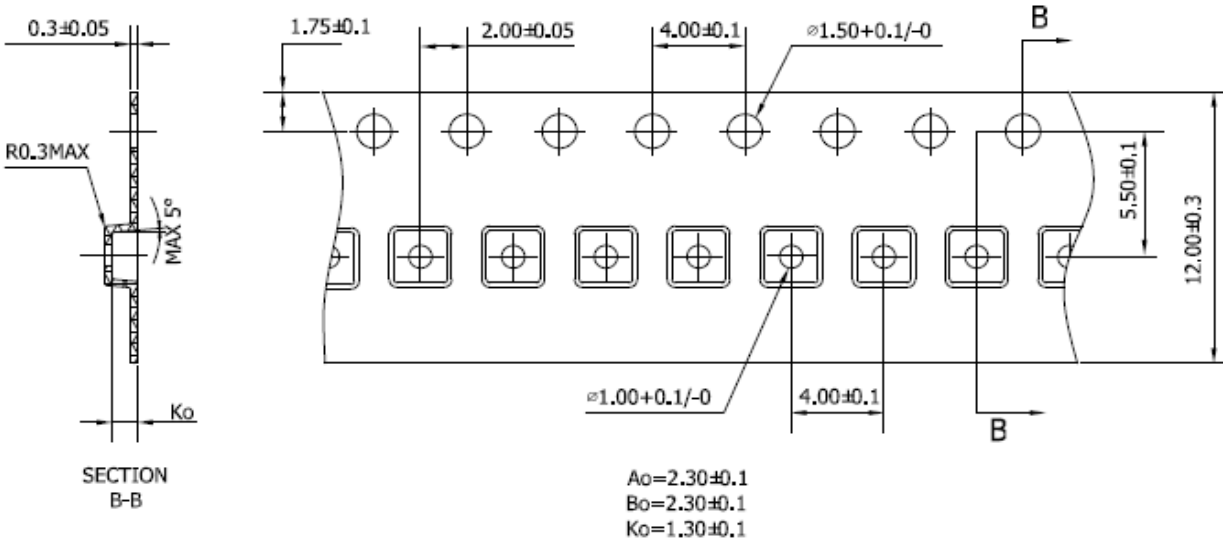


Figure 16 Tape and reel dimension in mm

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10. Reliability

The qualification condition of MiraMEMS's products is based on the stress test qualification for integrated circuits, JEDEC JESD47H.01 Standard. The test summary is listed below.

Table 92.Accelerated Life Tests

Test	Condition	Qty/lot	Lot	Acc/Rej	Result
High Temperature Storage (HTS)*	150C, 1000hrs JEDEC JESD22-A103D Condition A	77	3	0/1	PASS
High Temperature Operating Life Test (HTOL)*	125C, 1000hrs, 3.63V biased JEDEC JESD22-A108D	77	3	0/1	PASS
Highly Accelerated Stress Test (uHAST)*	130C/85%, 96hrs JEDEC JESD22-A118A Condition A	77	3	0/1	PASS

*Tests are preceded by MSL3 preconditioning in accordance with JEDEC JESD22-A113F

Table 93.Component Level Tests

Test	Condition	Qty/lot	Lot	Acc/Rej	Result
Preconditioning(MSL3)	24hrs HTSL (125C) ->192Hrs WHTSL (30C/60%RH) + 3x PbFree Reflow, 260C max JEDEC JESD22-A113F	77	3	0/1	PASS
Temperature Cycle*	-40C~85C (air to air) 500 cycles JEDEC JESD22-A104D Condition N	77	3	0/1	PASS
Shock Test	10000G/0.2ms, X/Y/Z 5 time/ direction JEDEC JESD22-B104C	10	3	0/1	PASS
Vibration Test	sweep 20-2000Hz, 4 times/direction JEDEC JESD22-B103B Condition 1 60Hz_32h/direction	10	2	0/1	PASS
ESD Susceptibility	2000V (HBM) JEDEC JS-001-2012	6	1	0/1	PASS
	200V (MM) JEDEC JESD22-A115C	6	1	0/1	PASS
	500V (CDM) JEDEC JESD22-C101E	6	1	0/1	PASS
Latch-up	>+/-2Vcc, max >+/-2Icc, max JEDEC JESD-78D	6	1	0/1	PASS

*Tests are preceded by MSL3 preconditioning in accordance with JEDEC JESD22-A113F

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11. Revision history

Table 94.Document revision history

Date	Revision	Changes
27-Mar.-2017	0.1	Initial release
28-Jun.-2017	0.2	Modify package size

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