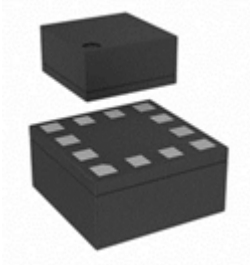
# MEMS digital output touch force sensor

# High sensitivity low power capacitance touch force sensor

## Key Features



- High sensitivity with low noise level
- 0 to 10N Range with good linearity
- Supply voltage, 1.71V to 3.6V
- Small size 2x2x1 mm LGA-12 package
- Digital I2C/SPI output interface
- 14 bit resolution
- Low power consumption
- RoHS compliant
- 10000G high shock survivability

## Applications

- Mobile / Smart phone
- Smart watch
- PC mouse pad/ Touchpads
- Video game controller
- Smart bottom
- Smart home application
- Robotic

## Product view

The df220 is a low power high performance digital micro touch force sensor developed by MEMS (microelectromechanical system) technology. This highly sensitive force sensor consists of a MEMS element and an ASIC packaged in a 2x2x1mm land grid array (LGA). The sensing element is fabricated by single crystal silicon with DRIE process and is protected by hermetically sealed silicon cap from the environment. The device supports a wide range applications requiring accurate measurement of small force (0 to 10N) with data output rate from 1Hz to 1KHz. The sleep mode makes it good for handset power management. Standard I2C and SPI interface is used to communicate with the chip. With such small standard LGA-12 (2mmX2mmX1mm), df220 micro touch force sensor is good for applications with limited spacing, pick-and-place assembly and reflow soldering to PCB or flex substrate.



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# 1. Pin Description

## 1.1. Block Diagram

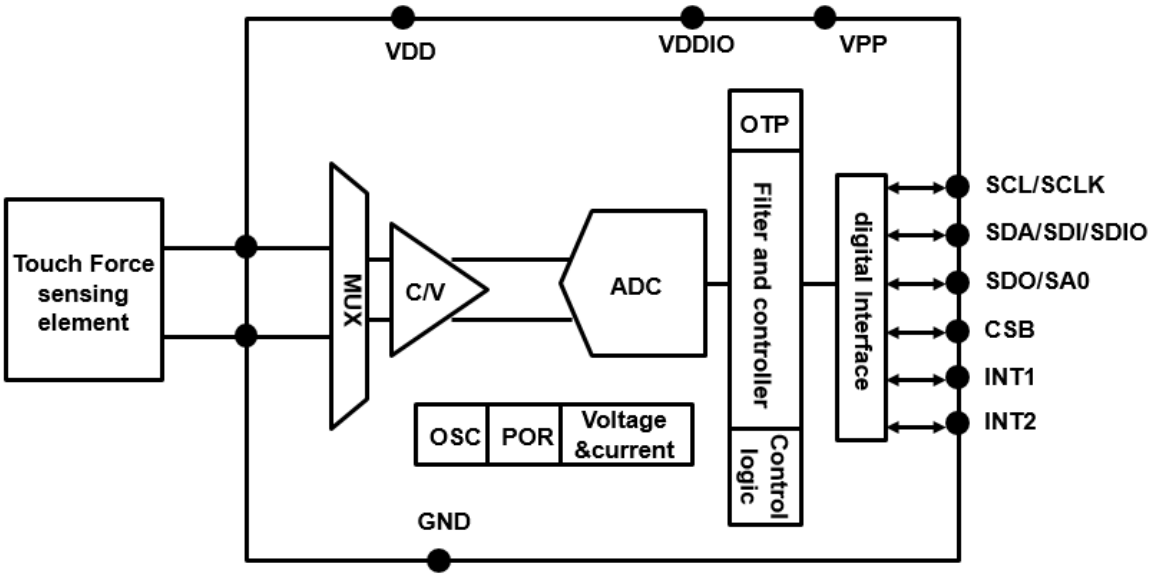
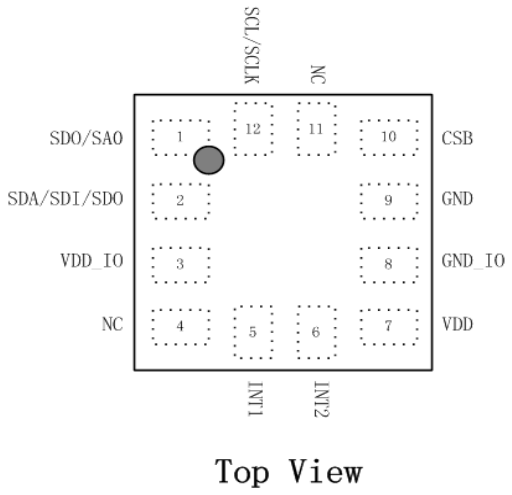



**Figure 1. Block Diagram**

## 1.2. Pin Description




Top View

**Figure 2. Pin Description Bottom View**



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**Table 1. Pin Description**

| Pin# | Name | I/O Type | Function |
|---|---|---|---|
| 1 | SDO<br>SA0 | Digital out<br>Digital in | SPI(4-wire mode) serial data output (SDO)<br>I2C less significant bit of the device address (SA0)<br>When using the I2C communication, SA0 pin must be connected to VDDIO or GND |
| 2 | SDA<br>SDI<br>SDO | Digital in/out | I2C serial data input/output(SDA)<br>SPI(4-wire mode) serial data input (SDI)<br>3-wire interface serial data input/output (SDO) |
| 3 | VDD_IO | Supply | Power supply for I/O pins |
| 4 | NC | -- | Not connected |
| 5 | INT1 | Digital out | Interrupt pin1 |
| 6 | INT2 | Digital out | Interrupt pin2 |
| 7 | VDD | Supply | Power supply |
| 8 | GND_IO | Ground | Ground supply for I/O pins |
| 9 | GND | Ground | Ground supply |
| 10 | CSB | Digital in | Chip select for SPI<br>When using the I2C communication, CSB pin must be connected to VDDIO |
| 11 | NC | -- | Not connected |
| 12 | SCL<br>SCLK | Digital in | I2C serial clock (SCL)<br>SPI serial clock (SCLK) |



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# 2. Electrical Specifications

## 2.1. Electrical Characteristics

Vdd = 2.5 V,T = 25 °C unless otherwise noted

**Table 2. Electrical Characteristics**

| Symbol | Parameter | Test conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| VDD | Supply voltage | | 1.62 | 2.5 | 3.6 | V |
| VDD_IO | I/O Pins supply voltage | | 1.62 | | VDD | V |
| IDD | current consumption in normal mode | Top=25℃, ODR=1kHz | | 180 | | uA |
| IDD_LP | current consumption in low power mode | Top=25℃, ODR=62.5Hz, BW=500Hz | | 40 | | uA |
| IDD_SM | current consumption in suspend mode | Top=25℃ | | 0.7 | | uA |
| VIH | Digital high level input voltage | SPI&I2C | 0.7*Vdd_IO | | | V |
| VIL | Digital low level input voltage | SPI&I2C | | | 0.3*Vdd_IO | V |
| VOH | high level output voltage | | 0.9*Vdd_IO | | | V |
| VOL | Low level output voltage | | | | 0.1*Vdd_IO | V |
| BW | System bandwidth | | 1.95 | | 500 | Hz |
| ODR | Output data rate | | 1 | | 1000 | Hz |
| TWU | Wake-up time | From stand-by | | 1 | | ms |
| TSU | Start-up time | From power off | | 3 | | ms |
| PSRR | Power Supply Rejection Rate | Top=25℃ | | | 20 | mg/V |



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# 2.2. Absolute Maximum Ratings

Stresses below those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 3. Absolute Maximum Rating**

| Item | Symbol | Test conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | VDD | | -0.3 | | 4.25 | V |
| | VDDIO | | -0.3 | | 4.25 | |
| Max Force Range | $P_r$ | | | x3 | | FS |
| Temperature Range | $T_r$ | | -40 | | 85 | ℃ |
| Analog pin voltage | $V_a$ | | -0.3 | | VDD+0.3 | V |
| Digital output voltage | $V_{DO}$ | | -0.3 | | VDDIO+0.3 | V |
| ESD Susceptibility | HBM | | | 2000 | | V |
| | CDM | | | 500 | | V |
| | MM | | | 200 | | V |
| Storage temperature | | | -40 | | 85 | ℃ |

***Note:*** *Supply voltage on any pin should never exceed 4.25V*

This is a mechanical shock sensitive device, improper handling can cause permanent damages to the part.

This is an ESD sensitive device, improper handling can cause permanent damages to the part.

# 2.3. Mechanical Characteristics

Vdd = 2.5 V, T = 25 °C unless otherwise noted

a. The product is factory calibrated at 2.5 V. The operational power supply range is from 1.71V to 3.6 V.

**Table 4. Mechanical Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Measurement range | FS(1) | | 10 | | N |
| Sensitivity (T=25°C) | So | | 1400 | | lsb/N |
| noise density (Normal mode 31.25Hz) | Fn | | 70 | | uN/sqrt(Hz) |
| FSTDEA noise (Normal mode 31.25Hz) | Fnoise | | 0.4 | | mN |
| Operation temperature range | Top | -40 | | 85 | °C |

***Note:***

***Calibrated measurement range is from 0N to 10N, the accuracy of measurement over 10N is not guaranteed.***



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# 3. Communication Interface

## 3.1. Communication Interface Electrical specification

### 3.1.1. SPI Electrical Specification

**Table 5. Electrical Specification of the SPI Interface Pins**

| Symbol | Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| fsclk | Clock frequency | Max load on SDIO or SDO = 25pF | | 10 | MHz |
| $t_{SCKL}$ | SLCK low pulse | | 20 | | |
| $t_{SCKH}$ | SLCK high pulse | | 20 | | |
| $t_{SDI_setup}$ | SDI setup time | | 20 | | ns |
| $t_{SDI_hold}$ | SDI hold time | | 20 | | ns |
| $t_{SDO_OD}$ | SDO/SDI output delay | Load = 25pF | | 30 | ns |
| | | Load = 250pF | | 40 | ns |
| $t_{CSB_setup}$ | CSB setup time | | 20 | | ns |
| $t_{CSB_hold}$ | CSB hold time | | 40 | | ns |

The figure below shows the definition of the SPI timing given in the above table:

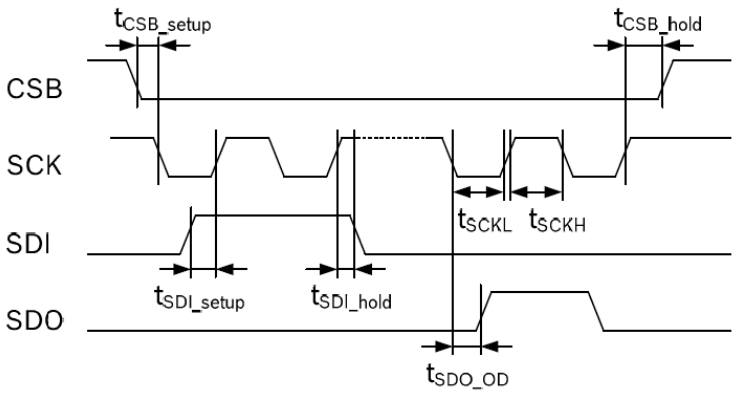



**Figure 3. SPI Slave Timing Diagram**



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# 3.1.2.I2C Electrical Specification

**Table 6. Electrical Specification of the I2C Interface Pins**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| fscl | Clock frequency | | 400 | kHz |
| $t_{LOW}$ | SCL low pulse | 1.3 | | us |
| $t_{HIGH}$ | SCL high pulse | 0.6 | | us |
| $t_{SUDAT}$ | SDA setup time | 0.1 | | us |
| $t_{HDDAT}$ | SDA hold time | 0.0 | | us |
| $t_{SUSTA}$ | Setup Time for a repeated start condition | 0.6 | | us |
| $t_{HDSTA}$ | Hold time for a start condition | 0.6 | | us |
| $t_{SUSTO}$ | Setup Time for a stop condition | 0.6 | | us |
| $t_{BUF}$ | Time before a new transmission can start | 1.3 | | us |

The figure below shows the definition of the I2C timing given in the above table:

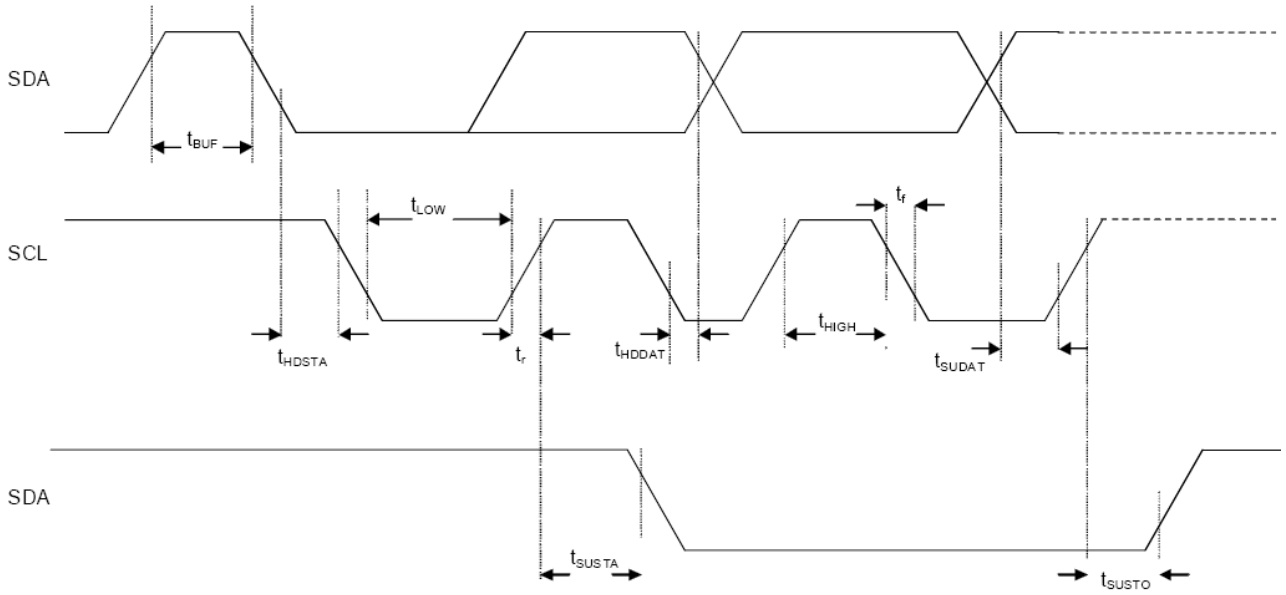



**Figure 4. I2C Slave Timing Diagram**



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# 3.2. Digital Interface Operation

The df220 supports two serial digital interface protocols for communications as slave with a host device: SPI and I2C. The active interface is selected by the state of the pin CS, 0 selects SPI and 1 selects I2C. By default, SPI operates in 3-wire mode and it can be re-configured by writing 1 to bit 'SDO_active' to work in 4-wire mode. Both interfaces share the same pins. The mapping for each interface is given in the following table:

**Table 7. Mapping of the Interface Pins**

| PIN name | I2C | SPI |
|---|---|---|
| SCL/SCLK | Serial clock | Serial clock |
| SDA/SDI | Serial Data | Data input (4-wire mode).<br>Data input/output (3-wire mode) |
| SA0/SDO | Used to set LSB of I2C address | Data output (4-wire mode) |
| CSB | Unused | Chip select |

## 3.2.1. SPI Operation

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of framing. Once the beginning of the frame has been determined, timing is straightforward. The first phase of the transfer is the instruction phase, which consists of 16 bits followed by data that can be of variable lengths in multiples of 8 bits. If the device is configured with CSB tied low, framing begins with the first rising edge of SCLK.

The instruction phase is the first 16 bits transmitted. As shown in the following figure, the instruction phase is divided into a number of bit fields.

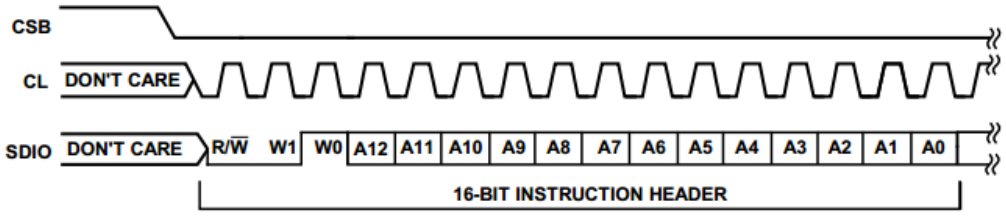



**Figure 5. Instruction Phase Bit Field**

The first bit in the stream is the read/write indicator bit (R/W). When this bit is high, a read is being requested, otherwise indicates it is a write operation.

W1 and W0 represent the number of data bytes to transfer for either read or write as shown in the following table(W1 and W0 setting table). If the number of bytes to transfer is three or less (00, 01, or 10), CSB can stall high on byte boundaries. Stalling on a non-byte boundary terminates the communications cycle. If these bits are 11, data can be transferred until CSB transitions high. CSB is not allowed to stall during the streaming process.

The remaining 13 bits represent the starting address of the data sent. If more than one word is being sent, sequential addressing is used, starting with the one specified, and it either increments (LSB first) or decrements (MSB first) based on the mode setting.



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**Table 8. W1 and W0 Settings**

| W1:W0 | Action | CSB stalling |
|---|---|---|
| 00 | 1 byte of data can be transferred. | Optional |
| 01 | 2 bytes of data can be transferred. | Optional |
| 10 | 3 bytes of data can be transferred. | Optional |
| 11 | 4 or more bytes of data can be transferred. CSB must be held low for entire sequence; otherwise, the cycle is terminated. | No |

Data follows the instruction phase. The amount of data sent is determined by the word length (Bit W0 and Bit W1). This can be one or more bytes of data. All data is composed of 8-bit words.

Data can be sent in either MSB-first mode or LSB-first mode (by setting 'LSB_first' bit). On power up, MSB-first mode is the default. This can be changed by programming the configuration register. In MSB-first mode, the serial exchange starts with the highest-order bit and ends with the LSB. In LSB-first mode, the order is reversed. The detail is shown in the below figure.

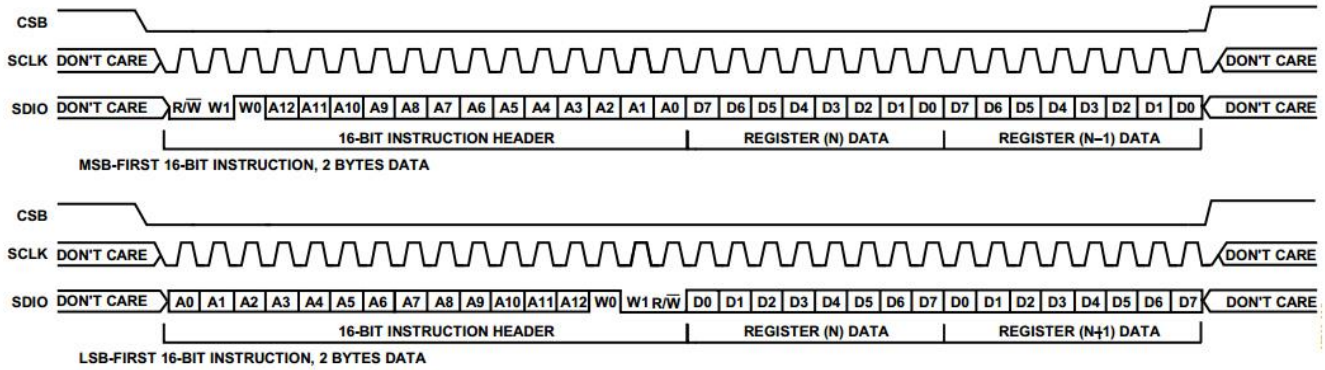



**Figure 6. MSB First and LSB First Instruction and Data Phases**

Register bit 'SDO_active' is responsible for activating SDO on devices. If this bit is cleared, then SDO is inactive and read data is routed to the SDI pin. If this bit is set, read data is placed on the SDO pin. The default for this bit is low, making SDO inactive.

# 3.2.2.I2C Operation

I2C bus uses SCL and SDA as signal lines. Both lines are connected to VDDIO externally via pull-up resistors so that they are pulled high when the bus is free. The I2C device address of da213 is shown below. The LSB bit of the 7bits device address is configured via SA0 pin.

**Table 9. I2C Address**

| SAD6 | SAD5 | SAD4 | SAD3 | SAD2 | SAD1 | SAD0 | W/R |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 | 1 | SAO | 0/1 |

**Table 10. SAD+Read/Write Patterns**

| Command | SAD[6:1] | SAD[0]=SA0 | R/W | SAD+R/W |
|---|---|---|---|---|
| Read | 010011 | 0 | 1 | 01001101(4dh) |
| Write | 010011 | 0 | 0 | 01001100(4ch) |
| Read | 010011 | 1 | 1 | 01001111(4fh) |
| Write | 010011 | 1 | 0 | 01001110(4eh) |



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The I2C interface protocol has special bus signal conditions. Start (S), stop (P) and binary data conditions are shown below. At start condition, SCL is high and SDA has a falling edge. Then the slave address is sent. After the 7 address bits, the direction control bit R/W selects the read or write operation. When a slave device recognizes that it is being addressed, it should acknowledge by pulling SDA low in the ninth SCL (ACK) cycle.

At stop condition, SCL is also high, but SDA has a rising edge. Data must be held stable at SDA when SCL is high. Data can change value at SDA only when SCL is low.

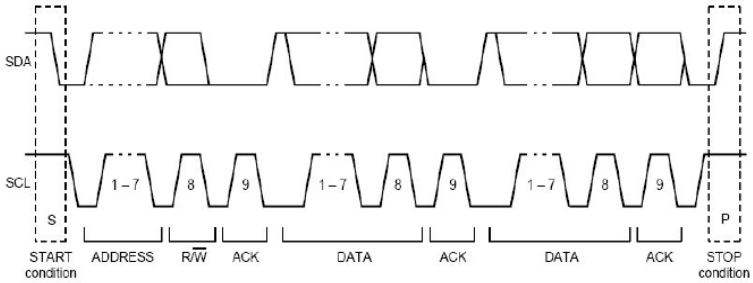



**Figure 7. I2C Protocol**

**Table 11. Transfer When Master is Writing One Byte to Slave**

| Master | S | SAD+W | | SUB | | DATA | | P |
|---|---|---|---|---|---|---|---|---|
| Slave | | | SAK | | SAK | | SAK | |

**Table 12. Transfer When Master is Writing Multiple Bytes to Slave**

| Master | S | SAD+W | | SUB | | DATA | | DATA | | P |
|---|---|---|---|---|---|---|---|---|---|---|
| Slave | | | SAK | | SAK | | SAK | | SAK | |

**Table 13. Transfer When Master is Receiving (reading) One Byte of Data From Slave**

| Master | S | SAD+W | | SUB | | SR | SAD+R | | | NMASK | P |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Slave | | | SAK | | SAK | | | SAK | DATA | | |

**Table 14. Transfer When Master is Receiving (reading) Multiple Bytes of Data From Slave**

| Master | S | SAD+W | | SUB | | SR | SAD+R | | | MAK | | MAK | | NMASK | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Slave | | | SAK | | SAK | | | SAK | DATA | | DATA | | DATA | | |

## Note：

| Symbol | Symbol explain | Symbol | Symbol explain |
|---|---|---|---|
| SAD | slave address | SAK | slave acknowledge |
| W | write | MAK | master acknowledge |
| R | read | NMASK | no master acknowledge |
| S | start | SUB | Sub-address(register address) |
| P | stop | DATA | Read or write data |
| SR | start | | |



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# 4. Functionality

## 4.1. Functionality

### 4.1.1. Power Mode

The df220 has three different power modes. Besides normal mode, which represents the fully operational state of the device, there are two special energy saving modes: low-power mode and suspend mode.

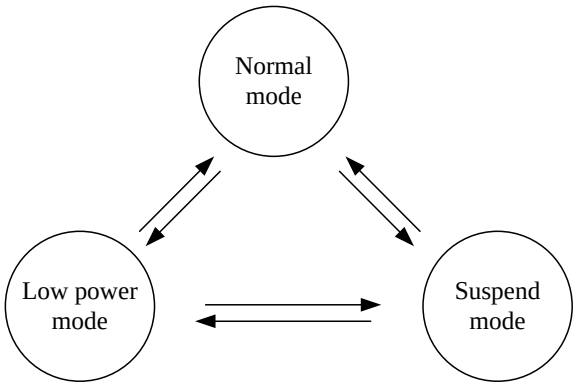



**Figure 8. Power Mode**

In normal mode, all parts of the electronic circuit are held powered-up and data acquisition is performed continuously.
In suspend mode, the whole analog part, including the oscillator, Ana LDO, Dig LDO and Drive Buffer are all powered down, no data acquisition is performed and the only supported operation is to read/write the registers. Suspend mode is entered by writing '11' or '10' to the (0x11) 'pwr_mode' bits.

In low power mode, the device is periodically switching between a sleep phase and a wake-up phase. The wake-up phase essentially corresponding to operation in normal mode with complete power-up of the circuitry. During the sleep phase the analog part except the oscillator is powered down.

During the wake-up phase, if a enabled interrupt is detected, the device stays in the wake-up phase as long as the interrupt condition endures (non-latched interrupt), or until the latch time expires (temporary interrupt), or until the interrupt is reset (latched interrupt). If no interrupt detected, the device enters the sleep phase.

### 4.1.2. Sensor Data

The width of acceleration data is 14bits given in two's complement representation. The 14bits for touch force data are split into an MSB part (one byte containing bits 13 to 6) and an LSB lower part (one byte containing bits 5 to 0)



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### 4.1.3.Factory Calibration

The IC is factory calibrated for offset and sensitivity. The trimming values are stored inside the chip's nonvolatile memory. The trimming parameters are loaded to registers while df220 reset (POR or software reset). This allows using the device without further calibration.

### 4.1.4.Smart Sensitivity Learning

This function can be applied to the stylus, so that the user can re-calibrate the sensor sensitivity according to the actual pressure value to obtain a better user experience.

## 4.2. Interrupt Controller

Interrupt engines are integrated in the df220. Each interrupt can be independently enabled and configured. If the condition of an enabled interrupt is fulfilled, the corresponding status bit is set to 1 and the selected interrupt pin is activated. There are two interrupt pins, INT1 and INT2; interrupts can be freely mapped to any of these two pins. The pin state is a logic 'or' combination of all mapped interrupts.

### 4.2.1.General Features

An interrupt is cleared depending on the selected interrupt mode, which is common to all interrupts. There are three different interrupt modes: non-latched, latched and temporary. The mode is selected by the 'latch_int' bits according to the following table.

**Table 15. Interrupt Mode Selection**

| latch_int1/2 | Interrupt mode |
|---|---|
| 0000 | non-latched |
| 0001 | temporary latched 250ms |
| 0010 | temporary latched 500ms |
| 0011 | temporary latched 1s |
| 0100 | temporary latched 2s |
| 0101 | temporary latched 4s |
| 0110 | temporary latched 8s |
| 0111 | latched |
| 1000 | non-latched |
| 1001 | temporary latched 1ms |
| 1010 | temporary latched 1ms |
| 1011 | temporary latched 2ms |
| 1100 | temporary latched 25ms |
| 1101 | temporary latched 50ms |
| 1110 | temporary latched 100ms |
| 1111 | latched |



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An interrupt is generated if its activation condition is met. It can't be cleared as long as the activation condition is fulfilled. In the non-latched mode the interrupt status bit and the selected pin (INT1 or INT2) are cleared as soon as the activation condition is no more valid. Exceptions to this behavior are the new data and orientation, which are automatically reset after a fixed time.

In the latched mode an asserted interrupt status and the selected pin are cleared by writing 1 to (0x20) 'reset_int' bit. If the activation condition still holds when it is cleared, the interrupt status is asserted again with the next change of the acceleration registers.

In the temporary mode an asserted interrupt and selected pin are cleared after a defined period of time. The behavior of the different interrupt modes is shown in the following figure.

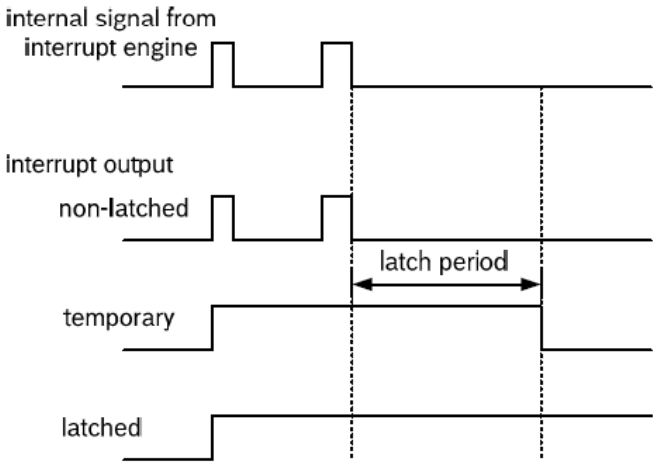



**Figure 9. Interrupt Mode**

## 4.2.2.Mapping

The mapping of interrupts to the interrupt pins is done by registers 'INT_MAP' (0x19 0x1a and 0x1b), setting *int1_inttype* (e.g. int1_freefall) to 1 can map this type of interrupt to INT1 pin and setting int2_inttyp to 1 can map this type interrupt to INT2 pin.

## 4.2.3.Electrical Behavior (INT1/INT2 to open-drive or push-pull)

Both interrupt pins can be configured to show desired electrical behavior. The active level for each pin is set by register bit int1_lvl (int2_lvl), if int1_lvl (int2_lvl) = 0 (1), then the pin INT1 (INT2) is 0 (1) active.
Also the electric type of the interrupt pin can be selected. By setting int1_od (int2_od) = 1 (0), the interrupt pin output type can be set to be open-drive (push-pull).

## 4.2.4.New Data Interrupt

This interrupt serves for synchronous reading of acceleration data. It is generated after an acceleration data was calculated. The interrupt is cleared automatically before the next acceleration data is ready.



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# 5. Application Hints

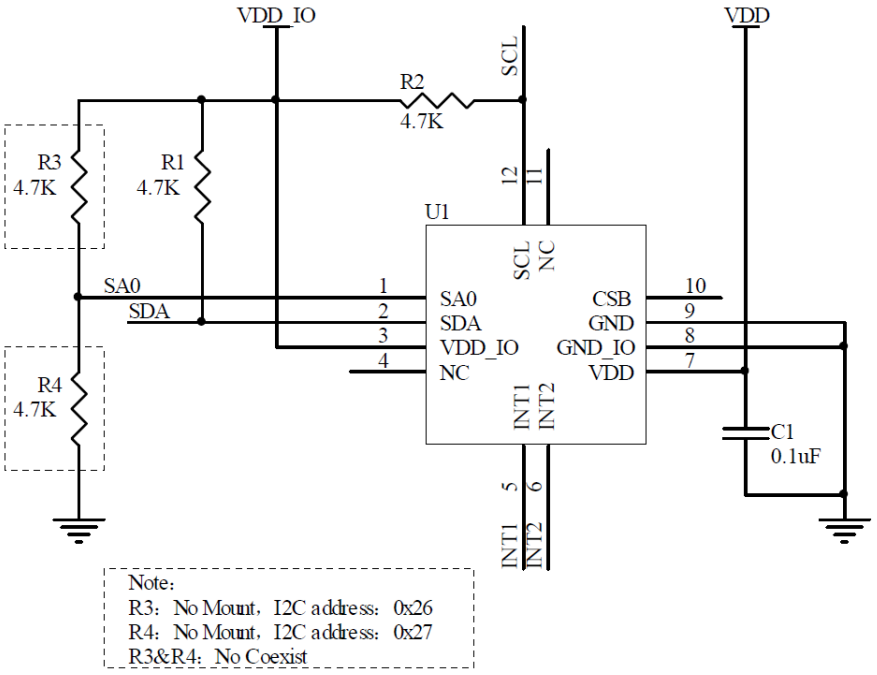



**Figure 10. df220 I2C Electrical Connect**

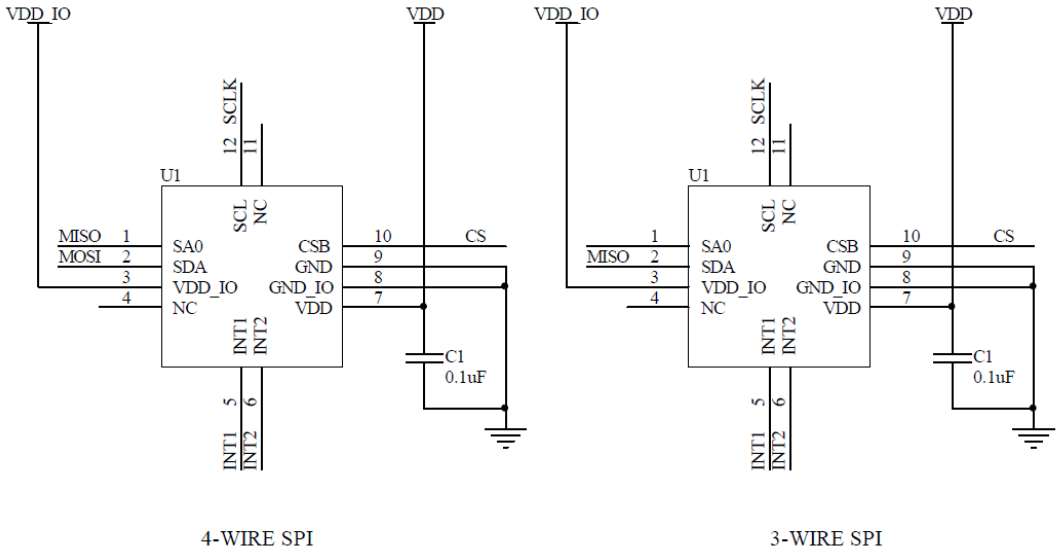



**Figure 11. df220 SPI Electrical Connect**

The device core is supplied through VDD line while the I/O pads are supplied through VDD_IO line. Power supply decoupling capacitors (100 nF ceramic) should be placed as near as possible to the pin 7 and pin 3 of the device (common design practice).

The functionality of the device and the measured acceleration data is selectable and accessible through the I2C or SPI interfaces. When using the I2C, CS must be tied high or keep NC (not connect). The functions, the threshold and the timing of the two interrupt pins (INT1 and INT2) can be completely programmed by the user through the I2C/SPI interface.



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# 6. Register Mapping

The table given below provides a listing of the 8 bit registers embedded in the device and the related addresses:

**Table 16. Register Address Map**

| Name | Type | Register address | Default | Soft Reset |
|---|---|---|---|---|
| SPI_CONFIG | RW | 0x00 | 00H | NO |
| CHIPID | R | 0x01 | 13H | NO |
| ACC_Z_LSB | R | 0x06 | 00H | YES |
| ACC_Z_MSB | R | 0x07 | 00H | YES |
| NEWDATA_FLAG | R | 0x0A | 00H | YES |
| ODR_AXIS | RW | 0x10 | 0FH | YES |
| MODE_BW | RW | 0x11 | 9EH | YES |
| INT_SET2 | RW | 0x17 | 00H | YES |
| INT_MAP2 | RW | 0x1A | 00H | YES |
| INT_CONFIG | RW | 0x20 | 05H | YES |
| INT_LATCH | RW | 0x21 | 00H | YES |



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# 7. Registers Description

## 7.1. SPI_CONFIG (00H)

**Table 17. SPI_CONFIG Register**

Default data: 0x00 Type: RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| SDO Active | LSB First | Soft Reset | Unused | Unused | Soft Reset | LSB First | SDO Active |

**Table 18. SPI_CONFIG Description**

| | |
|---|---|
| SDO Active | 0:3-wire SPI<br>1:4-wire SPI |
| LSB First | 0:MSB First<br>1:LSB First |
| Soft Reset | 1: soft reset |

## 7.2. CHIPID (01h)

**Table 19. CHIPID Register**

Default data: 0x13 Type: R

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |

## 7.3. Force_N_LSB (06H), Force_N _MSB (07H)

Force data, the value is expressed in two complement byte and are left justified.

**Table 20. Force_N _LSB Register**

Default data: 0x00 Type: R

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Unused | Unused |

**Table 21. Force_N _MSB Register**

Default data: 0x00 Type: R

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D[13] | D[12] | D[11] | D[10] | D[9] | D[8] | D[7] | D[6] |



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# 7.4. NEWDATA_FLAG (0AH)

**Table 22. NEWDATA_FLAG Register**

Default data: 0x00 Type: R

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| unused | unused | unused | unused | unused | unused | unused | new_data_int |

**Table 23. NEWDATA_FLAG Register Description**

| | |
|---|---|
| new_data_int | 0: no new_data interrupt<br>1: new_data interrupt has occurred |

# 7.5. ODR_FORCE (10H)

**Table 24. ODR_Force Register**

Default data: 0x0F Type: RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| unused | unused | Force data_disable | unused | ODR[3] | ODR[2] | ODR[1] | ODR[0] |

**Table 25. ODR_Force Register Description**

| | |
|---|---|
| Force data_disable | 0: enable force data<br>1: disable force data |
| ODR[3:0] | 0000: 1Hz (not available in normal mode)<br>0001: 1.95Hz (not available in normal mode)<br>0010: 3.9Hz<br>0011: 7.81Hz<br>0100: 15.63Hz<br>0101: 31.25Hz<br>0110: 62.5Hz<br>0111: 125Hz<br>1000: 250Hz<br>1001: 500Hz (not available in low power mode)<br>1010: 1000Hz (not available in low power mode)<br>1011-1111: 1000Hz (not available in low power mode) |



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# 7.6. MODE_BW (11H)

**Table 26. MODE_BW Register**

Default data: 0x9E Type: RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| pwr_mode [1] | pwr_mode [0] | unused | low_power_bw [3] | low_power_bw [2] | low_power_bw[1] | low_power_bw[0] | unused |

**Table 27. MODE_BW Register Description**

| | |
|---|---|
| pwr_mode[1:0] | 00: normal mode,<br>01: low power mode,<br>1x: suspend mode. |
| low_power_bw [3:0] | 0000-0010: 1.95Hz<br>0011: 3.9Hz<br>0100: 7.81Hz<br>0101: 15.63Hz<br>0110: 31.25Hz<br>0111: 62.5Hz<br>1000: 125Hz<br>1001: 250Hz<br>1010: 500Hz<br>1011-1111: 500Hz |

# 7.7. INT_SET2 (17H)

**Table 28. INT_SET2 Register**

Default data: 0x00 Type: RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| unused | unused | unused | new_data_int_en | unused | unused | unused | unused |

**Table 29. INT_SET2 Register Description**

| | |
|---|---|
| new_data_int_en | 0: disable the new data interrupt.<br>1: enable the new data interrupt. |



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# 7.8. INT_MAP2 (1AH)

**Table 30. INT_MAP2 Register**

Default data: 0x00 Type: RW

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| int2_new_data | unused | unused | unused | unused | unused | unused | unused | int1_new_data |

**Table 31. INT_MAP2 Register Description**

| | |
|---|---|
| int2_new_data | 0: doesn't mapping new data interrupt to INT2<br>1: mapping new data interrupt to INT2 |
| int1_new_data | 0: doesn't mapping new data interrupt to INT1<br>1: mapping new data interrupt to INT1 |

# 7.9. INT_CONFIG (20H)

**Table 32. INT_CONFIG Register**

Default data: 0x05 Type: RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Reset_int | unused | unused | unused | int2_od | int2_lvl | int1_od | int1_lvl |

**Table 33. INT_CONFIG Register Description**

| | |
|---|---|
| Reset_int | Write'1'to reset all latched int. |
| Int2_od | 0: select push-pull output for INT2<br>1: selects OD output for INT2 |
| Int2_lvl | 0: selects active level low for pin INT2<br>1: selects active level high for pin INT2 |
| int1_od | 0: select push-pull output for INT1<br>1: selects OD output for INT1 |
| int1_lvl | 0: selects active level low for pin INT1<br>1: selects active level high for pin INT1 |



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# 7.10. INT_LATCH (21H)

**Table 34. INT_LATCH Register**

Default data: 0x00 Type: RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| latch_int2[3] | latch_int2[2] | latch_int2[1] | latch_int2[0] | latch_int1[3] | latch_int1[2] | latch_int1[1] | latch_int1[0] |

**Table 35. INT_LATCH Register Description**

| | |
|---|---|
| latch_int2[3:0] | 0000: non-latched<br>0001: temporary latched 250ms<br>0010: temporary latched 500ms<br>0011: temporary latched 1s<br>0100: temporary latched 2s<br>0101: temporary latched 4s<br>0110: temporary latched 8s<br>0111: latched<br>1000: non-latched<br>1001: temporary latched 1ms<br>1010: temporary latched 1ms<br>1011: temporary latched 2ms<br>1100: temporary latched 25ms<br>1101: temporary latched 50ms<br>1110: temporary latched 100ms<br>1111: latched |
| latch_int1[3:0] | 0000: non-latched<br>0001: temporary latched 250ms<br>0010: temporary latched 500ms<br>0011: temporary latched 1s<br>0100: temporary latched 2s<br>0101: temporary latched 4s<br>0110: temporary latched 8s<br>0111: latched<br>1000: non-latched<br>1001: temporary latched 1ms<br>1010: temporary latched 1ms<br>1011: temporary latched 2ms<br>1100: temporary latched 25ms<br>1101: temporary latched 50ms<br>1110: temporary latched 100ms<br>1111: latched |

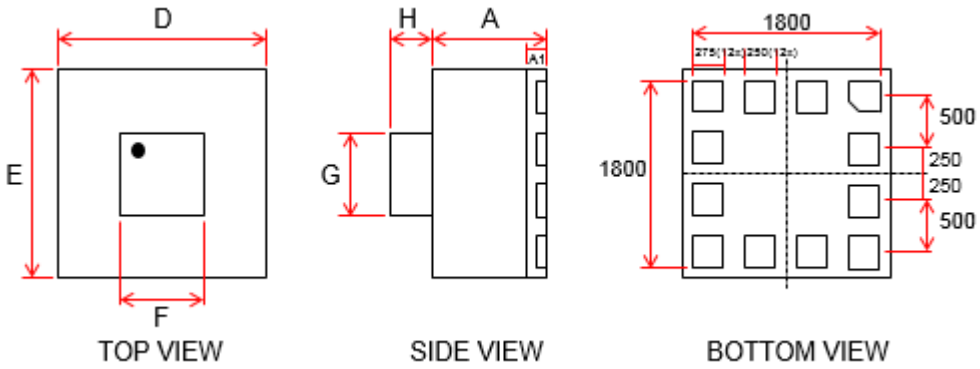


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# 8. Package Information

## 8.1. Outline Dimensions

The sensor housing is a standard LGA package. Its dimensions are the following.




| COMMON DIMENSIONS(um) | | | |
|---|---|---|---|
| PKG | NA | | |
| REF | MIN | NOM | MAX |
| A | 1000 | 1100 | 1200 |
| A1 | 200 REF | | |
| D | 1900 | 2000 | 2100 |
| E | 1900 | 2000 | 2100 |
| F | | 800 | |
| G | | 800 | |
| H | | 400 | |

**Figure 12. 12Pin LGA Mechanical Data and Package Dimensions**



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# 8.2. Assembly Considerations

The df220 sensor is configured to accept a normal load force applied directly to the top of the sensor. The styles or actuator assembly contact area must larger than touch force sensor top contact area (0.8x0.8mm) with the consideration of assembly tolerance.

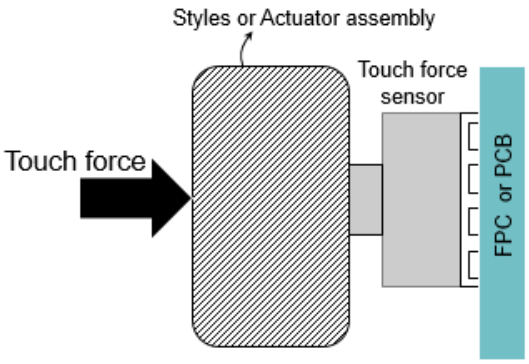



**Figure 13. Side View Force Load**



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# 8.3. Tape and Reel Specification

The df220 is shipped in a standard pizza box

The box dimension for 1 reel is: L x W x H = 35cm x 35cm x 5cm

df220 quantity: 5000pcs per reel, please handle with care.

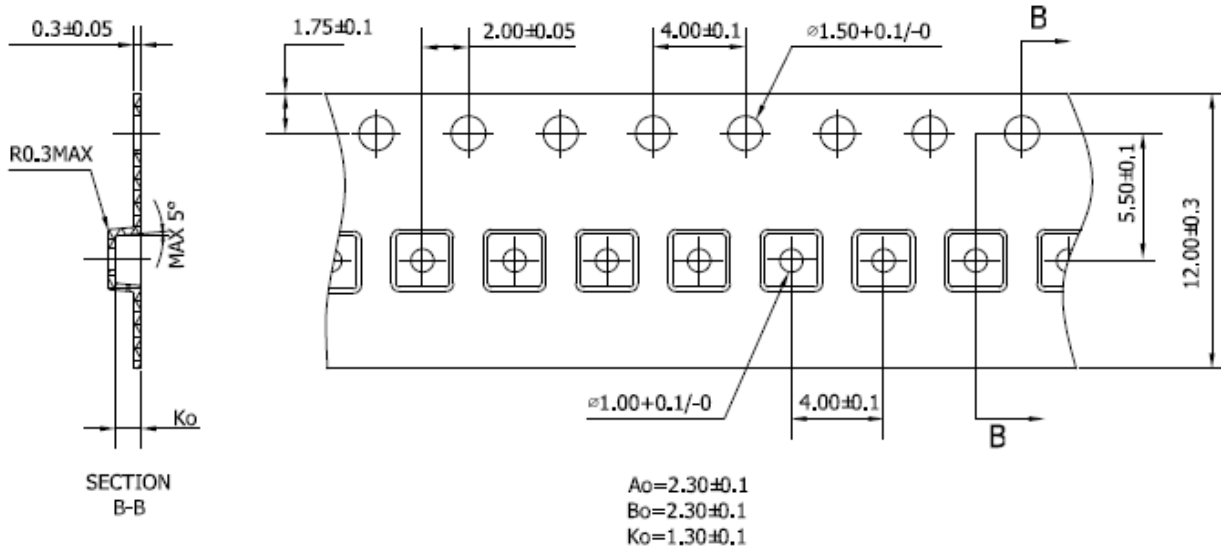



**Figure 14. Tape and Reel Dimension In mm**



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# 9. Revision History

**Table 36. Document Revision History**

| Date | Revision | Changes |
|---|---|---|
| 19-Dec.-2017 | 1.0 | Initial release |
| | | |
| | | |
| | | |
| | | |
| | | |



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