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IST8315-L
3D Magnetometer

Datasheet

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1. General Description

iSentek IST8315-L is a 3-axis digital magnetometer with a 1.6 x 1.6 x 1.0 mm^3, 12-pin LGA package. It is an integrated chip with 3-axis magnetic sensors, digital control logic, a built-in temperature compensation circuit, and self-testing function. IST8315-L provides an I^2C digital output with fast mode up to 400 kHz. Its ultra-high output data rate, ultra-low noise, ultra-low hysteresis and excellent temperature drift performance features make it a perfect candidate for applications requiring high speed and high precision.

Features

- Single-chip 3-axis magnetic sensor
- 1.6 x 1.6 x 1.0 mm^3, 12-pin LGA package
- I^2C slave, Fast Mode up to 400 kHz
- 14-bit data output
- Built-in FIFO with 32 depths for each axis
- Ultra-high output data rate with a maximum value of 1000 Hz
- Dynamic range of ±1000 uT.
- Ultra-low hysteresis (< 0.1 %FS)
- Ultra-low sensitivity temperature drift (±0.025 %/°C)
- Ultra-low offset temperature drift (0.016 uT/°C)
- High precision temperature compensation
- Wide operating temperature range
- Built-in self-test function
- Built-in noise suppression filter
- Software and algorithm support are available (for tilt compensation, soft/hard-iron calibration)
- RoHS, HF and TSCA compliant

Applications

- Augmented/Virtual Reality Applications
- Quadcopter/Drone Applications
- Navigation Applications
- Industrial Applications
- Magnetometry
- IoT devices
- Heading
- Gaming

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2. Block Diagram, Package Dimension and Application Circuit

2.1. Block diagram

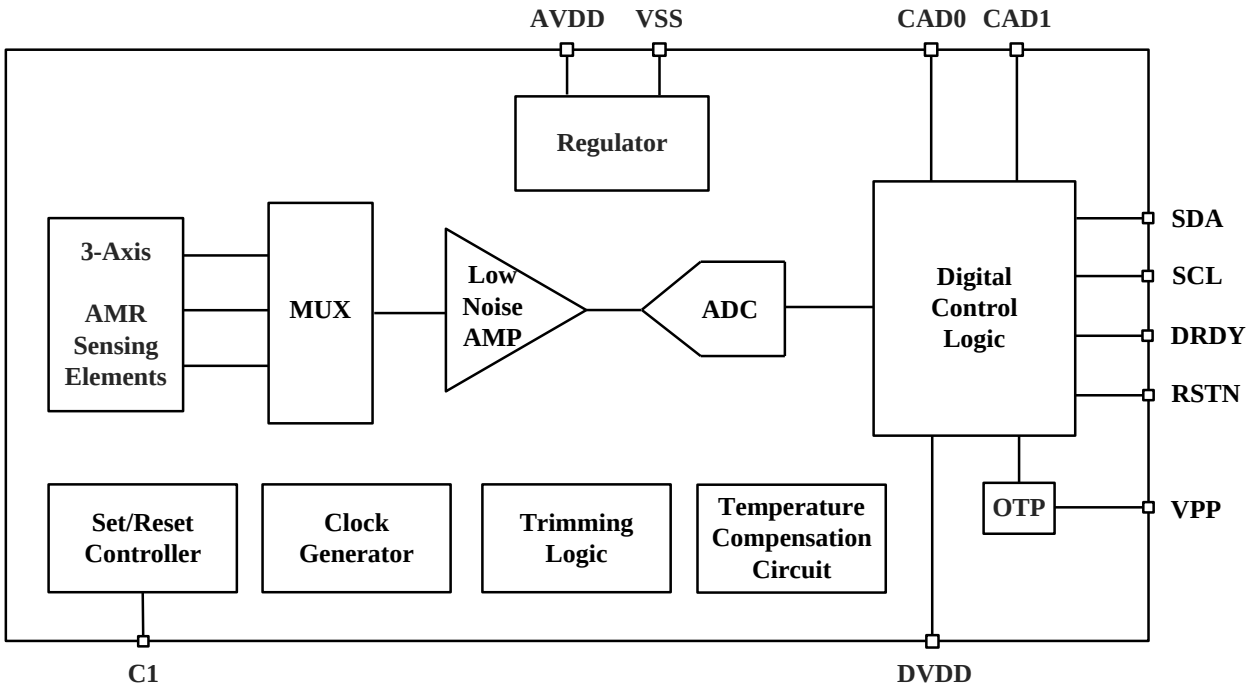


Figure 1. Block Diagram

2.2. Package Dimensions

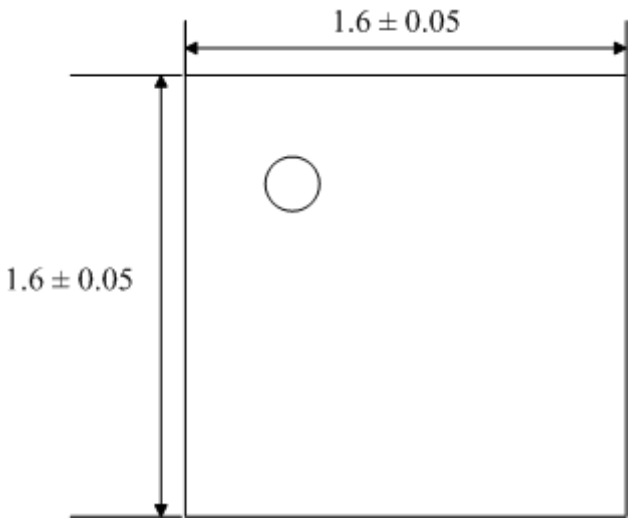


Figure 2. IST8315-L Top View

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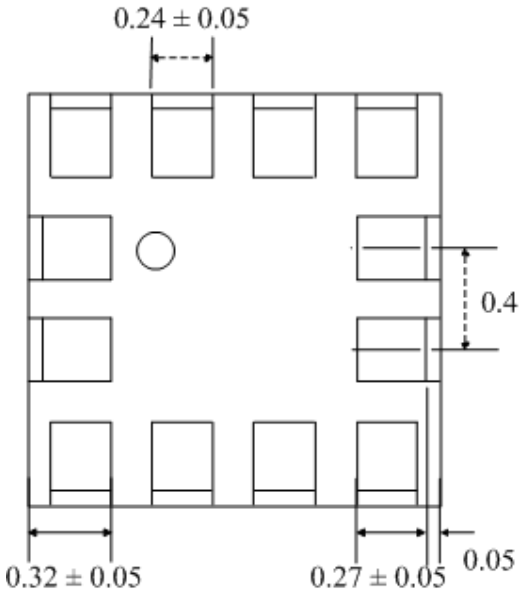
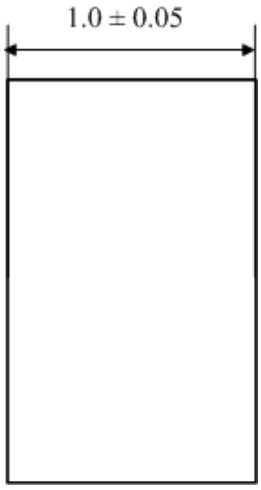


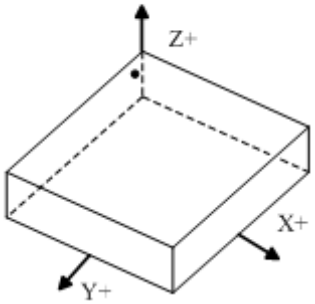
Figure 3. IST8315-L Bottom View



Unit: mm

Figure 4. IST8315-L Side View

IST8315-L 3D Top View



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2.3. Application Circuits and Pin Descriptions

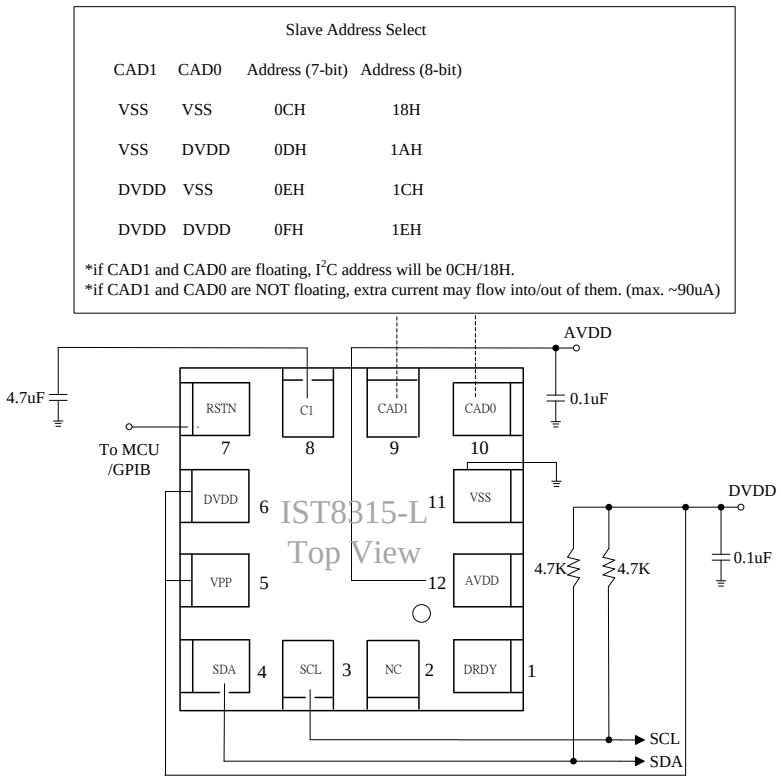


Figure 5. IST8315-L Application Circuit

Pin[*1]	Name	Function
1	DRDY	Data ready
2	NC	Not use
3	SCL	I²C serial clock
4	SDA	I²C serial data
5	VPP	Test pin, connect to DVDD or keep floating[*2]
6	DVDD	Digital supply voltage, 1.72 ~ 3.6 V
7	RSTN	Reset
8	C1	Set/Reset function
9	CAD1	I²C slave address select, internally pulled to “high” by default
10	CAD0	I²C slave address select, internally pulled to “low” by default
11	VSS	GND
12	AVDD	Analog supply voltage, 2.4 ~ 3.6 V

[*1] Please refer to Figure 2 on page 7.

[*2] Please keep CAD1 floating if VPP is floating.

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3. Operational Modes and Functional Descriptions

3.1. Operation modes

IST8315-L has following operation modes:

(1) Standby Mode

(2) Suspend Mode

(3) Single Measurement Mode

(4) Continuous Measurement Mode

(5) Self-test Mode

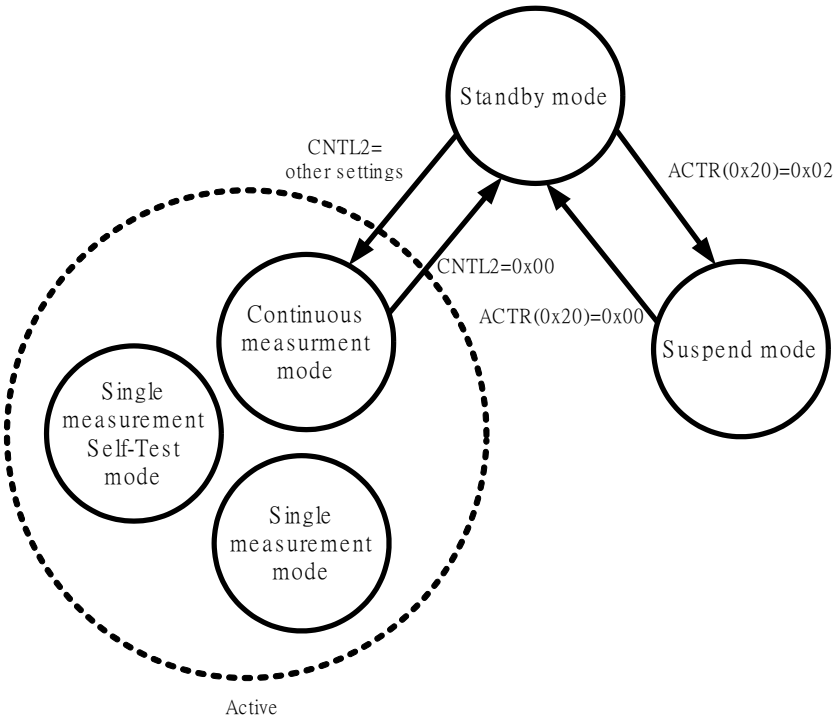


Figure 6. Operation Modes

3.1.1. Standby Mode

The initial mode (after power on) of IST8315-L is Standby Mode. In Standby Mode, all internal circuits are off (except oscillator and regulator) and all registers are accessible. The latest state of data saved in Read/Write registers is maintained. Registers can be reset by soft reset or hard reset (through RSTN pin).

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3.1.2. Suspend Mode

When Suspend Mode is set through ACTR(0x20), all circuits except those I^2C related will be turned off. This is a mode with extremely low power consumption (2 μA). Users are encouraged to use this mode when the system does not require e-compass data. Users must first enter Standby Mode before using additional modes.

3.1.3. Single Measurement Mode

In Single Measurement Mode, measured data are saved in data registers before IST8315-L automatically transitions to Standby Mode. When entering Standby Mode, Control Register 1(CNTL2[3:0]) is set to "0000". Simultaneously, DRDY bit in STAT1 register turns to "1". This is called "data ready". When any of the measurement data registers or STAT1 register is read, DRDY bit turns to "0". For the next measurement, user must set Control Register 1(CNTL2[3:0]) to "0001" again.

3.1.4. Continuous Measurement Mode

When Continuous Measurement Mode is set, the sensor is measured periodically at preset frequencies. The measured data is stored in Output Data Registers. When the next measurement time comes, IST8315-L automatically resumes measuring and the Output Data Registers will be updated.

3.1.5. Self-Test Mode

Self-Test mode is used to ensure that the IC functioning normally. One time measuring in Self-Test Mode can be done by setting the Self-Test Register (STR[6:0]) to "1000000". When the magnetic environment remains unchanged, this measurement result can be compared to the results of other measurement modes. If all 3-axis outputs have different polarities, the IC is functioning properly.

3.2. FIFO

IST8315-L has a built-in FIFO with 32 depths for each axis.

The FIFO function is enabled by setting FF_MODE (bit-7 of the CNTL2 register) to "1"; this applies to both Single Measurement Mode and Continuous Measurement Mode. When FIFO function is enabled, the measured 3-axis output data (from register DATAXL to register DATAZH) are stored as a group of data in the buffer. The FIFO contains 32 groups of data in total.

When reading out data from the FIFO, it should always start with register DATAXL and finish with

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register DATAZH. By accessing register DATAXL, the oldest data group in the FIFO will be read first in accordance with the FIFO operating principle (first-in first-out). Accessing register DATAZH is considered the end of reading out one group of data, after which the second-oldest group of data in the FIFO is transferred to the output data registers to be read. Simultaneously, the oldest group of data in the FIFO is discarded. If register DATAZH is not read, the output data register and FIFO remain unmodified.

The DRDY bit and DOR bit in register STAT1 behave differently when the FIFO function is enabled. If the number of data groups stored in the FIFO is equal to or more than the Watermark, DRDY bit turns to “active” (the definition of “active” can be set through DRP, bit 2 of the CNTL3 register). If a group of new data is measured when the FIFO is full, the DOR bit turns to “1”. By reading one data group from the FIFO, DOR immediately changes to “0”.

If any of the 3-axis output data registers are accessed when the FIFO function is enabled and FIFO is empty, INV (bit 2 of register STAT2) will become “1” and the data read will be 7FFFh. If a group of new data is measured, INV bit immediately changes to “0”. When IST8315-L is reset, FIFO buffer is cleared.

3.2.1. Watermark

When FIFO function is enabled, the watermark function is available. Watermark level threshold can be set via CNTL1[4:0], which can only be configured in Standby Mode. If the number of data groups stored in the FIFO equals or exceeds Watermark, DRDY bit turns to “active”.

3.2.2. DRDY Function

When FIFO function is disabled, DRDY function is used when the output data is updated. The DRDY pin is responsible for monitoring the data ready output. After reading data from the output register, DRDY is set to low (the DRP bit is assumed to be "1" by default). FIFO function is enabled, DRDY function indicates if the number of data groups stored in FIFO is equal to or greater than Watermark (see 3.2.1 for more details).

3.2.3. IST8315-L Read Process

(1) Read STAT1 register:

- Polling STAT1 register bit 0

  ❖ *DRDY: Data ready bit*

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i. When FIFO is disabled (CNTL2[7] = "0") and DRP is in default setting:

- DRDY turns to "1" when data is ready.

- DRDY turns to "0" when any of the 3-axis output data registers (from register DATAXL to register DATAZH) are accessed.

ii. When FIFO is enabled (CNTL2[7] = "1") and DRP is in default setting:

- If the number of data groups stored in the FIFO is equal to or more than Watermark (CNTL1[4:0]), DRDY bit turns to "1". If the number of data groups stored in the FIFO is less than Watermark, DRDY bit turns to "0".

❖ *DOR: Data overrun bit*

i. When FIFO is disabled (CNTL2[7] = "0"):

- DOR turns to "0" if no data have been skipped since last read

- DOR turns to "1" if data have been skipped since last read

ii. When FIFO is enabled (CNTL2[7] = "1"):

- When a new data is measured while FIFO is full, DOR turns to "1". If a data group is read, DOR bit turns to "0" automatically.

(2) Read Measurement Data:

Read Register 0x11h ~ 0x16h for X, Y and Z axis data.

i. When FIFO is disabled (CNTL2[7] = "0") and DRP is in default setting:

When data reading starts, DRDY bit and DOR bit turn to "0".

ii. When FIFO is enabled (CNTL2[7] = "1"):

When reading out data from the FIFO, it should always start with register DATAXL and finish with register DATAZH. By accessing register DATAXL, the oldest data group in the FIFO will be read first in accordance with the FIFO operating principle (first-in first-out). Accessing register DATAZH is considered the end of reading out one group of data, after which the second oldest group of data in the FIFO is transferred to the output data registers to be read. Simultaneously, the oldest group of data in the FIFO is discarded. If register DATAZH is not read, the output data register and FIFO remain unmodified.

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4. Electrical Specifications

4.1. Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
Storage Temperature	TSTG	-40 to +150	°C
Analog Supply Voltage	AVDD	-0.5 to +3.6	V
Digital Supply Voltage	DVDD	-0.5 to +3.6	V
Digital Input Voltage	VIN	-0.3 to DVDD+0.3	V
Electrostatic Discharge Voltage*[1]	VESD_HBM	-4000 to 4000	V
Electrostatic Discharge Voltage*[2]	VESD_MM	-300 to 300	V
Electrostatic Discharge Voltage*[3]	VESD_CDM	-700 to 700	V
Reflow Classification	JESD22-A113 with 260 °C Peak Temperature		

1. Human Body Model (HBM)

2. Machine Model (MM)

3. Charge Device Model (CDM)

4.2. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Temperature	TA	-40		+85	°C
Analog Supply Voltage	AVDD	2.4	3.3	3.6	V
Digital Supply Voltage	DVDD	1.72	1.8	3.6	V

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4.3. Electrical Specifications

(Operating conditions: TA = +25 °C; AVDD = 2.5 V; DVDD = 1.8 V; 4.7 µF ceramic capacitors tied to C1 pin with maximum allowed line width and 5 mm distance.)

Parameter	Symbol	Conditions	Min.	Typ.	Max	Unit
Operating Current	IDD3A	Full operation with OSR*[1]=1 setting, at 10 sps 20 sps 50 sps 100 sps 200 sps 333 sps 500 sps 1000 sps		 100 200 400 750 1450 2350 3450 6900		uA
Suspend Current	ISPD			2		uA
Output Data Rate (ODR)	ODR				1000*[2]	Hz
Over Sampling Rate*[1]	OSR		1		32	
Input Low Voltage	VIL		0		DVDD *30 %	V
Input High Voltage	VIH		DVDD *70 %		DVDD	V
Output Low Voltage	VOL	IOL = +4 mA	0		DVDD *20 %	V
Output High Voltage	VOH	IOH = -100 uA (Except SCL and SDA)	DVDD *80%		DVDD	V

1. Register OSRCNTL(0x41) controls OSR setting.

2. 1000Hz ODR can be achieved with OSR = 1.

4.4. Magnetic Sensor Specifications

(Operating conditions: TA = +25 °C; AVDD = 2.5 V; DVDD = 1.8 V; 4.7 µF ceramic capacitors tied to C1 pin with maximum allowed line width and 5 mm distance.)

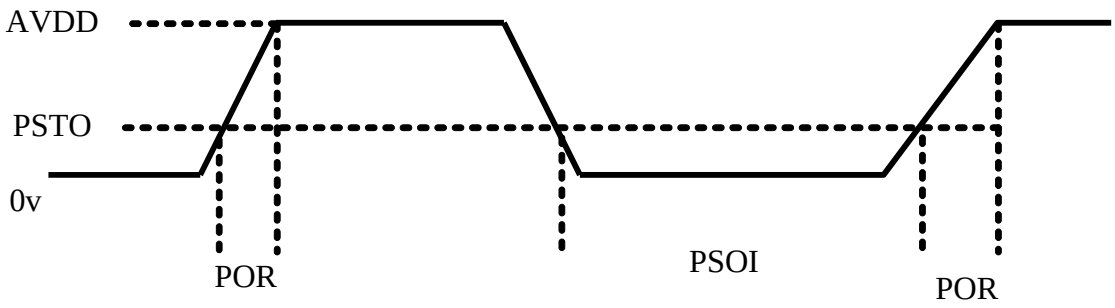
Parameter	Symbol	Condition	Min.	Typ.	Max	Unit
Dynamic Range	DR	TA = 25 °C		±1000		uT
Linearity	LIN			0.5		%FS
Resolution	RES			0.3		uT/LSB
Sensitivity	SEN			3.3		LSB/uT
Zero Gauss Offset	ZGD			±0.3		uT
Hysteresis	HS			0.1		%FS
Sensitivity Temperature Drift	TD_S	-40 ~ 85 °C		±0.025		%/°C

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Zero-B Offset Temperature Drift	TD_O	-40 ~ 85 °C		0.016		uT/°C

4.5. Power On Reset (POR) Specifications



PSTO: Power Supply Turn Off voltage
PSOI: Power Supply Turn Off Interval
POR: Power On Reset

PSTO: max=0.7volt
PSOI: min=10ms
POR: max:50ms

When POR circuit detects a rise of AVDD voltage, it resets all internal circuits and initializes all registers. After reset, IST8315-L transits to Standby mode.

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5. Technology Overview

5.1. AMR Technology

iSentek's patented magnetometer IST8315-L is designed using Anisotropy Magnetoresistance (AMR) technology. The output is generated by the change in resistance of the AMR resistors as the external magnetic field varies. The sensitivity is approximately 50 to 200 times greater than conventional Hall elements. The high sensitivity allows a higher output data rate (ODR), lower noise, and lower power consumption.

5.2. High Reliability Planarized Structure Design

IST8315-L consists of three full Wheatstone Bridges of AMR resistors. The three bridges detecting magnetic components in orthogonal directions are wire-bonded to a control ASIC on a single chip. This planarized structural design offers exceptional thermal shock stability, making our device extremely reliable, whereas other known AMR magnetometers with z-axis sensors placed vertically on the substrate employing 90-degree flip-chip packaging suffer from reliability issues.

5.3. Ultra-low Hysteresis Design

iSentek has developed a specialized high permeability (μ) material for magnetic field detection. This high-μ material has ultra-low residual magnetization below 0.1 %FS in the field range as large as ±500 G. The ultra-low hysteresis design prevents the magnetometer from experiencing dynamic offset after encountering a strong external magnetic field impact; that is, the angular accuracy is restored automatically without calibration after the removal of the interference field. This feature fulfills the requirements for applications when real-time calibration is unavailable. No calibration is required in general conditions.

5.4. Magnetic Setting Mechanism

AMR sensing resistors consist of permalloy thin film and metallization. Permalloy is a soft magnetic material. Irreversible magnetic rotation may occur when the strength of external magnetic field exceeds half of the anisotropy field of the sensing resistor, resulting in angular error induced by offset. To solve this issue, a magnetic setting mechanism has been introduced in IST8315-L. A magnetic field is generated within IST8315-L to align the magnetization of AMR sensing resistors before every measurement. This auto-zeroing mechanism ensures the stability of the IST8315-L's angular accuracy throughout the operation.

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6. Digital Interface and Registers

6.1. I²C Interface

The interface of IST8315-L follows the standard I²C definition guidelines with some additional protocol definitions. IST8315-L supports standard speed (100 kHz) and fast speed (400 kHz). Pull-up resistors of 4.7 kΩ for both SDA and SCL lines should be used.

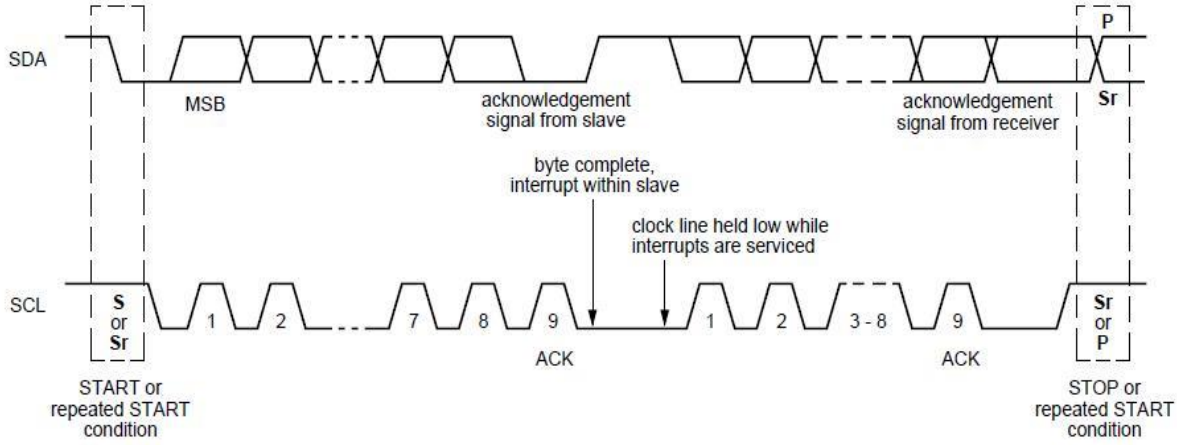


Figure 7. I²C Operation

Slave Address:

MSB LSB

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	1	1	selectable	selectable	R/W

IST8315-L has 4 different I²C slave addresses, which can be chosen through Pin 5 (CAD0) and Pin 6 (CAD1), the corresponding 7-bit and 8-bit defined I²C slave addresses are listed below:

CAD1	CAD0	I²C Slave Address (7-bit)	I²C Slave Address (8-bit)
VSS	VSS	0CH	18H
VSS	DVDD	0DH	1AH
DVDD	VSS	0EH	1CH
DVDD	DVDD	0FH	1EH
Floating (default)	Floating (default)	0CH	18H

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6.2. I²C Read Operation

Single Byte Read:

SA	Slave Address+ RW	ACK	Reg Address	ACK	SP	Slave Address+RW	ACK	DATA	NA	ST

I²C Single Byte Read Operation

ACK: Acknowledge, NA: Not Acknowledge, SA: START Condition, SP: Repeat Start Condition, ST: STOP Condition

■: Slave to Master □: Master to Slave

Multiple Byte Read:

SA	Slave Address+ RW	ACK	Reg Address	ACK	SP	Slave Address+RW	ACK	DATA	ACK	DATA	NA	ST

I²C Multiple Byte Read Operation

ACK: Acknowledge, NA: Not Acknowledge, SA: START Condition, SP: Repeat Start Condition, ST: STOP Condition

■: Slave to Master □: Master to Slave

6.3. I²C Write Operation

Single Byte Write:

SA	Slave Address +RW	ACK	Reg Address	ACK	DATA	ACK	ST

I²C Single Byte Write Operation

ACK: Acknowledge, NA: Not Acknowledge, SA: START Condition, SP: Repeat Start Condition, ST: STOP Condition

■: Slave to Master □: Master to Slave

Multiple Byte Write:

SA	Slave Address +RW	ACK	Reg Adderss	ACK	DATA	ACK	DATA	NA	ST

I²C Multiple Byte Write Operation

ACK: Acknowledge, NA: Not Acknowledge, SA: START Condition, SP: Repeat Start Condition, ST: STOP Condition

■: Slave to Master □: Master to Slave

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6.4. Registers

6.4.1. Customer Defined Registers

Register name	Typ	I²C Addr	Size (bit)	Info
Who Am I	R	00h	8	Device ID
Self-Test Register	R/W	0Ch	8	For self-test mode
Status Register 1	R	10h	8	Data status information
DATAXL	R	11h	8	Low byte of X-axis data
DATAXH	R	12h	8	High byte of X-axis data
DATAYL	R	13h	8	Low byte of Y-axis data
DATAYH	R	14h	8	High byte of Y-axis data
DATAZL	R	15h	8	Low byte of Z-axis data
DATAZH	R	16h	8	High byte of Z-axis data
Status Register 2	R	18h	8	Data status information
Action Register	R/W	20h	8	Suspend Mode control
Control Setting Register 1	R/W	30h	8	Chip control settings 1
Control Setting Register 2	R/W	31h	8	Chip control settings 2
Control Setting Register 3	R/W	32h	8	Chip control settings 3
Over-Sampling Ratio Control Register	R/W	41h	8	Oversampling ratio setting

6.4.2. Who Am I Register

This register provides device ID information

WAI (0x00)			
Bit	Description	Attr	Default
7:0	Device ID	R	0x15h

6.4.3. Self-Test Register

STR (0x0C)			
Bit	Description	Attr	Default
7	Reserved		
6	SELF_TEST : When this bit set to 1, chip enters self-test mode	R/W	0
5:0	Reserved		

6.4.4. Status Register 1

This register provides status information

STAT1 (0x10)			
Bit	Description	Attr	Default
7:2	Reserved		
1	DOR: Data overrun bit i. When FIFO is disabled (CNTL2[7] = "0"): - DOR turns to "0" if no data have been skipped since last read	R	0

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	- DOR turns to “1” if data have been skipped since last read ii. When FIFO is enabled (CNTL2[7] = “1”): - When a new data is measured while FIFO is full, DOR turns to “1”. If a data group is read, DOR bit turns to “0” automatically.		
0	DRDY: Data ready bit i. When FIFO is disabled (CNTL2[7] = “0”) and DRP is in default setting: - DRDY turns to “1” when data is ready. - DRDY turns to “0” when any of the 3-axis output data registers (from register DATAXL to DATAZH) are accessed. ii. When FIFO is enabled (CNTL2[7] = “1”) and DRP is in default setting: - If the number of data groups stored in the FIFO is equal to or more than Watermark (CNTL1[4:0]), DRDY bit turns to “1”. If the number of data groups stored in the FIFO is less than Watermark, DRDY bit turns to “0”. This status bit follows physical signal appearance, except the polarity control (refer to DRP bit in CNTL3 register) If data ready function enable bit is not set (refer to DREN bit in CNTL3 register), this bit remains at zero.	R	0

6.4.5. Output Data Registers

The Output Data Registers (from 0x11h ~ 0x16h) contain X, Y and Z axis measurement data.

Measurement data are stored in 2’s complement format.

DATAXL(0x11)			
Bit	Description	Attr	Default
7:0	Low Byte of X-axis data	R	0

DATAXH(0x12)			
Bit	Description	Attr	Default
7:0	High Byte of X-axis data	R	0

DATAYL(0x13)			
Bit	Description	Attr	Default
7:0	Low Byte of Y-axis data	R	0

DATAYH(0x14)			
Bit	Description	Attr	Default
7:0	High Byte of Y-axis data	R	0

DATAZL(0x15)			
Bit	Description	Attr	Default
7:0	Low Byte of Z-axis data	R	0

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DATAZH(0x16)			
Bit	Description	Attr	Default
7:0	High Byte of Z-axis data	R	0

6.4.6. Status Register 2

This register provides status information

STAT2 (0x18)			
Bit	Description	Attr	Default
7:3	Reserved		
2	INV bit: When FIFO function is enabled and FIFO is empty, if any of the 3-axis output data registers is accessed, INV bit will turn to “1” and the data read will be 7FFFh. If a group of new data is measured, INV bit turns to “0” automatically.	R	0
1:0	Reserved		

6.4.7. Action Register

This register controls the entrance and exit of Suspend Mode.

ACTR (0x20)			
Bit	Description	Attr	Default
7:2	Reserved		
1	SUSPEND_EN: When this bit is “1”, the chip will enter Suspend Mode. When IST8315-L is in Suspend Mode, only this register can be accessed by I^2C master, all other registers cannot be read or written.	R/W	0
0	Reserved		

6.4.8. Control Setting Register 1

This Register controls the settings of Noise Suppression Filter. “High” setting leads to lowest noise.

CNTL1(0x30)			
Bit	Description	Attr	Default
7	Reserved		
6:5	NSF[1:0]: Noise Suppression Filter setting Output data from magnetic sensor is filtered to suppress the noise according to this setting. 2’b00: Disable 2’b01: Low 2’b10: Middle 2’b11: High	R/W	0
4:0	WMT[4:0]: Watermark level threshold setting, functions when FIFO is enabled. Watermark level can be set every 1 step. The upper limit of watermark level is 32 steps (WMT [4:0] bits = 11111). It is prohibited to change WMT [4:0] bits in any other modes than Standby Mode.	R/W	0x0Fh

5’d0	5’d1	5’d2	5’d3
1 Steps	2 Steps	3 Steps	4 Steps

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	5'd4	**5'd5**	**5'd6**	**5'd7**		
	5 Steps	6 Steps	7 Steps	8 Steps		
	5'd8	**5'd9**	**5'd10**	**5'd11**		
	9 Steps	10 Steps	11 Steps	12 Steps		
	5'd12	**5'd13**	**5'd14**	**5'd15**		
	13 Steps	14 Steps	15 Steps	16 Steps		
	5'd16	**5'd17**	**5'd18**	**5'd19**		
	17 Steps	18 Steps	19 Steps	20 Steps		
	5'd20	**5'd21**	**5'd22**	**5'd23**		
	21 Steps	22 Steps	23 Steps	24 Steps		
	5'd24	**5'd25**	**5'd26**	**5'd27**		
	25 Steps	26 Steps	27 Steps	28 Steps		
	5'd28	**5'd29**	**5'd30**	**5'd31**		
	29 Steps	30 Steps	31 Steps	32 Steps		

6.4.9. Control Setting Register 2

This Register controls and adjusts the operation modes.

CNTL2(0x31)			
Bit	Description	Attr	Default
7	FF_MODE 1'b0: FIFO disable 1'b1: FIFO enable	R/W	0
6:5	Reserved		
4:0	MODE [4:0]: Operation mode setting 5'h00: Standby mode 5'h01: Single Measurement Mode (maximum ODR = 1000 Hz) 5'h02: Continuous Measurement Mode with ODR = 10 Hz 5'h04: Continuous Measurement Mode with ODR = 20 Hz 5'h06: Continuous Measurement Mode with ODR = 50 Hz 5'h08: Continuous Measurement Mode with ODR = 100 Hz 5'h0A: Continuous Measurement Mode with ODR = 200 Hz 5'h0B: Continuous Measurement Mode with ODR = 8 Hz 5'h0C: Continuous Measurement Mode with ODR = 1 Hz 5'h0D: Continuous Measurement Mode with ODR = 0.5 Hz 5'h10: Single Measurement Self-test Mode 5'h11: Continuous Measurement Mode with ODR = 333 Hz 5'h12: Continuous Measurement Mode with ODR = 500 Hz 5'h13: Continuous Measurement Mode with no-sleep measurement Others: Reserved	R/W	0

6.4.10. Control Setting Register 3

This Register controls and adjusts the setting of DREN, DRP and SRST parameters.

CNTL3(0x32)			
Bit	Description	Attr	Default
7:4	Reserved		
3	DREN: Data ready function enable 1'b0: Disable 1'b1: Enable (Master switch for DRDY output pin)	R/W	1
2	DRP: DRDY signal active	R/W	1

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	1'b0: Logic low 1'b1: Logic high		
1	Reserved		
0	SRST: Soft reset, perform the same routine as POR 0: No action 1: Start immediately POR routine —This bit is automatically reset to zero after POR routine	R	0

6.4.11. Over-Sampling Ratio Control Register

This register controls the Over-Sampling Ratio (OSR) of IST8315-L to lower the noise. Higher OSR leads to lower noise.

OSRCNTL(0x41)			
Bit	Description	Attr	Default
7:6	Reserved.	R/W	0
5:3	OSR for Y sensor data. Oversampling will be done before switching to next channel 3'b000: OSR = 1 (ODR_{max} = 1000 Hz) 3'b001: OSR = 2 (ODR_{max} = 500 Hz) 3'b010: OSR = 4 (ODR_{max} = 333 Hz) 3'b011: OSR = 8 (ODR_{max} = 200 Hz) 3'b100: OSR = 16 (ODR_{max} = 100 Hz) (Default) 3'b101: OSR = 32 (ODR_{max} = 50 Hz) Others: OSR = 2 (ODR_{max} = 500 Hz)	R/W	0x4h
2:0	OSR for X & Z sensors' data. Oversampling will be done before switching to the next channel 3'b000: OSR = 1 (ODR_{max} = 1000 Hz) 3'b001: OSR = 2 (ODR_{max} = 500 Hz) 3'b010: OSR = 4 (ODR_{max} = 333 Hz) 3'b011: OSR = 8 (ODR_{max} = 200 Hz) 3'b100: OSR = 16 (ODR_{max} = 100 Hz) (Default) 3'b101: OSR = 32 (ODR_{max} = 50 Hz) Others: OSR = 2 (ODR_{max} = 500 Hz)	R/W	0x4h

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7. Ordering Information

Order Number	Package Type	Packaging	Marking Information
IST8315-L	LGA – 12 pin	Tape and Reel: 3k pieces per reel	$X_1X_2X_3$ 15● X_1: Last number of the year X_2X_3: Week number 15: Product code

For more information on iSentek's Magnetic Sensors, please send an email to sales@isentek.com; or visit us online at www.isentek.com.

The U.S. patents 9297863 and 9562953B2 and the Taiwanese patents I437249, I420128, I463160, and I565958 cover our described magnetic sensor technology.

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