T-3488 Datasheet

High Performance 6-Axis MotionTracking™ IMU

T-3488 HIGHLIGHTS

The T-3488 is a high performance 6-axis MEMS MotionTracking device that combines a 3-axis gyroscope and a 3-axis accelerometer. It has a configurable host interface that supports I3C℠, I²C, and SPI serial communication, features up to 1 Kbytes FIFO and 2 programmable interrupts with ultra-low-power wake-on-motion support to minimize system power consumption.

The T-3488 supports the lowest gyro and accel sensor noise in this IMU class, and has the highest stability against temperature, shock (up to 20,000g) or SMT/bend induced offset as well as immunity against out-of-band vibration induced noise.

Other industry-leading features include on-chip APEX Motion Processing engine for gesture recognition, along with programmable digital filters, and an embedded temperature sensor.

The device supports a VDD operating range of 1.71V to 3.6V, and a separate VDDIO operating range from 1.08V to 3.6V.

BLOCK DIAGRAM



T-3488 FEATURES

- Gyroscope Noise: 8.6 mdps/√Hz & Accelerometer Noise: 185 µg/√Hz (X and Y-axis); 220 µg/√Hz (Z-axis)
- Low-Noise mode 6-axis current consumption of 0.77 mA
- Low-Power mode support for always-on experience
- User selectable Gyro Full-scale range (dps): ±250/500/1000/2000
- User selectable Accelerometer Full-scale range (g): ± 2/4/8/16
- User-programmable digital filters for gyro, accel, and temp sensor
- APEX Motion Functions: Tilt Detection, Low-g Detection, High-g Detection, Freefall Detection, Tap Detection, Wake on Motion, Bring to See, Activity/Inactivity Detection
- Host interface: 12.5 MHz I3C℠, 1 MHz I²C, 16 MHz SPI

APPLICATIONS

- Head Mounted Displays; AR/VR Controllers; Wearables; IoT Applications

ORDERING INFORMATION

PART	TEMP RANGE	PACKAGE
T-3488	−40°C to +85°C	2.5x3mm 14-Pin LGA

RoHS and Green-Compliant Package

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1 INTRODUCTION

1.1 PURPOSE AND SCOPE

This document is a preliminary product specification, providing a description, specifications, and design related information on the T-3488 Single-Interface MotionTracking device. The device is housed in a small 2.5x3x0.76 mm 14-pin LGA package.

Specifications and features described in the document are preliminary and subject to update.

1.2 PRODUCT OVERVIEW

The T-3488 is a 6-axis MotionTracking device that combines a 3-axis gyroscope and a 3-axis accelerometer in a small 2.5x3x0.76 mm (14-pin LGA) package. It also features up to 1 Kbytes FIFO that can lower the traffic on the serial bus interface and reduce power consumption by allowing the system processor to burst read sensor data and then go into a low-power mode. T-3488, with its 6-axis integration, enables manufacturers to eliminate the costly and complex selection, qualification, and system level integration of discrete devices, guaranteeing optimal motion performance for consumers.

The gyroscope supports four programmable full-scale range settings from ±250 dps to ±2000 dps and the accelerometer supports four programmable full-scale range settings from ±2g to ±16g.

Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and programmable interrupts. The device features I3C^{SM}, I^{2}C, and SPI serial interfaces, a VDD operating range of 1.71V to 3.6V, and a separate VDDIO operating range of 1.08V to 3.6V.

The host interface can be configured to support I3C^{SM} slave, I^{2}C slave, or SPI slave modes. The I3C^{SM} interface supports speeds up to 12.5 MHz (data rates up to 12.5 Mbps in SDR mode), the I^{2}C interface supports speeds up to 1 MHz, and the SPI interface supports speeds up to 16 MHz.

The device provides high robustness by supporting 20,000*g* shock reliability.

1.3 APPLICATIONS

- Head Mounted Displays; AR/VR Controllers; Wearables; IoT Applications

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2 FEATURES

2.1 GYROSCOPE FEATURES

The triple-axis MEMS gyroscope in the T-3488 includes a wide range of features:

- Digital-output X-, Y-, and Z-axis angular rate sensors (gyroscopes) with programmable full-scale range of ±250, ±500, ±1000, and ±2000 degrees/sec
- Low Noise (LN) power mode support
- Digitally programmable low-pass filters
- Factory calibrated sensitivity scale factor
- Self-test

2.2 ACCELEROMETER FEATURES

The triple-axis MEMS accelerometer in T-3488 includes a wide range of features:

- Digital-output X-, Y-, and Z-axis accelerometer with programmable full-scale range of ±2*g*, ±4*g*, ±8*g* and ±16*g*
- Low Noise (LN) and Low Power (LP) power modes support
- User-programmable interrupts
- Wake-on-motion interrupt for low power operation of applications processor
- Self-test

2.3 MOTION FEATURES

T-3488 includes the following motion features, also known as APEX:

- Tilt Detection: Issues an interrupt when the Tilt angle exceeds a user configurable value (default 35 degrees) for more than a programmable time.
- Low-g Detection: Triggers an interrupt when absolute value of accelerometer combined axis falls below a programmable threshold and stays below the threshold for a programmable time.
- High-g Detection: Triggers an interrupt when absolute value of any accelerometer axis goes above a programmable threshold and stays above the threshold for a programmable time.
- Freefall Detection: Triggers an interrupt when device freefall is detected and outputs freefall duration.
- Tap Detection: Triggers an interrupt when single/double/triple TAP is detected on any axis.
- Tap-on-face (Wide Area Tap, WAT): Recognizes tap gestures made on the user's face or ear. The system detects impact locations that are not in direct contact with the device itself. Triggers an interrupt when double/triple WAT is detected on any axis.
- Wake on Motion (WoM): Detects motion when accelerometer samples exceed a programmable threshold. This motion event can be used to enable device operation from sleep mode.
- Bring To See: Triggers an interrupt when device is brought to user eyesight or when device is brought back to a resting position.
- Activity/Inactivity Detection: Triggers an interrupt when activity, inactivity or inactivity for a significantly longer time is detected.

2.4 ADDITIONAL FEATURES

T-3488 includes the following additional features:

- Up to 1 Kbytes FIFO buffer enables the applications processor to read the data in bursts
- User-programmable digital filters for gyroscope, and accelerometer
- 12.5 MHz I3C^{SM} (data rates up to 12.5 Mbps in SDR mode) / 1 MHz I^{2}C / 16 MHz SPI slave host interface
- Digital-output temperature sensor
- Smallest and thinnest LGA package for portable devices: 2.5x3x0.76 mm (14-pin LGA)
- 20,000*g* shock tolerant
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

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3 ELECTRICAL CHARACTERISTICS

3.1 GYROSCOPE SPECIFICATIONS

Typical Operating Conditions, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
GYROSCOPE SENSITIVITY						
Full-Scale Range	GYRO_UI_FS_SEL=1		±2000		º/s	1
	GYRO_UI_FS_SEL=2		±1000		º/s	1
	GYRO_UI_FS_SEL=3		±500		º/s	1
	GYRO_UI_FS_SEL=4		±250		º/s	1
Gyroscope ADC Word Length	Output in two's complement format		16		bits	1
Sensitivity Scale Factor	GYRO_UI_FS_SEL=1		16.4		LSB/(º/s)	1
	GYRO_UI_FS_SEL=2		32.8		LSB/(º/s)	1
	GYRO_UI_FS_SEL=3		65.5		LSB/(º/s)	1
	GYRO_UI_FS_SEL=4		131		LSB/(º/s)	1
Sensitivity Scale Factor Initial Tolerance	Component-level, 25°C		±0.25		%	2, 5
Sensitivity Scale Factor Variation Over Temperature	0°C to +85°C; Board-Level		±0.007		%/ºC	2, 4
Nonlinearity	Best fit straight line; 25°C; Board-Level		±0.1		%	2, 4
Cross-Axis Sensitivity	Board-level		±0.2		%	2, 4
ZERO-RATE OUTPUT (ZRO)						
Initial ZRO Tolerance	Component-level, 25°C		±1		º/s	2, 5
ZRO Variation vs. Temperature	0°C to +85°C; Board-Level		±0.015		º/s/ºC	2, 4
OTHER PARAMETERS						
Rate Noise Spectral Density	@ 10 Hz		0.0086		º/s /√Hz	2
Total RMS Noise	Bandwidth = 100 Hz		0.086		º/s-rms	3
Gyroscope Mechanical Frequencies		27	29	32	kHz	2
Gyroscope Start-Up Time	Time from gyro enable to gyro drive ready		40		ms	2, 6
Output Data Rate		12.5		800	Hz	1

Table 1. Gyroscope Specifications

Notes:

1. Guaranteed by design.
2. Derived from validation or characterization of parts, not tested in production.
3. Calculated from Rate Noise Spectral Density.
4. Board-level spec values depend on specific board design. For design information of boards used for device characterization, that forms the basis of the spec values reported here, please contact your local TDK InvenSense FAE.
5. Value after factory test and trim.
6. Measurement conditions: Gyroscope ODR = 800Hz; Register field GYRO_LPF_BW_SEL = 000.

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3.2 ACCELEROMETER SPECIFICATIONS

Typical Operating Conditions, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS	NOTES
ACCELEROMETER SENSITIVITY							
Full-Scale Range	ACCEL_UI_FS_SEL=1			±16		*g*	1
	ACCEL_UI_FS_SEL=2			±8		*g*	1
	ACCEL_UI_FS_SEL=3			±4		*g*	1
	ACCEL_UI_FS_SEL=4			±2		*g*	1
ADC Word Length	Output in two's complement format			16		bits	1
Sensitivity Scale Factor	ACCEL_UI_FS_SEL=1			2,048		LSB/*g*	1
	ACCEL_UI_FS_SEL=2			4,096		LSB/*g*	1
	ACCEL_UI_FS_SEL=3			8,192		LSB/*g*	1
	ACCEL_UI_FS_SEL=4			16,384		LSB/*g*	1
Sensitivity Scale Factor Initial Tolerance	Component-level, 25°C			±0.25		%	2, 5
Sensitivity Change vs. Temperature	0°C to +85°C; Board-Level			±0.015		%/ºC	2, 4
Nonlinearity	Best Fit Straight Line, ±2g; Board-Level			±0.1		%	2, 4
Cross-Axis Sensitivity	Board-level			±0.2		%	2, 4
ZERO-G OUTPUT							
Initial Tolerance	Component-level, 25°C			±15		m*g*	2, 5
Zero-G Level Change vs. Temperature	0°C to +85°C; Board-Level			±0.2		mg/ºC	2, 4
OTHER PARAMETERS							
Power Spectral Density	@ 10 Hz	X and Y-axis		185		µg/√Hz	2
		Z-axis		220		µg/√Hz	2
RMS Noise	Bandwidth = 100 Hz	X and Y-axis		1.85		mg-rms	3
		Z-axis		2.20		mg-rms	3
Accelerometer Startup Time	From sleep mode to valid data			10		ms	2, 6
Output Data Rate			0.78125		800	Hz	1

Table 2. Accelerometer Specifications

Notes:

1. Guaranteed by design.
2. Derived from validation or characterization of parts, not tested in production.
3. Calculated from Power Spectral Density.
4. Board-level spec values depend on specific board design. For design information of boards used for device characterization, that forms the basis of the spec values reported here, please contact your local TDK InvenSense FAE.
5. Value after factory test and trim.
6. Measurement conditions: Accelerometer ODR = 800Hz. Register field ACCEL_LPF_BW_SEL = 000.

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3.3 ELECTRICAL SPECIFICATIONS

3.3.1 D.C. Electrical Characteristics

Typical Operating Conditions, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLY VOLTAGES						
VDD		1.71	1.8	3.6	V	1
VDDIO		1.08	1.8	3.6	V	1
SUPPLY CURRENTS						
Low-Noise Mode	6-Axis Gyroscope + Accelerometer		0.77		mA	2
	3-Axis Accelerometer		0.34		mA	2
	3-Axis Gyroscope		0.69		mA	2
Low-Power Mode	3-Axis Accelerometer (100Hz ODR; 2x AVG)		55		µA	2
	3-Axis Accelerometer (50Hz ODR; 2x AVG)		35		µA	2
	3-Axis Accelerometer (25Hz ODR; 2x AVG)		20		µA	2
Full-Chip Sleep Mode	At 25ºC		3		µA	2
TEMPERATURE RANGE						
Specified Temperature Range	Performance parameters are not applicable beyond Specified Temperature Range	-40		+85	°C	1

Table 3. D.C. Electrical Characteristics

Notes:

1. Guaranteed by design.
2. Derived from validation or characterization of parts, not tested in production.

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3.3.2 A.C. Electrical Characteristics

Typical Operating Conditions, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLIES						
Supply Ramp Time	Monotonic ramp. Ramp rate is 10% to 90% of the final value	0.01		1	ms	1
Power Supply Noise	Up to 1MHz		10	50	mV peak-peak	1
TEMPERATURE SENSOR						
Operating Range	Ambient	-40		85	°C	1
25°C Output	Output in two's complement format		0		LSB	3
ADC Resolution			16		bits	2
ODR	With Filter	0.78125		800	Hz	2, 4
Room Temperature Offset	25°C	-3		3	°C	3
Stabilization Time (fixed number of clock cycles)				0.64	sec	2
Sensitivity	Trimmed	125	128	129	LSB/°C	1
Sensitivity for FIFO data	Trimmed	1.95	2	2.01	LSB/°C	1
POWER-ON RESET						
Start-up time for register read/write	From power-up			1	ms	1
I²C ADDRESS						
I²C ADDRESS	AP_AD0 = 0 AP_AD0 = 1		1101000 1101001			
DIGITAL INPUTS (SCLK, SDI, CS)						
V_{IH}, High Level Input Voltage		0.7*VDDIO			V	1
V_{IL}, Low Level Input Voltage				0.3*VDDIO	V	
C_I, Input Capacitance				10	pF	
DIGITAL OUTPUT (SDO, INT1, INT2)						
V_{OH}, Logic Output High Voltage		0.9*VDDIO			V	1
V_{OL}, Logic Output Low Voltage				0.1*VDDIO	V	
Logic High-Z Output Current	0 < Vpin < VDDIO	-0.1		0.1	µA	
t_{INT}, INT Pulse Width	int_tpulse_duration= 0 , 1 (100us, 8us) ;	8		100	µs	
I²C I/O (SCL, SDA)						
V_{IL}, LOW-Level Input Voltage		-0.5V		0.3*VDDIO	V	1
V_{IH}, HIGH-Level Input Voltage		0.7*VDDIO		VDDIO + 0.5V	V	
V_{hys}, Hysteresis			0.1*VDDIO		V	
V_{OL}, LOW-Level Output Voltage	3 mA sink current	0		0.4	V	
I_{OL}, LOW-Level Output Current	V_{OL}=0.4 V V_{OL}=0.6 V		3 6		mA mA	
Output Leakage Current			100		nA	
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pf	20+0.1C_b		300	ns	
INTERNAL CLOCK SOURCE						
Clock Frequency Initial Tolerance	Gyro inactive; 25°C	-1		+1	%	1
	Gyro active; 25°C	-1		+1	%	1
Frequency Variation over Temperature	Gyro inactive; -40°C to +85°C			±3	%	1
	Gyro active; -40ºC to +85ºC			±1.25	%	1

Table 4. A.C. Electrical Characteristics

Notes:

1. Expected results based on design, will be updated after characterization. Not tested in production.
2. Guaranteed by design.
3. Production tested.
4. Temperature sensor ODR is the higher value between gyroscope and accelerometer ODR.

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3.4 I²C TIMING CHARACTERIZATION

Typical Operating Conditions, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted. Slew Rate can be configured by the user using register PAD_SLEW1.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
I²C TIMING	**I²C FAST-MODE PLUS**					
f_{SCL}, SCL Clock Frequency				1	MHz	1
$t_{HD.STA}$, (Repeated) START Condition Hold Time		0.26			µs	1
t_{LOW}, SCL Low Period		0.5			µs	1
t_{HIGH}, SCL High Period		0.26			µs	1
$t_{SU.STA}$, Repeated START Condition Setup Time		0.26			µs	1
$t_{HD.DAT}$, SDA Data Hold Time		0			µs	1
$t_{SU.DAT}$, SDA Data Setup Time		50			ns	1
$t_{SU.STO}$, STOP Condition Setup Time		0.5			µs	1
t_{BUF}, Bus Free Time Between STOP and START Condition		0.5			µs	1
C_b, Capacitive Load for each Bus Line				550	pF	1
$t_{VD.DAT}$, Data Valid Time				0.45	µs	1
$t_{VD.ACK}$, Data Valid Acknowledge Time				0.45	µs	1
t_{rSCL}, SCL signal Rise Time	Sourced by host	-		120	ns	1
t_{fSCL}, SCL signal Fall Time	Sourced by host	20*VDDIO/5.5V		120	ns	1
t_{rSDA}, SDA signal Rise Time		-		120	ns	1
t_{fSDA}, SDA signal Fall Time		20*VDDIO/5.5V		120	ns	1

Table 5. I²C Timing Characteristics

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

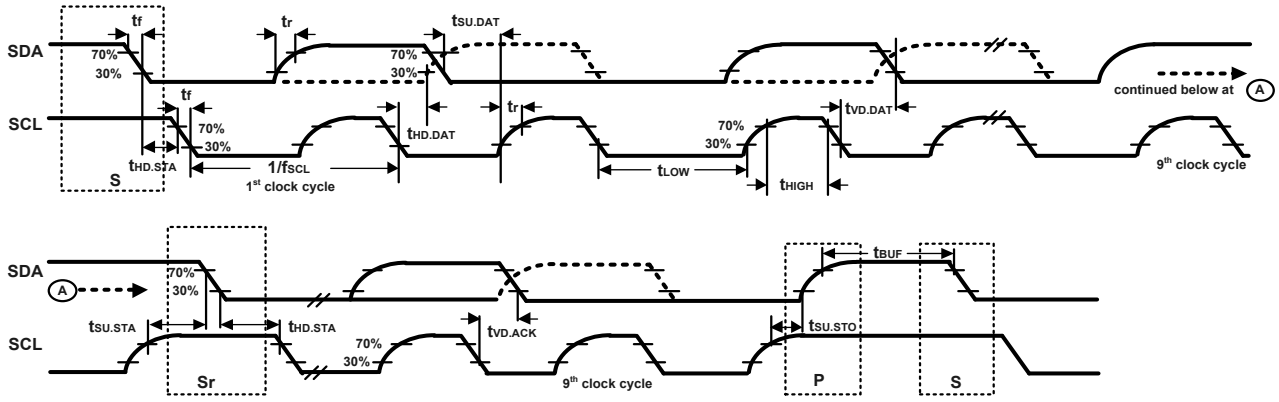


Figure 1. I²C Bus Timing Diagram

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3.5 SPI TIMING CHARACTERIZATION – 4-WIRE SPI MODE

Typical Operating Conditions, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted. Slew Rate can be configured by the user using register PAD_SLEW0.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SPI TIMING						
f_{SPC}, SCLK Clock Frequency	Default			16	MHz	1
t_{LOW}, SCLK Low Period		28			ns	1
t_{HIGH}, SCLK High Period		28			ns	1
$t_{SU.CS}$, CS Setup Time		17			ns	1
$t_{HD.CS}$, CS Hold Time		5			ns	1
$t_{SU.SDI}$, SDI Setup Time		3			ns	1
$t_{HD.SDI}$, SDI Hold Time		8			ns	1
$t_{VD.SDO}$, SDO Valid Time	C_{load} = 20 pF			18.5	ns	1
$t_{HD.SDO}$, SDO Hold Time	C_{load} = 20 pF	3.5			ns	1
$t_{DIS.SDO}$, SDO Output Disable Time				18.5	ns	1

Table 6. 4-Wire SPI Timing Characteristics

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

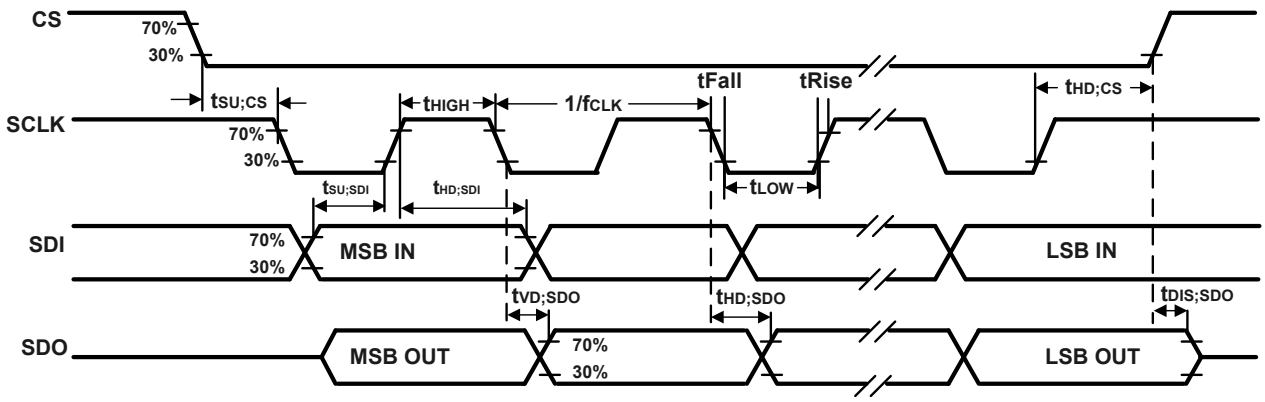


Figure 2. 4-Wire SPI Bus Timing Diagram

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3.6 SPI TIMING CHARACTERIZATION – 3-WIRE SPI MODE

Typical Operating Conditions, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted. Slew Rate can be configured by the user using register PAD_SLEW0.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SPI TIMING						
f_{SPC}, SCLK Clock Frequency	Default			16	MHz	1
t_{LOW}, SCLK Low Period		28			ns	1
t_{HIGH}, SCLK High Period		28			ns	1
$t_{SU.CS}$, CS Setup Time		17			ns	1
$t_{HD.CS}$, CS Hold Time		5			ns	1
$t_{SU.SDIO}$, SDIO Input Setup Time		3			ns	1
$t_{HD.SDIO}$, SDIO Input Hold Time		8			ns	1
$t_{VD.SDIO}$, SDIO Output Valid Time	C_{load} = 20 pF			18.5	ns	1
$t_{HD.SDIO}$, SDIO Output Hold Time	C_{load} = 20 pF	3.5			ns	1
$t_{DIS.SDIO}$, SDIO Output Disable Time				18.5	ns	1

Table 7. 3-Wire SPI Timing Characteristics

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

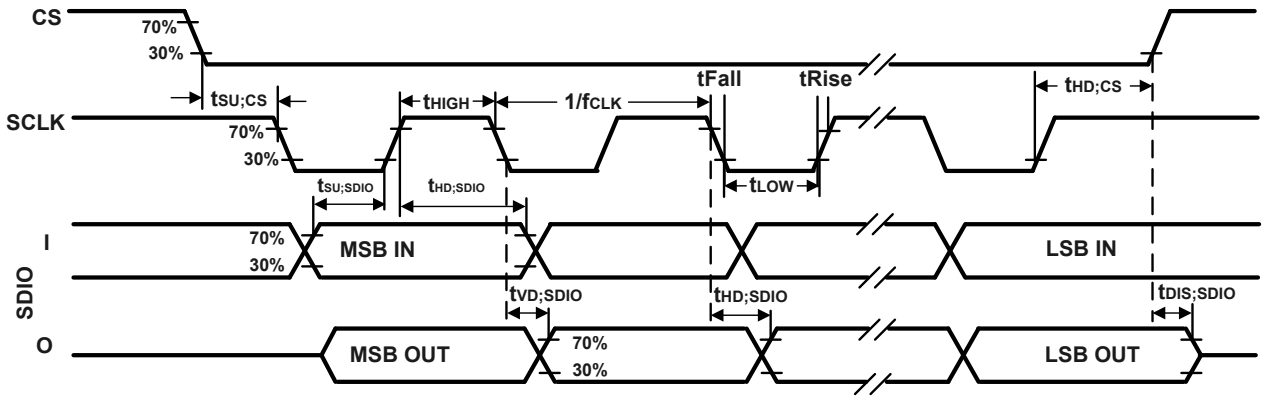


Figure 3. 3-Wire SPI Bus Timing Diagram

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3.7 ABSOLUTE MAXIMUM RATINGS

Stresses above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

PARAMETER	RATING
Supply Voltage, VDD	-0.5V to 4V
Supply Voltage, VDDIO	-0.5V to 4V
Input Voltage Level (SCL, SDA)	-0.5V to VDDIO + 0.5 V
Acceleration (Any Axis, unpowered)	20,000g for 0.2 ms
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-40°C to +125°C
Electrostatic Discharge (ESD) Protection	2 kV (HBM); 500V (CDM)
Latch-up	JEDEC Class II (2),125°C ±100 mA

Table 8. Absolute Maximum Ratings

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4 APPLICATIONS INFORMATION

4.1 PIN OUT DIAGRAM AND SIGNAL DESCRIPTION

PIN NUMBER	PIN NAME	PIN DESCRIPTION	NOTES
1	AP_SDO / AP_AD0	AP_SDO: AP SPI serial data output (4-wire mode); AP_AD0: AP I3C^{SM} / I^{2}C slave address LSB	This pin supports both internal pull-up and pull-down functionality. By default, internal weak pull-down is enabled. If user is driving the input, it is recommended to disable the pull-down by setting PADS_AP_SDO_PE_TRIM_D2A=0 to avoid leakage.
2	RESV	No Connect or Connect to GND or Connect to VDDIO	
3	RESV	No Connect or Connect to GND or Connect to VDDIO	
4	INT1 / INT	INT1: Interrupt 1 (Note: INT1 can be push-pull or open drain) INT: All interrupts mapped to pin 4	
5	VDDIO	IO power supply voltage	
6	GND	Power supply ground	
7	RESV	Connect to GND	
8	VDD	Power supply voltage	
9	INT2	INT2: Interrupt 2 (Note: INT2 can be push-pull or open drain)	
10	RESV	No Connect or Connect to GND or Connect to VDDIO	
11	RESV	No Connect or Connect to GND or Connect to VDDIO	
12	AP_CS	AP SPI Chip select (AP SPI interface); Do not connect (float) if using AP I3C^{SM} / I^{2}C interface	This pin supports both internal pull-up and pull-down functionality. By default, internal weak pull-up is enabled. If user is driving the input, it is recommended to disable the pull-up by setting PADS_AP_CS_PE_TRIM_D2A=0 to avoid leakage.
13	AP_SCL / AP_SCLK	AP_SCL: AP I3C^{SM} / I^{2}C serial clock; AP_SCLK: AP SPI serial clock	This pin supports both internal pull-up and pull-down functionality. By default, internal weak pull-up is enabled. If user is driving the input, it is recommended to disable the pull-up by setting PADS_AP_SCLK_PE_TRIM_D2A=0 to avoid leakage.
14	AP_SDA / AP_SDIO / AP_SDI	AP_SDA: AP I3C^{SM} / I^{2}C serial data; AP_SDIO: AP SPI serial data I/O (3-wire mode); AP_SDI: AP SPI serial data input (4-wire mode)	This pin supports both internal pull-up and pull-down functionality. By default, internal weak pull-up is enabled. If user is driving the input, it is recommended to disable the pull-up by setting PADS_AP_SDI_PE_TRIM_D2A=0 to avoid leakage.

Table 9. Signal Descriptions

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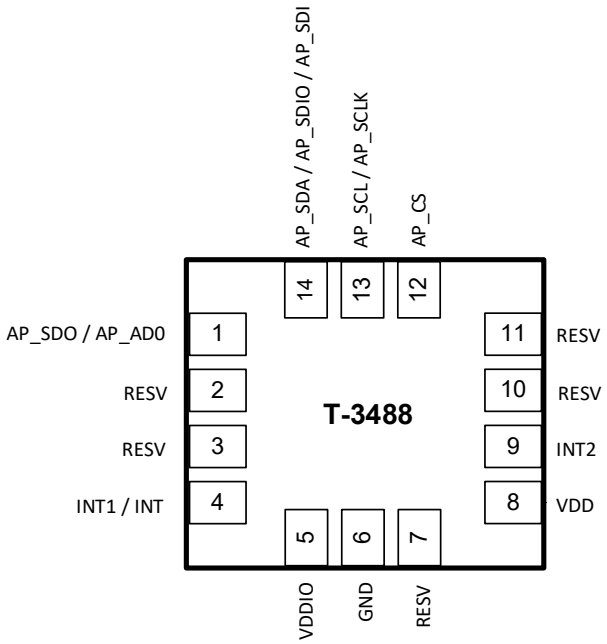


Figure 4. Pin Out Diagram (Top View) for T-3488 2.5x3x0.76 mm LGA

4.2 TYPICAL OPERATING CIRCUIT

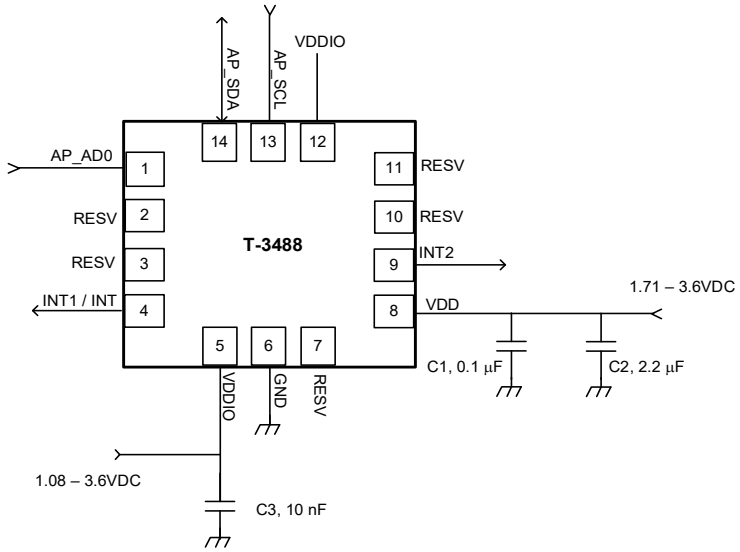


Figure 5. T-3488 Application Schematic (I3C^{SM} / I^{2}C Interface to Host)

Note: I^{2}C lines are open drain and pull-up resistors (e.g. 10 kΩ) are required.

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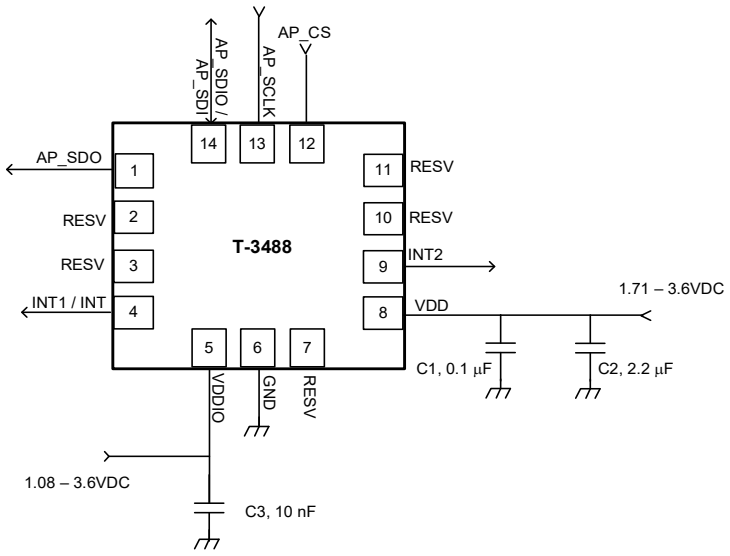


Figure 6. T-3488 Application Schematic (SPI Interface to Host)

4.3 BILL OF MATERIALS FOR EXTERNAL COMPONENTS

COMPONENT	LABEL	SPECIFICATION	QUANTITY
VDD Bypass Capacitors	C1	X7R, 0.1µF ±10%	1
	C2	X7R, 2.2µF ±10%	1
VDDIO Bypass Capacitor	C3	X7R, 10nF ±10%	1

Table 10. Bill of Materials

4.4 SYSTEM BLOCK DIAGRAM

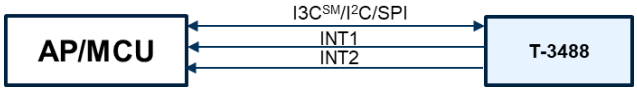


Figure 7. T-3488 System Block Diagram

Note: The above block diagram is an example. Please refer to the pin-out (section 4.1) for other configuration options.

4.5 OVERVIEW

The T-3488 is comprised of the following key blocks and functions:

- Three-axis MEMS gyroscope
- Three-axis MEMS accelerometer
- I3C^{SM}, I^{2}C, and SPI serial communications interfaces to Host
- Self-Test
- Sensor Data Registers
- FIFO
- Interrupts
- Digital-Output Temperature Sensor
- Bias and LDOs
- Charge Pump
- Standard Power Modes

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4.6 THREE-AXIS MEMS GYROSCOPE

The T-3488 includes a vibratory MEMS rate gyroscope, which detects rotation about the X-, Y-, and Z- Axes. When the gyroscope is rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pickoff. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using on-chip Analog-to-Digital Converter (ADC) to sample each axis. The full-scale range of the gyro sensor may be digitally programmed to ±250, ±500, ±1000, and ±2000 degrees per second (dps).

4.7 THREE-AXIS MEMS ACCELEROMETER

The T-3488 includes a 3-Axis MEMS accelerometer. Acceleration along a particular axis induces displacement of a proof mass in the MEMS structure, and capacitive sensors detect the displacement. The T-3488 architecture reduces the accelerometers' susceptibility to fabrication variations as well as to thermal drift. When the device is placed on a flat surface, it will measure 0*g* on the X- and Y-axes and +1*g* on the -Z-axis. The accelerometers' scale factor is calibrated at the factory and is nominally independent of supply voltage. The full-scale range of the digital output can be adjusted to ±2*g*, ±4*g*, ±8*g* and ±16*g*.

4.8 I3C^{SM}, I^{2}C AND SPI HOST INTERFACE

The T-3488 communicates to the application processor using an I3C^{SM}, I^{2}C, or SPI serial interface. The T-3488 always acts as a slave when communicating to the application processor.

4.9 SELF-TEST

Self-test allows for the testing of the mechanical and electrical portions of the sensors. The self-test for each measurement axis can be activated by means of the gyroscope and accelerometer self-test registers. When the self-test is activated, the electronics cause the sensors to be actuated and produce an output signal. The output signal is used to observe the self-test response. The self-test response is defined as follows:

SELF-TEST RESPONSE = SENSOR OUTPUT WITH SELF-TEST ENABLED – SENSOR OUTPUT WITH SELF-TEST DISABLED

When the value of the self-test response is within the specified min/max limits, the part has passed self-test. When the self-test response exceeds the min/max values, the part is deemed to have failed self-test.

4.10 SENSOR DATA REGISTERS

The sensor data registers contain the latest gyroscope, accelerometer, and temperature measurement data. They are read-only registers and are accessed via the serial interface.

4.11 INTERRUPTS

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the interrupt pins configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are (1) new data is available to be read (from the FIFO and Data registers); (2) accelerometer event interrupts; (3) FIFO watermark; (4) FIFO full. The interrupt status can be read from the Interrupt Status register.

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4.12 DIGITAL-OUTPUT TEMPERATURE SENSOR

An on-chip temperature sensor and ADC are used to measure the T-3488 die temperature. The readings from the ADC can be read from the FIFO and/or the Sensor Data registers.

Temperature sensor ODR is the higher value between gyroscope and accelerometer ODR.

Temperature data value from the sensor data registers can be converted to degrees centigrade by using the following formula:

Temperature in Degrees Centigrade = (TEMP_DATA / 128) + 25

Temperature data stored in FIFO is an 8-bit quantity at FIFO packet format, it can be converted to degrees centigrade by using the following formula:

Temperature in Degrees Centigrade = (TEMP_DATA / 2) + 25

4.13 BIAS AND LDOS

The bias and LDO section generate the internal supply and the reference voltages and currents required by the T-3488.

4.14 CHARGE PUMP

An on-chip charge pump generates the high voltage required for the MEMS oscillator.

4.15 STANDARD POWER MODES

The following table lists the user-accessible power modes for T-3488.

MODE	NAME	GYRO	ACCEL
1	Sleep Mode	Off	Off
2	Accelerometer Low-Power Mode	Off	Duty-Cycled
3	Accelerometer Low-Noise Mode	Off	On
4	Gyroscope Low-Noise Mode	On	Off
5	6-Axis Low-Noise Mode	On	On

Table 11. Standard Power Modes for T-3488

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5 SIGNAL PATH

The following figure shows a block diagram of the signal path for T-3488.

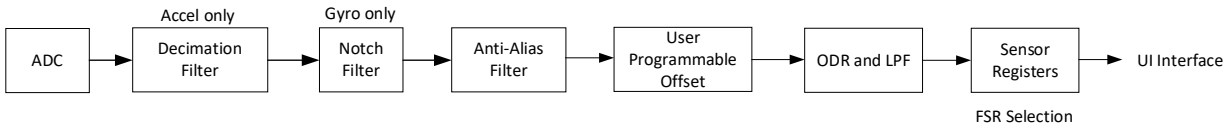


Figure 8. T-3488 Signal Path

The signal path starts with ADCs for the gyroscope and accelerometer. This is followed by Decimation Filter for the accelerometer and Notch Filter for the gyroscope. The signal is then sent through an Anti-Alias Filter (AAF). The AAF is a filter with fixed coefficients (not user configurable), also the AAF should not be bypassed.

The AAF is followed by User Programmable Offset adjustment and a 1st Order Low Pass Filter (LPF) with user selectable filter bandwidth options using register fields ACCEL_LPF_BW_SEL and GYRO_LPF_BW_SEL.

In Accelerometer Low-Power Mode, the Decimation Filter output is sent through an Average filter, with user configurable average filter setting using register field ACCEL_LP_AVG_SEL.

ODR selection is performed with user selectable ODR using register fields ACCEL_ODR and GYRO_ODR.

The output of 1st Order LPF in Low-Noise Mode is at the rate of selected ODR. In Low-Power Mode the Average filter generates samples at the ODR rate.

This is followed by Full Scale Range (FSR) selection based on user configurable settings for register fields SREG_UI_ACCEL_FS_SEL and SREG_UI_GYRO_FS_SEL.

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6 FIFO

The T-3488 contains up to 1Kbyte FIFO register that is accessible via the serial interface.

6.1 FIFO FRAME STRUCTURE

Figure 9 shows the FIFO frame structures supported in T-3488.

1. The device supports only an 8-byte FIFO frame.
2. Each FIFO frame has a 4-bit header.
    a. One bit of the header indicates if the FIFO frame contains Accel data
    b. One bit of the header indicates if the FIFO frame contains Gyro data.
3. Each FIFO frame contains data from one sensor only.
4. If two sensors are enabled, depending on the Accel and Gyro ODR rate settings, each ODR event could produce up to two 8-byte FIFO frames, one for Accel data and one for Gyro data.
5. Only 16-bit motion sensor data and 8-bit temperature data is available in FIFO frame.

Accel-only		
0	rsvd = 0	Header
1	temp, 8-bit	
2	Ax_0	
3	Ax_1	
4	Ay_0	
5	Ay_1	
6	Az_0	
7	Az_1	

Gyro-only		
0	rsvd = 0	Header
1	temp, 8-bit	
2	Gx_0	
3	Gx_1	
4	Gy_0	
5	Gy_1	
6	Gz_0	
7	Gz_1	

Header (4-bits)	
0	1: Accel, 0: not Accel
1	1: Gyro, 0: not Gyro
2	1: Invalid, 0: Valid
3	1: Big endian, 0: Little endian

Figure 9. FIFO Frame Structure

6.2 FIFO READ

1. The host should use burst read operation to read FIFO data, and each burst read should read 8*N bytes of FIFO data, as each FIFO frame is 8-byte long.
2. The device does not support a FIFO partial read from the host.
3. A partially read 8-byte FIFO frame is treated as the whole 8-byte FIFO frame has been fully read.
4. After AP_CS = 0, or after a START event, or after a reSTART event, the 1st byte of an 8-byte FIFO frame is always returned to the host in a FIFO read operation.

6.3 FIFO EMPTY PATTERN

1. A 0x7F value at the 1st byte of a FIFO frame is returned to the host as an in-band FIFO-empty notification when the FIFO buffer is empty.
2. The 1st byte of a FIFO frame is not allocated for sensor data in mission mode operation. So, the 0x7F is not a reserved word and it can be present as real sensor data.
3. The host should ignore the remaining 7-byte of a FIFO frame when the 1st byte of the FIFO frame is 0x7F. When FIFO is empty, the device keeps sending 0x7F back to host for all the 8-byte FIFO frame, not just the 1st byte of the FIFO frame.
4. In a FIFO read operation, non 0x7F data is sent to the host at the beginning if the FIFO is not empty. Once the 1st 0x7F FIFO-empty notification is sent to the host because FIFO is empty in the middle of a burst read, then all the subsequent data from the same burst read will be 0x7F, even if the FIFO buffer is no longer empty later in the same burst read operation, (before the end of the same burst read operation).

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6.4 INVALID SENSOR DATA FLAG

1. There are two options to invalidate the data in a FIFO frame.
    a. The 1st option is to use the invalid sensor data pattern as the data in the FIFO frame.
    b. The 2nd option is using the invalid flag in the 4-bit FIFO header.
2. If the 1st byte of a FIFO frame is not 0x7F, but bit [2] of the 1st byte of FIFO frame is 1 (which is bit [2] of the FIFO header), there is no valid sensor data from the current FIFO frame. The host should just ignore the sensor data from the FIFO frame.

6.5 HYBRID BURST READ

Registers FIFO_CNT and FIFO_DATA are assigned by two consecutive addresses to support the hybrid burst read operation.

6.6 FIFO FULL INTERRUPT

1. Register MIN_FREE_SPACE allows users to instruct the device when to assert a FIFO_FULL interrupt. The FIFO_FULL interrupt is asserted when the following conditions are met:
    a. After a new FIFO frame is written into the FIFO buffer, and
    b. The available free space left in the FIFO buffer ≤ MIN_FREE_SPACE
2. In stop-on-full mode, after the available free space left in the FIFO buffer = 0, the subsequent new sensor data is dropped and no new FIFO frame is written into the FIFO buffer. The condition remains so till available free space is freed up.
3. In stop-on-full mode, if the eDMP has two frames to write at the same ODR event but free space left in the FIFO buffer = 1, then the eDMP will push the accel frame and drop the gyro frame.
4. In streaming mode, if MIN_FREE_SPACE ≠ 0, the oldest FIFO frame is automatically dropped when the available free space left in FIFO buffer < MIN_FREE_SPACE. This is to free up space to accommodate the new FIFO frame. No new FIFO frame will be dropped because the available free space left in the FIFO buffer is > 0.
5. In streaming mode, if MIN_FREE_SPACE = 0, the oldest FIFO frame is not dropped by the device. Upon receiving the FIFO_FULL interrupt (when the available free space left in FIFO buffer = MIN_FREE_SPACE = 0), the host should read at least one FIFO frame before the next ODR event when one sensor is enabled. Or the host should read at least two FIFO frames before the next ODR event when two sensors are enabled. If the host has difficulties in keeping up with the ODR cadence to read FIFO frame, the host should keep the MIN_FREE_SPACE at its POR default value of 2, which would allow the oldest FIFO frame to be dropped automatically to free up space for new FIFO frame.
6. In streaming mode, if MIN_FREE_SPACE = 0, the oldest FIFO frame is not dropped by the device. If the eDMP has two frames to write at the same ODR event but free space left in the FIFO buffer = 1, then the eDMP will push the accel frame and drop the gyro frame.
7. In the case of streaming mode, with MIN_FREE_SPACE = 0, the FIFO buffer can store up to 128 FIFO frames, as the oldest FIFO frame(s) is(are) present in the FIFO buffer not removed by the device automatically. The device supports up to 128 FIFO frames in both stop-on-full and streaming mode.
8. MIN_FREE_SPACE can be changed when FIFO is in bypass mode, or FIFO operation is not enabled.

6.7 FIFO THRESHOLD REGISTER

1. Register FIFO_THRESHOLD can be changed on-the-fly without restriction.
2. Any programming of the FIFO_THRESHOLD register (with or without changing values) will automatically compare FIFO_CNT to FIFO_WM_TH, and trigger a FIFO_THS interrupt when needed.

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6.8 FIFO ODR DOWN-SAMPLING

1. GYRO_FIFO_ODR_DEC configures the down-sampled ODR rate for saving gyro data into FIFO.
2. ACCEL_FIFO_ODR_DEC configures the down-sampled ODR rate for saving accel data into FIFO.
3. On the fly change is supported for reconfiguring the FIFO ODR down-sampling operation.

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7 PROGRAMMABLE INTERRUPTS

The T-3488 has a programmable interrupt system that can generate an interrupt signal on the INT pins. Status flags indicate the source of an interrupt. Interrupt sources may be enabled and disabled individually. There are two interrupt outputs. Any interrupt may be mapped to either interrupt pin as explained in the register section. The following configuration options are available for the interrupts

- INT1 and INT2 can be push-pull or open drain
- Level or pulse mode
- Active high or active low

Additionally, T-3488 includes In-band Interrupt (IBI) support for the I3C^{SM} interface.

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8 APEX MOTION FUNCTIONS

The APEX features of T-3488 consist of:

- Tilt Detection: Issues an interrupt when the Tilt angle exceeds a user configurable value (default 35 degrees) for more than a programmable time.
- Low-g Detection: Triggers an interrupt when absolute value of accelerometer combined axis falls below a programmable threshold and stays below the threshold for a programmable time.
- High-g Detection: Triggers an interrupt when absolute value of any accelerometer axis goes above a programmable threshold and stays above the threshold for a programmable time.
- Freefall Detection: Triggers an interrupt when device freefall is detected and outputs freefall duration.
- Tap Detection: Triggers an interrupt when single/double/triple TAP is detected on any axis.
- Tap-on-face (Wide Area Tap, WAT): Recognizes tap gestures made on the user's face or ear. The system detects impact locations that are not in direct contact with the device itself. Triggers an interrupt when double/triple WAT is detected on any axis.
- Wake on Motion (WoM): Detects motion when accelerometer samples exceed a programmable threshold. This motion event can be used to enable device operation from sleep mode.
- Bring To See: Triggers an interrupt when device is brought to user eyesight or when device is brought back to a resting position.
- Activity/Inactivity Detection: Triggers an interrupt when activity, inactivity or inactivity for a significantly longer time is detected.

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9 DIGITAL INTERFACE

9.1 I3C^{SM}, I^{2}C AND SPI SERIAL INTERFACES

The internal registers and memory of the T-3488 can be accessed using I3C^{SM} at 12.5 MHz (data rates up to 12.5 Mbps in SDR mode), I^{2}C at 1 MHz or SPI at 16 MHz. SPI operates in 3-wire or 4-wire mode. Pin assignments for serial interfaces are described in Section 4.1.

9.2 I3C^{SM} INTERFACE

I3C^{SM} is a new 2-wire digital interface comprised of the signals serial data (SDA) and serial clock (SCLK). I3C^{SM} is intended to improve upon the I^{2}C interface, while preserving backward compatibility. The I3C^{SM} capability of this device is compliant with Version 1.1.1 of the MIPI Alliance Specification for I3C^{SM}.

I3C^{SM} carries the advantages of I^{2}C in simplicity, low pin count, easy board design, and multi-drop (vs. point to point), but provides the higher data rates, simpler pads, and lower power of SPI. I3C^{SM} adds higher throughput for a given frequency, in-band interrupts (from slave to master), dynamic addressing.

T-3488 supports the following features of I3C^{SM}:

- SDR data rate up to 12.5 Mbps
- Dynamic address allocation
- In-band Interrupt (IBI) support
- If the I3C^{SM} bus is stuck, the I3C^{SM} master can issue in-band-reset to bring the I3C^{SM} bus out of stuck mode – this is available in addition to a 32ms timeout
- Error detection (Parity)
- Common Command Code (CCC)

The T-3488 always operates as an I3C^{SM} slave device when communicating to the system processor, which thus acts as the I3C^{SM} master. I3C^{SM} master controls an active pullup resistance on SDA, which it can enable and disable. The pullup resistance may be a board level resistor controlled by a pin, or it may be internal to the I3C^{SM} master.

The following table shows I3C^{SM} Common Command Code (CCC) commands supported by the device.

Command Code	CCC Type	CCC is Required / Conditional / Optional	Command Name	Supported by T-3488	Comments
0x00	Broadcast	R	ENEC	Yes	Only IBI can be configured
0x01	Broadcast	R	DISEC	Yes	Only IBI can be configured
0x02	Broadcast	C	ENTAS0	Yes	Active state unused
0x03	Broadcast	O	ENTAS1	Yes	Active state unused
0x04	Broadcast	O	ENTAS2	Yes	Active state unused
0x05	Broadcast	O	ENTAS3	Yes	Active state unused
0x06	Broadcast	R	RSTDAA	Yes	
0x07	Broadcast	C	ENTDAA	Yes	
0x08	Broadcast	C	DEFTGTS	No	
0x09	Broadcast	R	SETMWL	No	MIPI defined exception
0x0A	Broadcast	R	SETMRL	No	MIPI defined exception
0x0B	Broadcast	O	ENTTM	No	
0x0C	Broadcast	O	SETBUSCON	No	
0x12	Broadcast	C	ENDXFER	No	
0x20	Broadcast	C	ENTHDR0	Yes	Only to ignore HDR traffic
0x21	Broadcast	C	ENTHDR1	Yes	Only to ignore HDR traffic
0x22	Broadcast	C	ENTHDR2	Yes	Only to ignore HDR traffic

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0x23	Broadcast	C	ENTHDR3	Yes	Only to ignore HDR traffic
0x24	Broadcast	C	ENTHDR4	Yes	Only to ignore HDR traffic
0x25	Broadcast	C	ENTHDR5	Yes	Only to ignore HDR traffic
0x26	Broadcast	C	ENTHDR6	Yes	Only to ignore HDR traffic
0x27	Broadcast	C	ENTHDR7	Yes	Only to ignore HDR traffic
0x28	Broadcast	C	SETXTIME	No	All actions ignored (STC, AsyncMode0 are not supported.)
0x29	Broadcast	O	SETAASA	Yes	
0x2A	Broadcast	R	RSTACT	Yes	Defining byte up to 0x2
0x2B	Broadcast	C	DEFGRPA	No	
0x2C	Broadcast	C	RSTGRPA	No	
0x2D	Broadcast	C	MLANE	No	
0x80	Direct	R	ENEC	Yes	Only IBI can be configured
0x81	Direct	R	DISEC	Yes	Only IBI can be configured
0x82	Direct	C	ENTAS0	Yes	Active state unused
0x83	Direct	O	ENTAS1	Yes	Active state unused
0x84	Direct	O	ENTAS2	Yes	Active state unused
0x85	Direct	O	ENTAS3	Yes	Active state unused
0x86	Direct	R	RSTDAA	No	Deprecated in MIPI standard
0x87	Direct Set	O	SETDASA	Yes	Formats 1 and 2 supported
0x88	Direct Set	C	SETNEWDA	Yes	
0x89	Direct Set	R	SETMWL	No	MIPI defined exception
0x8A	Direct Set	R	SETMRL	No	MIPI defined exception
0x8B	Direct Get	R	GETMWL	No	MIPI defined exception
0x8C	Direct Get	R	GETMRL	No	MIPI defined exception
0x8D	Direct Get	C	GETPID	Yes	
0x8E	Direct Get	C	GETBCR	Yes	
0x8F	Direct Get	C	GETDCR	Yes	
0x90	Direct Get	R	GETSTATUS	Yes	Only Format 1 supported
0x91	Direct Get	C	GETACCCR	No	
0x92	Direct	C	ENDXFER	No	
0x93	Direct Set	O	SETBRGTGT	No	
0x94	Direct Get	C	GETMXDS	Yes	Only Format 1 supported
0x95	Direct Get	C	GETCAPS	Yes	Only Format 1 supported, returns two bytes
0x96	Direct	O	SETROUTE	No	
0x97	Direct	C	D2DXFER	No	
0x98	Direct	C	SETXTIME	No	
0x99	Direct	C	GETXTIME	No	
0x9A	Direct	R	RSTACT	Yes	Defining byte up to 0x2
0x9B	Direct	C	SETGRPA	No	
0x9C	Direct	C	RSTGRPA	No	
0x9D	Direct	C	MLANE	No	

Table 12. I3C^{SM} CCC Commands

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9.3 I²C INTERFACE

I²C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I²C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The T-3488 always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDDIO. The maximum bus speed is 1 MHz.

The slave address of the T-3488 is b110100X, which is 7 bits long. The LSB bit of the 7-bit address is determined by the logic level on pin AP_AD0. This allows two T-3488s to be connected to the same I²C bus. When used in this configuration, the address of one of the devices should be b1101000 (pin AP_AD0 is logic low) and the address of the other should be b1101001 (pin AP_AD0 is logic high).

9.4 I²C COMMUNICATIONS PROTOCOL

START (S) and STOP (P) Conditions

Communication on the I²C bus starts when the master puts the START condition (S) on the bus, which is defined as a HIGH-to-LOW transition of the SDA line while SCL line is HIGH (see figure below). The bus is considered to be busy until the master puts a STOP condition (P) on the bus, which is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH (see Figure 10).

Additionally, the bus remains busy if a repeated START (Sr) is generated instead of a STOP condition.

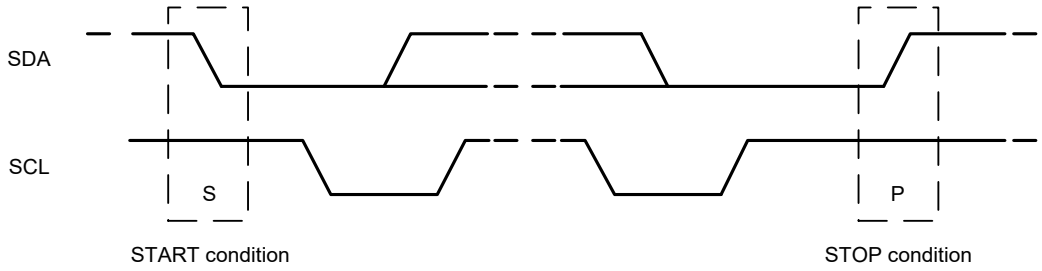


Figure 10. START and STOP Conditions

Data Format / Acknowledge

I²C data bytes are defined to be 8-bits long. There is no restriction to the number of bytes transmitted per data transfer. Each byte transferred must be followed by an acknowledge (ACK) signal. The clock for the acknowledge signal is generated by the master, while the receiver generates the actual acknowledge signal by pulling down SDA and holding it low during the HIGH portion of the acknowledge clock pulse.

Communications

After beginning communications with the START condition (S), the master sends a 7-bit slave address followed by an 8th bit, the read/write bit. The read/write bit indicates whether the master is receiving data from or is writing to the slave device. Then, the master releases the SDA line and waits for the acknowledge signal (ACK) from the slave device. Each byte transferred must be followed by an acknowledge bit. To acknowledge, the slave device pulls the SDA line LOW and keeps it LOW for the high period of the SCL line. Data transmission is always terminated by the master with a STOP condition (P), thus freeing the communications line. However, the master can generate a repeated START condition (Sr), and address another slave without first generating a STOP condition (P). A LOW to HIGH transition on the SDA line while SCL is HIGH defines the stop condition. All SDA changes should take place when SCL is low, with the exception of start and stop conditions.

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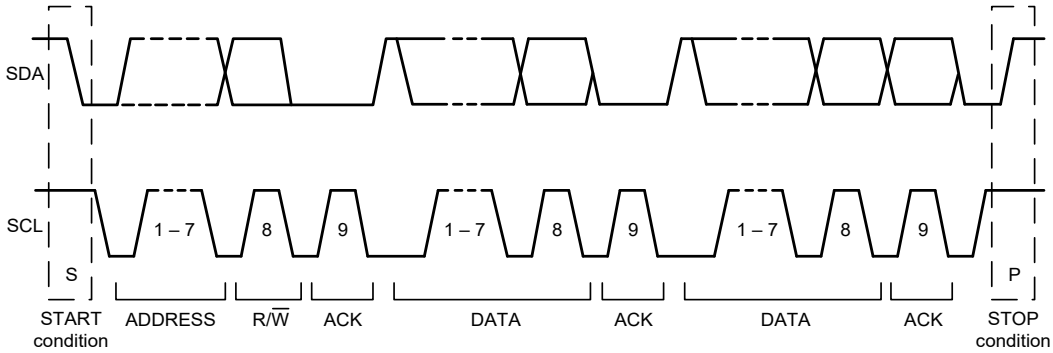


Figure 11. Complete I²C Data Transfer

To write the internal T-3488 registers, the master transmits the start condition (S), followed by the I²C address and the write bit (0). At the 9th clock cycle (when the clock is high), the T-3488 acknowledges the transfer. Then the master puts the register address (RA) on the bus. After the T-3488 acknowledges the reception of the register address, the master puts the register data onto the bus. This is followed by the ACK signal, and data transfer may be concluded by the stop condition (P). To write multiple bytes after the last ACK signal, the master can continue outputting data rather than transmitting a stop signal. In this case, the T-3488 automatically increments the register address and loads the data to the appropriate register. The following figures show single and two-byte write sequences.

Single-Byte Write Sequence

Master	S	AD+W		RA		DATA		P
Slave			ACK		ACK		ACK	

Burst Write Sequence

Master	S	AD+W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

To read the internal T-3488 registers, the master sends a start condition, followed by the I²C address and a write bit, and then the register address that is going to be read. Upon receiving the ACK signal from the T-3488, the master transmits a start signal followed by the slave address and read bit. As a result, the T-3488 sends an ACK signal and the data. The communication ends with a not acknowledge (NACK) signal and a stop bit from master. The NACK condition is defined such that the SDA line remains high at the 9th clock cycle. The following figures show single and two-byte read sequences.

Single-Byte Read Sequence

Master	S	AD+W		RA		S	AD+R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Burst Read Sequence

Master	S	AD+W		RA		S	AD+R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

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9.5 I²C TERMS

SIGNAL	DESCRIPTION
S	Start Condition: SDA goes from high to low while SCL is high
AD	Slave I²C address
W	Write bit (0)
R	Read bit (1)
ACK	Acknowledge: SDA line is low while the SCL line is high at the 9th clock cycle
NACK	Not-Acknowledge: SDA line stays high at the 9th clock cycle
RA	T-3488 internal register address
DATA	Transmit or received data
P	Stop condition: SDA going from low to high while SCL is high

Table 13. I²C Terms

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9.6 SPI INTERFACE

The T-3488 supports 3-wire or 4-wire SPI for the host interface. The T-3488 always operates as a Slave device during standard Master-Slave SPI operation.

With respect to the Master, the Serial Clock output (SCLK), the Serial Data Output (SDO), the Serial Data Input (SDI), and the Serial Data IO (SDIO) are shared among the Slave devices. Each SPI slave device requires its own Chip Select (CS) line from the master.

CS goes low (active) at the start of transmission and goes back high (inactive) at the end. Only one CS line is active at a time, ensuring that only one slave is selected at any given time. The CS lines of the non-selected slave devices are held high, causing their SDO lines to remain in a high-impedance (high-z) state so that they do not interfere with any active devices.

SPI Operational Features

1. Data is delivered MSB first and LSB last
2. Data is latched on the rising edge of SCLK
3. Data should be transitioned on the falling edge of SCLK
4. The maximum frequency of SCLK is 16 MHz
5. SPI read operations are completed in 24 or more clock cycles (two or more bytes). The first byte has a dummy value of 0 (see AN-000528 for details). SPI write operations are completed in 16 or more clock cycles (two or more bytes). The first byte contains the Register Address, and the following byte(s) contain(s) the SPI data. The first bit of the first byte contains the Read/Write bit and indicates the Read (1) operation. The following 7 bits contain the Register Address. In cases of multiple-byte Reads, data is two or more bytes:

Register Address format

MSB							**LSB**
R/W	A6	A5	A4	A3	A2	A1	A0

SPI Data format

MSB							**LSB**
D7	D6	D5	D4	D3	D2	D1	D0

6. Supports Single or Burst Read/Writes.

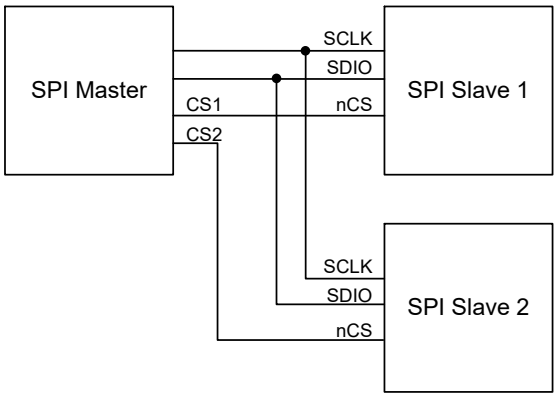


Figure 12. Typical SPI Master/Slave Configuration

Note: For each SPI read operation, the 1st byte of the read return data after (AP_CS = 0) is always a dummy value of 0. The byte after the 1st dummy byte is the read return data from the selected register per the address.

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10 ASSEMBLY

This section provides general guidelines for assembling Micro Electro-Mechanical Systems (MEMS) devices packaged in LGA package.

10.1 ORIENTATION OF AXES

The diagram below shows the orientation of the axes of sensitivity and the polarity of rotation. Note the pin 1 identifier (•) in the figure.

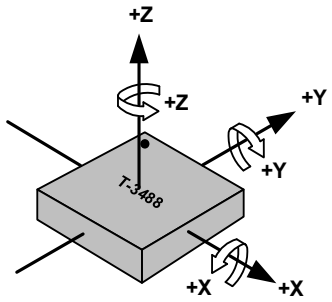


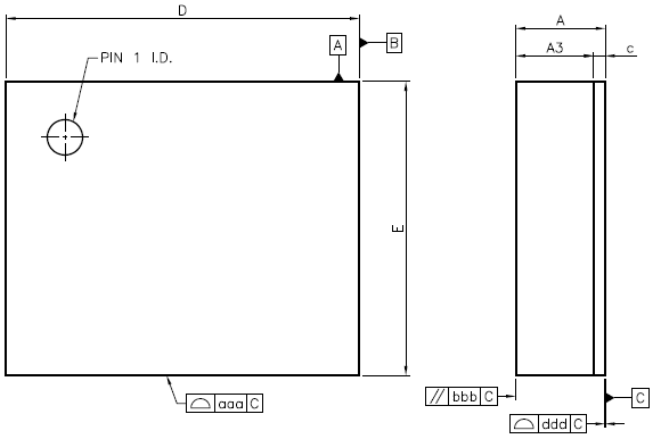
Figure 13. Orientation of Axes of Sensitivity and Polarity of Rotation

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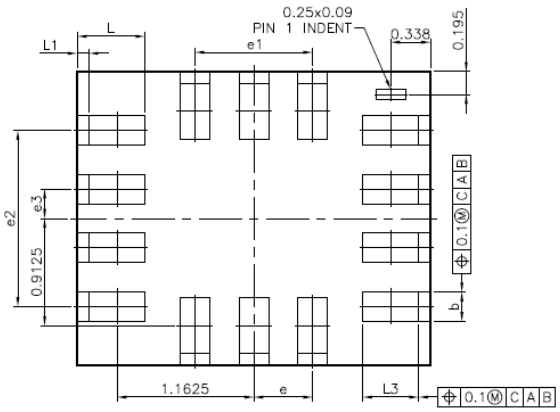
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10.2 PACKAGE DIMENSIONS

14 Lead LGA (2.5x3x0.76mm)



Top View



Bottom View

		DIMENSIONS IN MILLIMETERS		
	SYMBOLS	MIN	NOM	MAX
Total Thickness	A	0.71	0.76	0.81
Mold Thickness	A3	---	0.66 REF	---
Lead Width	b	0.20	0.25	0.30
Substrate Thickness	c	---	0.115 REF	---
Body Size	D	2.95	3.00	3.05
	E	2.45	2.50	2.55
Lead Pitch	e	---	0.50	---
Edge Ball Center to Center	e1	---	1.00	---
	e2	---	1.50	---
Body Center to Contact Ball	e3	---	0.25 REF	---
Lead to PKG Edge	L	0.525	0.575	0.625
Lead Edge to PKG Edge	L1	---	0.1 REF	---
Lead Length	L3	0.425	0.475	0.525
Package Edge Tolerance	aaa	---	0.1 REF	---
Mold Flatness	bbb	---	0.2 REF	---
Coplanarity	ccc	---	0.08 REF	---

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11 DEVICE PACKAGE IN TAPE AND REEL

T-3488 devices are packaged in the tape and reel as shown in the figures below.

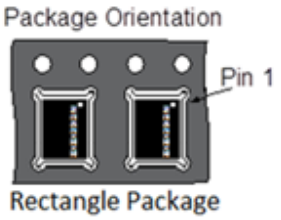


Figure 14. T-3488 Device Package in Tape and Reel

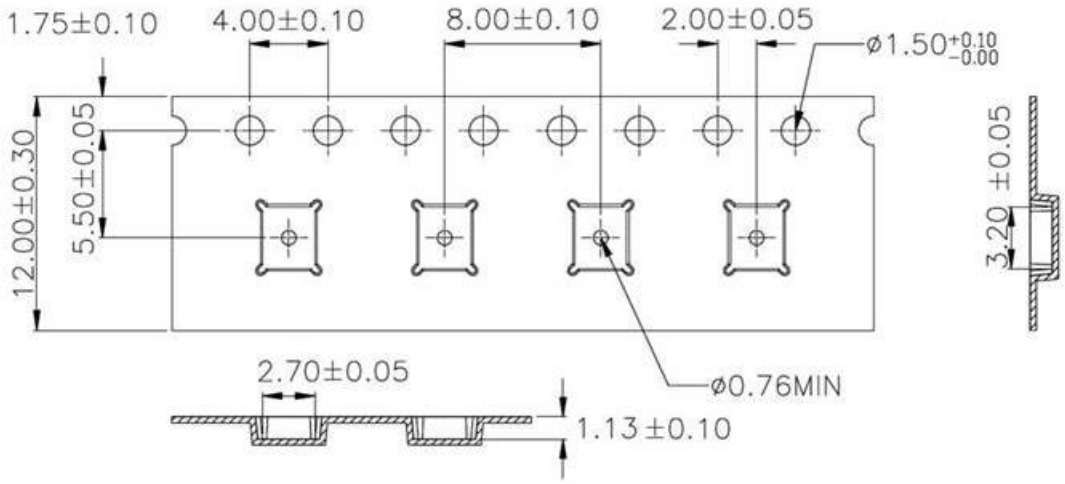


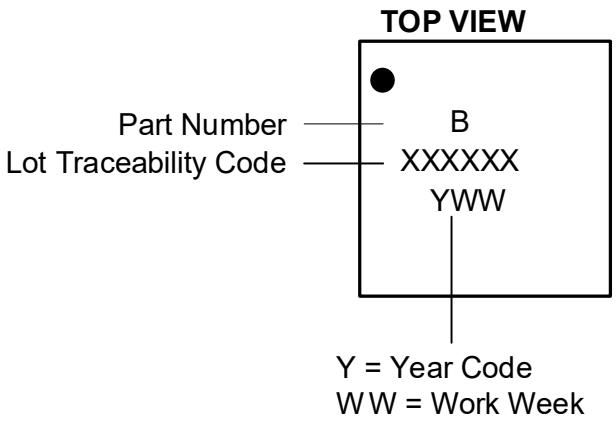
Figure 15. Tape Dimensions with T-3488 Device Package

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12 PART NUMBER PACKAGE MARKING

The part number package marking for T-3488 devices is summarized below:



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13 USE NOTES

13.1 READING SENSE REGISTER (SREG) DATA

The following procedure should be used to read Sense Register (SREG) data. Data is in Little Endian format.

User sets the value of SREG_RD_CFG[6:0] register-field to determine what sensor data they want to read, and then they read SREG_DATA register repeatedly to get the desired sensor data.

For example, to read gyroscope and accelerometer data for all three axes and also temperature data, set SREG_RD_CFG to 1111111. Reading SREG_DATA repeatedly will then provide the following.

Byte seq	SREG_RD_CFG	Little Endian Data (byte)
0	[0]=1	Ax0
1	[0]=1	Ax1
2	[1]=1	Ay0
3	[1]=1	Ay1
4	[2]=1	Az0
5	[2]=1	Az1
6	[3]=1	Gx0
7	[3]=1	Gx1
8	[4]=1	Gy0
9	[4]=1	Gy1
10	[5]=1	Gz0
11	[5]=1	Gz1
12	[6]=1	Tmp0
13	[6]=1	Tmp1
14 or more		0x8000

As another example, if the user only wants to read the Gyro data, then they can set SREG_RD_CFG[6:0] to 0111000, and then read the 6 bytes of Gyro data in the following order:

Byte seq	SREG_RD_CFG	Little Endian Data (byte)
0	[3]=1	Gx0
1	[3]=1	Gx1
2	[4]=1	Gy0
3	[4]=1	Gy1
4	[5]=1	Gz0
5	[5]=1	Gz1
6 or more		0x8000

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As yet another example, if the user only wants to read Accel axes X and Y, Gyro axis X, and the Temp sensor data, then they can set SREG_RD_CFG[6:0] to 1001011, and then read the 8 bytes in the following order:

Byte seq	SREG_RD_CFG	Little Endian Data (byte)
0	[0]=1	Ax0
1	[0]=1	Ax1
2	[1]=1	Ay0
3	[1]=1	Ay1
4	[3]=1	Gx0
5	[3]=1	Gx1
6	[6]=1	Tmp0
7	[6]=1	Tmp1
8 or more		0x8000

If user reads more bytes from SREG_DATA than the configured sequence within the same burst read, then all the additional bytes will have “invalid data code” of 0x8000.

Every new burst read of SREG_DATA starts with byte #0 in the sequence of the tables above. If the user does multiple burst reads of SREG_DATA between 2 ODRs, then they will read the same sensor data information. There is no issue if the user ends the burst read before reading all the bytes in the sequence, but when the user starts a new burst read of SREG_DATA the sequence will restart at byte #0. If an ODR occurs while a burst read of SREG_DATA is in progress, then the remaining bytes of the burst read in progress will remain coherent with the bytes read at the beginning of the burst read, and the sensor data for the new ODR will be available at the next burst read.

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14 INDIRECT REGISTER ACCESS

14.1 HOST INDIRECT ACCESS REGISTER (IREG)

An IREG is a register or a memory storage element that is not addressed directly by a 7-bit address. IREGs can only be addressed using an internal 16-bit address. Indirect register access procedures described in this section must be used to access all IREGs.

The host configures the internal 16-bit address by programming following registers:
{ireg_addr_15_8[7:0], ireg_addr_7_0[7:0]}.

14.2 GENERAL RULES FOR ACCESSING IREG

1. Burst-write and burst-read operations are not supported when accessing IREGs from the host.
2. Reading of an IREG is done on a read-pre-fetch basis (details in IREG READ section below).
3. A minimum wait time (refer to section MINIMUM WAIT TIME GAP below for details) is required between two consecutive read/write access to an IREG.

14.3 MINIMUM WAIT TIME-GAP

The minimum time gap between two consecutive IREG accesses for various IREG components is 4µs.

14.4 IREG WRITE

Procedure for writing to an IREG.

1. The host specifies the destination address of an IREG by programming IREG_ADDR_7_0, IREG_ADDR_15_8.
    a. If host wants to access a register in IMEM_SRAM, it should add base address 0x0000 to the address of that register shown in the IMEM_SRAM registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    b. If host wants to access a register in IMEM_SRAM_APEX, it should add base address 0x0000 to the address of that register shown in the IMEM_SRAM_APEX registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    c. If host wants to access a register in IMEM_SRAM_STC, it should add base address 0x0000 to the address of that register shown in the IMEM_SRAM_STC registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    d. If host wants to access a register in IMEM_SIGP, it should add base address 0x4000 to the address of that register shown in the IMEM_SIGP registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    e. If host wants to access a register in IPREG_BAR, it should add base address 0xA000 to the address of that register shown in the IPREG_BAR registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    f. If host wants to access a register in IPREG_SYS1, it should add base address 0xA400 to the address of that register shown in the IPREG_SYS1 registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    g. If host wants to access a register in IPREG_SYS2, it should add base address 0xA500 to the address of that register shown in the IPREG_SYS2 registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    h. If host wants to access a register in IPREG_TOP1, it should add base address 0xA200 to the address of that register shown in the IPREG_TOP1 registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
2. The host programs the write data to the IREG_DATA register.
3. The above programming steps must be performed in a single burst-write transaction to prevent an un-intended read-pre-fetch operation.
4. After the IREG_DATA register is written, an internal operation is triggered to pass the contents from the IREG_DATA register to a register pointed by {IREG_ADDR_7_0, IREG_ADDR_15_8}.
5. After the contents from the IREG_DATA register is written to the selected register, the internal 16-bit address is auto-incremented.

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6. After a minimum wait time-gap, the host can write to the IREG_DATA register again, which is effectively writing to the register pointed by the post-auto-incremented address.
7. Or, after a minimum wait time-gap, the host can program a new destination address for the next write operation.

14.5 IREG READ

Procedure for reading from an IREG.

1. The host specifies the destination address of an IREG by programming IREG_ADDR_7_0, IREG_ADDR_15_8.
    a. If host wants to access a register in IMEM_SRAM_APEX, it should add base address 0x0000 to the address of that register shown in the IMEM_SRAM_APEX registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    b. If host wants to access a register in IMEM_SRAM_STC, it should add base address 0x0000 to the address of that register shown in the IMEM_SRAM_STC registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    c. If host wants to access a register in IMEM_SIGP, it should add base address 0x4000 to the address of that register shown in the IMEM_SIGP registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    d. If host wants to access a register in IPREG_BAR, it should add base address 0xA000 to the address of that register shown in the IPREG_BAR registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    e. If host wants to access a register in IPREG_SYS1, it should add base address 0xA400 to the address of that register shown in the IPREG_SYS1 registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    f. If host wants to access a register in IPREG_SYS2, it should add base address 0xA500 to the address of that register shown in the IPREG_SYS2 registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    g. If host wants to access a register in IPREG_TOP1, it should add base address 0xA200 to the address of that register shown in the IPREG_TOP1 registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
2. Upon the CSB=1 (SPI) or STOP (I2C) after the above programming, an internal read-pre-fetch operation is triggered.
3. The internal read-pre-fetch operation returns the desired data, which is saved to the IREG_DATA register.
4. After a minimum wait time-gap, the host reads the IREG_DATA register to retrieve the read-data.
5. After the host reads the IREG_DATA register, the internal 16-bit address is auto-incremented, and another internal read-pre-fetch is automatically triggered, to fetch data from the IREG register pointed to by the post-auto-incremented address.
6. After a minimum wait time-gap, the host can either read the IREG_DATA register to get the read-data from the next address location, or it can program a new read address.

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15 REGISTER MAP

This section lists the register map for the T-3488, for user bank DREG_BANK1, IMEM_SRAM_APEX, IMEM_SRAM_STC, IMEM_SIGP, IPREG_BAR, IPREG_SYS1, IPREG_SYS2, and IPREG_TOP1.

15.1 USER BANK DREG_BANK1 REGISTER MAP

ADDR (HEX)	ADDR (DEC)	REGISTER NAME	SERIAL I/F	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00	00	FIFO_COUNT	R	FIFO_CNT[7:0]							
01	01	FIFO_DATA	R	FIFO_DATA[7:0]							
02	02	SREG_CONFIG0	R/W	SREG_RD_CFG[6:0]							-
03	03	SREG_DATA	R	SREG_DATA[7:0]							
06	06	FIFO_CONFIG1	R/W	FIFO_WM_TH[7:0]							
07	07	FIFO_CONFIG2	R/W	-					FIFO_WR_WM_GT_TH[0]	MIN_FREE_SPACE[1:0]	
08	08	FSD_CONFIG0	R/W	-			FIFO_FLUSH[0]	FIFO_MODE[1:0]		-	
09	09	SMC_TICK_PER_FRC_0	R/W	TICK_PER_FRC[7:0]							
0A	10	SMC_TICK_PER_FRC_1	R/W	-							TICK_PER_FRC[8]
0B	11	SMC_TICK_PER_FRC_SUB	R/W	-			TICK_PER_FRC_SUB[4:0]				
0C	12	ACCEL_CONFIG0	R/W	-	SREG_UI_ACCEL_FS_SEL[2:0]			ACCEL_ODR[3:0]			
0D	13	GYRO_CONFIG0	R/W	SREG_UI_GYRO_FS_SEL[3:0]				GYRO_ODR[3:0]			
0E	14	ODR_DECIMATE_CONFIG	R/W	GYRO_FIFO_ODR_DEC[3:0]				ACCEL_FIFO_ODR_DEC[3:0]			
0F	15	PWR_MGMT0	R/W	-			ACCEL_LP_CLK_SEL[0]	GYRO_MODE[1:0]		ACCEL_MODE[1:0]	
10	16	PWR_MGMT1	R	-		GYRO_UI_STATUS_PM[1:0]		ACCEL_UI_STATUS_PM[1:0]		GYRO_UI_STATUS_CONF_INVALID[0]	ACCEL_UI_STATUS_CONF_INVALID[0]
11	17	SMC_ODR_STAT	R	GYRO_AP_STATUS_ODR[3:0]				ACCEL_AP_STATUS_ODR[3:0]			
12	18	INT1_CONFIG0	R/W	-					INT1_DURATION[0]	INT1_INTERRUPT_POLARITY[0]	INT1_INTERRUPT_MODE[0]
13	19	INT1_CONFIG1	R/W	-		INT1_EN_GYRO_STALL[0]	INT1_EN_APEX_EVENT[0]	INT1_EN_I3C_PROTOCOL_ERR[0]	INT1_EN_FIFO_FULL[0]	INT1_EN_FIFO_THS[0]	INT1_EN_DRDY[0]
14	20	INT2_CONFIG0	R/W	-					INT2_DURATION[0]	INT2_INTERRUPT_POLARITY[0]	INT2_INTERRUPT_MODE[0]
15	21	INT2_CONFIG1	R/W	-		INT2_EN_GYRO_STALL[0]	INT2_EN_APEX_EVENT[0]	INT2_EN_I3C_PROTOCOL_ERR[0]	INT2_EN_FIFO_FULL[0]	INT2_EN_FIFO_THS[0]	INT2_EN_DRDY[0]
16	22	IBI_CONFIG0	R/W	-		IBI_INT_EN_GYRO_STALL[0]	IBI_INT_EN_APEX_EVENT[0]	IBI_INT_EN_I3C_PROTOCOL_ERR[0]	IBI_INT_EN_FIFO_FULL[0]	IBI_INT_EN_FIFO_THS[0]	IBI_INT_EN_DRDY[0]
19	25	INT1_STATUS	R/C	-		INT1_STATUS_GYRO_STALL[0]	INT1_STATUS_APEX_EVENT[0]	INT1_STATUS_I3C_PROTOCOL_ERR[0]	INT1_STATUS_FIFO_FULL[0]	INT1_STATUS_FIFO_THS[0]	INT1_STATUS_DRDY[0]
1C	28	INT2_STATUS	R/C	-		INT2_STATUS_GYRO_STALL[0]	INT2_STATUS_APEX_EVENT[0]	INT2_STATUS_I3C_PROTOCOL_ERR[0]	INT2_STATUS_FIFO_FULL[0]	INT2_STATUS_FIFO_THS[0]	INT2_STATUS_DRDY[0]
1F	31	IBI_STATUS	R/C	-		IBI_INT_STATUS_GYRO_STALL[0]	IBI_INT_STATUS_APEX_EVENT[0]	IBI_INT_STATUS_I3C_PROTOCOL_ERR[0]	IBI_INT_STATUS_FIFO_FULL[0]	IBI_INT_STATUS_FIFO_THS[0]	IBI_INT_STATUS_DRDY[0]
25	37	INT_PAD_CONFIG	R/W	-						INT2_DRIVE[0]	INT1_DRIVE[0]
26	38	PAD_SLEW0	R/W	-		PADS_SPI_SLEW[2:0]			PADS_SLEW[2:0]		
27	39	PAD_SLEW1	R/W	-		PADS_SDR_SLEW[2:0]			PADS_I2C_SLEW[2:0]		
28	40	PAD_DELAY	R/W	GLITCH_FILTER_DIS[0]	I3C_SDA_OUT_DLY[2:0]			I2C_SDA_OUT_DLY[3:0]			
2A	42	EDMP_APEX_CONFIG	R/W	LOWG_DET_EN[0]	HIGHG_DET_EN[0]	-	TAP_DET_EN[0]	B2S_DET_EN[0]	FF_DET_EN[0]	WOM_DET_EN[0]	TILT_DET_EN[0]
2B	43	EDMP_CFG_MISC	R/W	-					APEX_PWR_SAVE_EN[0]	FIFO_GYRO_EN[0]	FIFO_ACCEL_EN[0]

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ADDR (HEX)	ADDR (DEC)	REGISTER NAME	SERIAL I/F	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
2E	46	EDMP_APEX_STATUS0	R/C	REV_B2S_APEX_STATUS[0]	B2S_APEX_STATUS[0]	LOWG_APEX_STATUS[0]	HIGHG_APEX_STATUS[0]	-	FF_APEX_STATUS[0]	INACTIVE_APEX_STATUS[0]	ACTIVE_APEX_STATUS[0]
2F	47	EDMP_APEX_STATUS1	R/C	-					TAP_APEX_STATUS[0]	TILT_APEX_STATUS[0]	WOM_APEX_STATUS[0]
31	49	EDMP_MODE_STATUS	R	EDMP_BUSY[0]	-			EDMP_FIFO_MODE[1:0]		-	
72	114	WHOAMI	R	WHOAMI[7:0]							
77	119	INTF_CONFIG0	R/W	-						AP_SPI_34_MODE[0]	AP_SPI_MODE[0]
7C	124	IREG_ADDR_15_8	R/W	IREG_ADDR_15_8[7:0]							
7D	125	IREG_ADDR_7_0	R/W	IREG_ADDR_7_0[7:0]							
7E	126	IREG_DATA	R/W	IREG_DATA[7:0]							
7F	127	REG_MISC2	R/W	-					SOFT_RST[0]	IREG_AUTOINC[0]	IREG_DONE[0]

15.2 USER BANK IMEM_SRAM_APEX REGISTER MAP

ADDR (HEX)	ADDR (DEC)	REGISTER NAME	SERIAL I/F	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
D2	210	IMEM_SRAM_APEX_REG_210	R/W	FF_DURATION[7:0]							
D3	211	IMEM_SRAM_APEX_REG_211	R/W	FF_DURATION[15:8]							
D4	212	IMEM_SRAM_APEX_REG_212	R/W	ODR_B2S[7:0]							
D5	213	IMEM_SRAM_APEX_REG_213	R/W	ODR_B2S[15:8]							
D6	214	IMEM_SRAM_APEX_REG_214	R/W	ODR_AID[7:0]							
D7	215	IMEM_SRAM_APEX_REG_215	R/W	ODR_AID[15:8]							
D8	216	IMEM_SRAM_APEX_REG_216	R/W	WOM_STATE[7:0]							
D9	217	IMEM_SRAM_APEX_REG_217	R/W	TILT_RESET_EN[7:0]							
DA	218	IMEM_SRAM_APEX_REG_218	R/W	ODR_TILT[7:0]							
DB	219	IMEM_SRAM_APEX_REG_219	R/W	ODR_TILT[15:8]							
EA	234	IMEM_SRAM_APEX_REG_234	R/W	TAP_NUM[7:0]							
EB	235	IMEM_SRAM_APEX_REG_235	R/W	TAP_AXIS[7:0]							
EC	236	IMEM_SRAM_APEX_REG_236	R/W	TAP_DIR[7:0]							
ED	237	IMEM_SRAM_APEX_REG_237	R/W	DOUBLE_TAP_TIMING[7:0]							
EE	238	IMEM_SRAM_APEX_REG_238	R/W	TRIPLE_TAP_TIMING[7:0]							
104	260	IMEM_SRAM_APEX_REG_260	R/W	WOM_THRESHOLD_X[7:0]							
105	261	IMEM_SRAM_APEX_REG_261	R/W	WOM_THRESHOLD_X[15:8]							
106	262	IMEM_SRAM_APEX_REG_262	R/W	WOM_THRESHOLD_Y[7:0]							
107	263	IMEM_SRAM_APEX_REG_263	R/W	WOM_THRESHOLD_Y[15:8]							
108	264	IMEM_SRAM_APEX_REG_264	R/W	WOM_THRESHOLD_Z[7:0]							
109	265	IMEM_SRAM_APEX_REG_265	R/W	WOM_THRESHOLD_Z[15:8]							
10A	266	IMEM_SRAM_APEX_REG_266	R/W	WOM_WAIT_TIME[7:0]							
10B	267	IMEM_SRAM_APEX_REG_267	R/W	WOM_WAIT_TIME[15:8]							

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ADDR (HEX)	ADDR (DEC)	REGISTER NAME	SERIAL I/F	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
10C	268	IMEM_SRAM_APEX_REG_268	R/W	WOM_ANDORLOGIC[7:0]							
118	280	IMEM_SRAM_APEX_REG_280	R/W	AID_UPDATEWIN[7:0]							
119	281	IMEM_SRAM_APEX_REG_281	R/W	AID_UPDATEWIN[15:8]							
11A	282	IMEM_SRAM_APEX_REG_282	R/W	AID_UPDATEWIN[23:16]							
11B	283	IMEM_SRAM_APEX_REG_283	R/W	AID_UPDATEWIN[31:24]							
11C	284	IMEM_SRAM_APEX_REG_284	R/W	AID_ENABLE_OUTPUT[7:0]							
11D	285	IMEM_SRAM_APEX_REG_285	R/W	AID_DISABLE_MULTIPLE_OUTPUT[7:0]							
13C	316	IMEM_SRAM_APEX_REG_316	R/W	FF_MIN_DURATION[7:0]							
13D	317	IMEM_SRAM_APEX_REG_317	R/W	FF_MIN_DURATION[15:8]							
13E	318	IMEM_SRAM_APEX_REG_318	R/W	FF_MIN_DURATION[23:16]							
13F	319	IMEM_SRAM_APEX_REG_319	R/W	FF_MIN_DURATION[31:24]							
140	320	IMEM_SRAM_APEX_REG_320	R/W	FF_MAX_DURATION[7:0]							
141	321	IMEM_SRAM_APEX_REG_321	R/W	FF_MAX_DURATION[15:8]							
142	322	IMEM_SRAM_APEX_REG_322	R/W	FF_MAX_DURATION[23:16]							
143	323	IMEM_SRAM_APEX_REG_323	R/W	FF_MAX_DURATION[31:24]							
144	324	IMEM_SRAM_APEX_REG_324	R/W	FF_DEBOUNCE_DURATION[7:0]							
145	325	IMEM_SRAM_APEX_REG_325	R/W	FF_DEBOUNCE_DURATION[15:8]							
146	326	IMEM_SRAM_APEX_REG_326	R/W	FF_DEBOUNCE_DURATION[23:16]							
147	327	IMEM_SRAM_APEX_REG_327	R/W	FF_DEBOUNCE_DURATION[31:24]							
14E	334	IMEM_SRAM_APEX_REG_334	R/W	LOWG_PEAK_TH[7:0]							
14F	335	IMEM_SRAM_APEX_REG_335	R/W	LOWG_PEAK_TH[15:8]							
150	336	IMEM_SRAM_APEX_REG_336	R/W	LOWG_PEAK_TH_HYST[7:0]							
151	337	IMEM_SRAM_APEX_REG_337	R/W	LOWG_PEAK_TH_HYST[15:8]							
152	338	IMEM_SRAM_APEX_REG_338	R/W	LOWG_TIME_TH[7:0]							
153	339	IMEM_SRAM_APEX_REG_339	R/W	LOWG_TIME_TH[15:8]							
15A	346	IMEM_SRAM_APEX_REG_346	R/W	HIGHG_PEAK_TH[7:0]							
15B	347	IMEM_SRAM_APEX_REG_347	R/W	HIGHG_PEAK_TH[15:8]							
15C	348	IMEM_SRAM_APEX_REG_348	R/W	HIGHG_PEAK_TH_HYST[7:0]							
15D	349	IMEM_SRAM_APEX_REG_349	R/W	HIGHG_PEAK_TH_HYST[15:8]							
15E	350	IMEM_SRAM_APEX_REG_350	R/W	HIGHG_TIME_TH[7:0]							
15F	351	IMEM_SRAM_APEX_REG_351	R/W	HIGHG_TIME_TH[15:8]							
16C	364	IMEM_SRAM_APEX_REG_364	R/W	B2S_MOUNTING_MATRIX[7:0]							
170	368	IMEM_SRAM_APEX_REG_368	R/W	B2S_DEV_NORM_MAX[7:0]							
171	369	IMEM_SRAM_APEX_REG_369	R/W	B2S_DEV_NORM_MAX[15:8]							

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ADDR (HEX)	ADDR (DEC)	REGISTER NAME	SERIAL I/F	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
172	370	IMEM_SRAM_APEX_REG_370	R/W	B2S_DEV_NORM_MAX[23:16]							
173	371	IMEM_SRAM_APEX_REG_371	R/W	B2S_DEV_NORM_MAX[31:24]							
174	372	IMEM_SRAM_APEX_REG_372	R/W	B2S_SIN_LIMIT[7:0]							
175	373	IMEM_SRAM_APEX_REG_373	R/W	B2S_SIN_LIMIT[15:8]							
176	374	IMEM_SRAM_APEX_REG_374	R/W	B2S_SIN_LIMIT[23:16]							
177	375	IMEM_SRAM_APEX_REG_375	R/W	B2S_SIN_LIMIT[31:24]							
178	376	IMEM_SRAM_APEX_REG_376	R/W	B2S_FAST_MOTION_AGE_LIMIT[7:0]							
179	377	IMEM_SRAM_APEX_REG_377	R/W	B2S_FAST_MOTION_AGE_LIMIT[15:8]							
17A	378	IMEM_SRAM_APEX_REG_378	R/W	B2S_FAST_MOTION_AGE_LIMIT[23:16]							
17B	379	IMEM_SRAM_APEX_REG_379	R/W	B2S_FAST_MOTION_AGE_LIMIT[31:24]							
17C	380	IMEM_SRAM_APEX_REG_380	R/W	B2S_FAST_LIMIT[7:0]							
17D	381	IMEM_SRAM_APEX_REG_381	R/W	B2S_FAST_LIMIT[15:8]							
17E	382	IMEM_SRAM_APEX_REG_382	R/W	B2S_FAST_LIMIT[23:16]							
17F	383	IMEM_SRAM_APEX_REG_383	R/W	B2S_FAST_LIMIT[31:24]							
180	384	IMEM_SRAM_APEX_REG_384	R/W	B2S_FAST_MOTION_TIME_LIMIT[7:0]							
181	385	IMEM_SRAM_APEX_REG_385	R/W	B2S_FAST_MOTION_TIME_LIMIT[15:8]							
182	386	IMEM_SRAM_APEX_REG_386	R/W	B2S_FAST_MOTION_TIME_LIMIT[23:16]							
183	387	IMEM_SRAM_APEX_REG_387	R/W	B2S_FAST_MOTION_TIME_LIMIT[31:24]							
184	388	IMEM_SRAM_APEX_REG_388	R/W	B2S_AGE_LIMIT[7:0]							
185	389	IMEM_SRAM_APEX_REG_389	R/W	B2S_AGE_LIMIT[15:8]							
186	390	IMEM_SRAM_APEX_REG_390	R/W	B2S_AGE_LIMIT[23:16]							
187	391	IMEM_SRAM_APEX_REG_391	R/W	B2S_AGE_LIMIT[31:24]							
188	392	IMEM_SRAM_APEX_REG_392	R/W	B2S_STATIC_LIMIT[7:0]							
189	393	IMEM_SRAM_APEX_REG_393	R/W	B2S_STATIC_LIMIT[15:8]							
18A	394	IMEM_SRAM_APEX_REG_394	R/W	B2S_STATIC_LIMIT[23:16]							
18B	395	IMEM_SRAM_APEX_REG_395	R/W	B2S_STATIC_LIMIT[31:24]							
18C	396	IMEM_SRAM_APEX_REG_396	R/W	B2S_THR_COS_ANGLE[7:0]							
18D	397	IMEM_SRAM_APEX_REG_397	R/W	B2S_THR_COS_ANGLE[15:8]							
18E	398	IMEM_SRAM_APEX_REG_398	R/W	B2S_THR_COS_ANGLE[23:16]							
18F	399	IMEM_SRAM_APEX_REG_399	R/W	B2S_THR_COS_ANGLE[31:24]							
190	400	IMEM_SRAM_APEX_REG_400	R/W	B2S_REVB2S_LATENCY_THR[7:0]							
191	401	IMEM_SRAM_APEX_REG_401	R/W	B2S_REVB2S_LATENCY_THR[15:8]							
192	402	IMEM_SRAM_APEX_REG_402	R/W	B2S_REVB2S_LATENCY_THR[23:16]							
193	403	IMEM_SRAM_APEX_REG_403	R/W	B2S_REVB2S_LATENCY_THR[31:24]							

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194	404	IMEM_SRAM_APEX_REG_404	R/W	B2S_REVB2S_X_LIMIT[7:0]							
195	405	IMEM_SRAM_APEX_REG_405	R/W	B2S_REVB2S_X_LIMIT[15:8]							
196	406	IMEM_SRAM_APEX_REG_406	R/W	B2S_REVB2S_X_LIMIT[23:16]							
197	407	IMEM_SRAM_APEX_REG_407	R/W	B2S_REVB2S_X_LIMIT[31:24]							
198	408	IMEM_SRAM_APEX_REG_408	R/W	B2S_SIN_FLAT_ANGLE[7:0]							
199	409	IMEM_SRAM_APEX_REG_409	R/W	B2S_SIN_FLAT_ANGLE[15:8]							
19A	410	IMEM_SRAM_APEX_REG_410	R/W	B2S_SIN_FLAT_ANGLE[23:16]							
19B	411	IMEM_SRAM_APEX_REG_411	R/W	B2S_SIN_FLAT_ANGLE[31:24]							
19C	412	IMEM_SRAM_APEX_REG_412	R/W	B2S_TIMER_FLAT_REJECT[7:0]							
19D	413	IMEM_SRAM_APEX_REG_413	R/W	B2S_TIMER_FLAT_REJECT[15:8]							
19E	414	IMEM_SRAM_APEX_REG_414	R/W	B2S_TIMER_FLAT_REJECT[23:16]							
19F	415	IMEM_SRAM_APEX_REG_415	R/W	B2S_TIMER_FLAT_REJECT[31:24]							
282	642	IMEM_SRAM_APEX_REG_642	R/W	TILT_WAIT_TIME[7:0]							
283	643	IMEM_SRAM_APEX_REG_643	R/W	TILT_WAIT_TIME[15:8]							
284	644	IMEM_SRAM_APEX_REG_644	R/W	TILT_ANGLE_TH[7:0]							
285	645	IMEM_SRAM_APEX_REG_645	R/W	TILT_ANGLE_TH[15:8]							
286	646	IMEM_SRAM_APEX_REG_646	R/W	TILT_ANGLE_TH[23:16]							
287	647	IMEM_SRAM_APEX_REG_647	R/W	TILT_ANGLE_TH[31:24]							
288	648	IMEM_SRAM_APEX_REG_648	R/W	TAP_MIN_JERK[7:0]							
289	649	IMEM_SRAM_APEX_REG_649	R/W	TAP_MIN_JERK[15:8]							
28A	650	IMEM_SRAM_APEX_REG_650	R/W	TAP_TMAX[7:0]							
28B	651	IMEM_SRAM_APEX_REG_651	R/W	TAP_TMAX[15:8]							
28C	652	IMEM_SRAM_APEX_REG_652	R/W	TAP_TMIN[7:0]							
28D	653	IMEM_SRAM_APEX_REG_653	R/W	TAP_SMUDGE_REJECT_THR[7:0]							
28E	654	IMEM_SRAM_APEX_REG_654	R/W	TAP_MAX_PEAK_TOL[7:0]							
28F	655	IMEM_SRAM_APEX_REG_655	R/W	TAP_TAVG[7:0]							
290	656	IMEM_SRAM_APEX_REG_656	R/W	TAP_MAX[7:0]							
291	657	IMEM_SRAM_APEX_REG_657	R/W	TAP_MIN[7:0]							
292	658	IMEM_SRAM_APEX_REG_658	R/W	TAP_ODR[7:0]							

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15.3 USER BANK IMEM_SRAM_STC REGISTER MAP

ADDR (HEX)	ADDR (DEC)	REGISTER NAME	SERIAL I/F	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
700	1792	IMEM_SRAM_STC_REG_1792	R/W	GYRO_X_STR_FT[7:0]							
701	1793	IMEM_SRAM_STC_REG_1793	R/W	GYRO_X_STR_FT[15:8]							
702	1794	IMEM_SRAM_STC_REG_1794	R/W	GYRO_Y_STR_FT[7:0]							
703	1795	IMEM_SRAM_STC_REG_1795	R/W	GYRO_Y_STR_FT[15:8]							
704	1796	IMEM_SRAM_STC_REG_1796	R/W	GYRO_Z_STR_FT[7:0]							
705	1797	IMEM_SRAM_STC_REG_1797	R/W	GYRO_Z_STR_FT[15:8]							
706	1798	IMEM_SRAM_STC_REG_1798	R/W	ACCEL_X_STR_FT[7:0]							
707	1799	IMEM_SRAM_STC_REG_1799	R/W	ACCEL_X_STR_FT[15:8]							
708	1800	IMEM_SRAM_STC_REG_1800	R/W	ACCEL_Y_STR_FT[7:0]							
709	1801	IMEM_SRAM_STC_REG_1801	R/W	ACCEL_Y_STR_FT[15:8]							
70A	1802	IMEM_SRAM_STC_REG_1802	R/W	ACCEL_Z_STR_FT[7:0]							
70B	1803	IMEM_SRAM_STC_REG_1803	R/W	ACCEL_Z_STR_FT[15:8]							

15.4 USER BANK IMEM_SIGP REGISTER MAP

ADDR (HEX)	ADDR (DEC)	REGISTER NAME	SERIAL I/F	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
80	128	IMEM_SIGP_REG_128	R/W	ACCEL_X_GOS_GAIN_USER[7:0]							
81	129	IMEM_SIGP_REG_129	R/W	ACCEL_X_GOS_GAIN_USER[15:8]							
94	148	IMEM_SIGP_REG_148	R/W	ACCEL_X_GOS_OFF_USER[7:0]							
95	149	IMEM_SIGP_REG_149	R/W	ACCEL_X_GOS_OFF_USER[15:8]							
148	328	IMEM_SIGP_REG_328	R/W	ACCEL_Y_GOS_GAIN_USER[7:0]							
149	329	IMEM_SIGP_REG_329	R/W	ACCEL_Y_GOS_GAIN_USER[15:8]							
15C	348	IMEM_SIGP_REG_348	R/W	ACCEL_Y_GOS_OFF_USER[7:0]							
15D	349	IMEM_SIGP_REG_349	R/W	ACCEL_Y_GOS_OFF_USER[15:8]							
210	528	IMEM_SIGP_REG_528	R/W	ACCEL_Z_GOS_GAIN_USER[7:0]							
211	529	IMEM_SIGP_REG_529	R/W	ACCEL_Z_GOS_GAIN_USER[15:8]							
224	548	IMEM_SIGP_REG_548	R/W	ACCEL_Z_GOS_OFF_USER[7:0]							
225	549	IMEM_SIGP_REG_549	R/W	ACCEL_Z_GOS_OFF_USER[15:8]							
2D8	728	IMEM_SIGP_REG_728	R/W	GYRO_X_GOS_GAIN_USER[7:0]							
2D9	729	IMEM_SIGP_REG_729	R/W	GYRO_X_GOS_GAIN_USER[15:8]							
2EC	748	IMEM_SIGP_REG_748	R/W	GYRO_X_GOS_OFF_USER[7:0]							
2ED	749	IMEM_SIGP_REG_749	R/W	GYRO_X_GOS_OFF_USER[15:8]							
3D0	976	IMEM_SIGP_REG_976	R/W	GYRO_Y_GOS_GAIN_USER[7:0]							
3D1	977	IMEM_SIGP_REG_977	R/W	GYRO_Y_GOS_GAIN_USER[15:8]							
3E4	996	IMEM_SIGP_REG_996	R/W	GYRO_Y_GOS_OFF_USER[7:0]							
3E5	997	IMEM_SIGP_REG_997	R/W	GYRO_Y_GOS_OFF_USER[15:8]							
4C8	1224	IMEM_SIGP_REG_1224	R/W	GYRO_Z_GOS_GAIN_USER[7:0]							
4C9	1225	IMEM_SIGP_REG_1225	R/W	GYRO_Z_GOS_GAIN_USER[15:8]							
4DC	1244	IMEM_SIGP_REG_1244	R/W	GYRO_Z_GOS_OFF_USER[7:0]							
4DD	1245	IMEM_SIGP_REG_1245	R/W	GYRO_Z_GOS_OFF_USER[15:8]							

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15.5 USER BANK IPREG_BAR REGISTER MAP

ADDR (HEX)	ADDR (DEC)	REGISTER NAME	SERIAL I/F	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
5E	94	IPREG_BAR_REG_94	R/W	PADS_AP_SCLK_PUD_TRIM_D2A[0]	PADS_AP_SCLK_PE_TRIM_D2A[0]	-	PADS_AP_CS_PUD_TRIM_D2A[0]	PADS_AP_CS_PE_TRIM_D2A[0]	-		
5F	95	IPREG_BAR_REG_95	R/W	-		PADS_AP_SDO_PUD_TRIM_D2A[0]	PADS_AP_SDO_PE_TRIM_D2A[0]	-	PADS_AP_SDI_PUD_TRIM_D2A[0]	PADS_AP_SDI_PE_TRIM_D2A[0]	-
ED	237	IPREG_BAR_REG_237	R/W	-				TEMP_FORCE_ON_RR_TIMING_TRIM_D2D[0]	-		

15.6 USER BANK IPREG_SYS1 REGISTER MAP

ADDR (HEX)	ADDR (DEC)	REGISTER NAME	SERIAL I/F	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
09	09	IPREG_SYS1_REG_9	R/W	-					GYRO_LPF_BW_SEL[2:0]		

15.7 USER BANK IPREG_SYS2 REGISTER MAP

ADDR (HEX)	ADDR (DEC)	REGISTER NAME	SERIAL I/F	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
06	06	IPREG_SYS2_REG_6	R/W	-					ACCEL_LPF_BW_SEL[2:0]		
08	08	IPREG_SYS2_REG_8	R/W	-				ACCEL_LP_AVG_SEL[3:0]			

15.8 USER BANK IPREG_TOP1 REGISTER MAP

ADDR (HEX)	ADDR (DEC)	REGISTER NAME	SERIAL I/F	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
06	06	I3C_CONFIG	R/W	-						IBI_EN[0]	SDR_EN[0]
07	07	SMC_CONTROL_0	R/W	-					ULP_ED_RCOSC_WU_TRIM[2:0]		
08	08	SMC_CONTROL_1	R/W	-			RESERVED	GYRO_AP_EN[0]	ACCEL_AP_EN[0]	EN_OFFGRID_MODE[0]	TEMP_DIS[0]
17	23	FIFO_CONFIG0	R/W	-						FIFO_DEPTH[1:0]	
18	24	SREG_CONFIG1	R/W	-				NXT_WR_BNK[1:0]		NXT_NEW_BNK[1:0]	
19	25	EDMP_INT_ENABLE	R/W	-						EDMP_INT_EN_ON_DEMAND_REQ[0]	EDMP_INT_EN_ODR_EVENT[0]
1B	27	EDMP_INT_STATUS	R/C	-						EDMP_INT_STATUS_ON_DEMAND_REQ[0]	EDMP_INT_STATUS_ODR_EVENT[0]
33	51	SELFTEST	R/W	-		EN_GZ_ST[0]	EN_GY_ST[0]	EN_GX_ST[0]	EN_AZ_ST[0]	EN_AY_ST[0]	EN_AX_ST[0]
E6	230	EDMP_PRGRM_IRQ0_0	R/W	PRGRM_STRT_ADDR_IRQ_0[7:0]							
E7	231	EDMP_PRGRM_IRQ0_1	R/W	-			PRGRM_STRT_ADDR_IRQ_0[12:8]				
E8	232	EDMP_SP_START_ADDR	R/W	-	SP_START_ADDR[6:0]						
E9	233	EDMP_CFG	RWS	-					EDMP_AUTH[0]	EDMP_INIT[0]	FORCED_ODR[0]

Detailed register descriptions are provided in the sections that follow.

Register fields marked as Reserved must not be modified by the user. The Reset Value of the register can be used to determine the default value of reserved register fields, and unless otherwise noted this default value must be maintained even if the values of other register fields are modified by the user.

In the sections that follow, some register fields are described as can be changed on-the-fly even if sensor is on. These are the only register fields that can be changed on-the-fly even if sensor is on. Register fields not described as such must not be changed on-the-fly if sensor is on.

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16 USER BANK DREG_BANK1 – DESCRIPTIONS

This section describes the function and contents of each register within user DREG_BANK1.

Note: The device powers up in sleep mode.

16.1 FIFO_COUNT

Name: FIFO_COUNT
Address: 00 (00h)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	FIFO_CNT[7:0]	[Supports Dynamic Change] FIFO data counter. It returns the number of unread frames inside the FIFO. Can be read anytime. Can be read as a single byte FIFO data count, or in a hybrid read, data count + data burst.

16.2 FIFO_DATA

Name: FIFO_DATA
Address: 01 (01h)
Serial IF: R
Reset value: 0x7F

BIT	NAME	FUNCTION
7:0	FIFO_DATA[7:0]	FIFO data read by serial interface.

16.3 SREG_CONFIG0

Name: SREG_CONFIG0
Address: 02 (02h)
Serial IF: R/W
Reset value: 0xFE

BIT	NAME	FUNCTION
7:1	SREG_RD_CFG[6:0]	[Supports Dynamic Change] SREG data read configuration: enables selected sensor data & axis for read out when SREG data is read by Host. If not enabled, that sensor data or sensor axis is skipped during SREG data read. Write by Host; Read by Hardware. Default, all sensors and axis enabled. [0]: if 1 accel X-axis data enabled; 0 not enabled. [1]: if 1 accel Y-axis data enabled; 0 not enabled. [2]: if 1 accel Z-axis data enabled; 0 not enabled. [3]: if 1 gyro X-axis data enabled; 0 not enabled. [4]: if 1 gyro Y-axis data enabled; 0 not enabled. [5]: if 1 gyro Z-axis data enabled; 0 not enabled. [6]: if 1 temperature data enabled; 0 not enabled. Can be changed on-the-fly.
0	-	Reserved

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16.4 SREG_DATA

Name: SREG_DATA
Address: 03 (03h)
Serial IF: R
Reset value: 0x80

BIT	NAME	FUNCTION
7:0	SREG_DATA[7:0]	SREG data read by serial interface.

16.5 FIFO_CONFIG1

Name: FIFO_CONFIG1
Address: 06 (06h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	FIFO_WM_TH[7:0]	[Supports Dynamic Change] FIFO watermark threshold. Can be changed on-the-fly. When set to 0, the watermark is disabled. New threshold register value will take effect after register is written.

16.6 FIFO_CONFIG2

Name: FIFO_CONFIG2
Address: 07 (07h)
Serial IF: R/W
Reset value: 0x02

BIT	NAME	FUNCTION
7:3	-	Reserved
2	FIFO_WR_WM_GT_TH[0]	Set write watermark interrupt generating condition. 0: write watermark interrupt generated when counter is equal to threshold 1: write watermark interrupt generated when counter is greater than or equal to threshold Can be changed when FIFO is disabled (Bypass mode)
1:0	MIN_FREE_SPACE[1:0]	[Supports Dynamic Change] Specifies the minimum frame free space permitted before full condition is detected: 2'b00: 0 FIFO frames 2'b01: 1 FIFO frames 2'b10: 2 FIFO frames 2'b11: 4 FIFO frames Can be changed when in bypass mode

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16.7 FSD_CONFIG0

Name: FSD_CONFIG0
Address: 08 (08h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:5	-	Reserved
4	FIFO_FLUSH[0]	[Supports Dynamic Change] FIFO flush command. When set high the FIFO read pointer is reset, and on SIFS read, 0x7F data is returned. Can be changed on-the-fly. The host should not program FIFO_FLUSH to a value of 0.
3:2	FIFO_MODE[1:0]	[Supports Dynamic Change] Set the FIFO operation mode. 2'b00: Bypass (disabled) 2'b01: Stream mode - Frames are overwritten when the FIFO full condition is reached. 2'b10: Stop-on-full mode - Frames are not stored in FIFO once the FIFO full condition is reached. 2'b11: Reserved Can be changed on-the-fly.
1:0	-	Reserved

16.8 SMC_TICK_PER_FRC_0

Name: SMC_TICK_PER_FRC_0
Address: 09 (09h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	TICK_PER_FRC[7:0]	Integer number of 2.016MHz clock cycles in the desired ODR Tick period for off-grid ODR

16.9 SMC_TICK_PER_FRC_1

Name: SMC_TICK_PER_FRC_1
Address: 10 (0Ah)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:1	-	Reserved
0	TICK_PER_FRC[8]	Integer number of 2.016MHz clock cycles in the desired ODR Tick period for off-grid ODR

16.10 SMC_TICK_PER_FRC_SUB

Name: SMC_TICK_PER_FRC_SUB
Address: 11 (0Bh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:5	-	Reserved
4:0	TICK_PER_FRC_SUB[4:0]	Fractional number (5 bits; 1 LSB = 1/32) of 2.016MHz clock cycles in the desired ODR Tick period for off-grid ODR

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16.11 ACCEL_CONFIG0

Name: ACCEL_CONFIG0
Address: 12 (0Ch)
Serial IF: R/W
Reset value: 0x06

BIT	NAME	FUNCTION
7	-	Reserved
6:4	SREG_UI_ACCEL_FS_SEL[2:0]	[Supports Dynamic Change] Set the UI/AP signal path accel full scale: 1: ±16g 2: ±8g 3: ±4g 4: ±2g
3:0	ACCEL_ODR[3:0]	[Supports Dynamic Change] Accelerometer Output Data Rate: 0: Reserved 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: 800Hz (LN) 6: 400Hz (LN/LP (default)) 7: 200Hz (LN/LP) 8: 100Hz (LN/LP) 9: 50Hz (LN/LP) 10: 25Hz (LN/LP) 11: 12.5Hz (LN/LP) 12: 6.25Hz (LP) 13: 3.125Hz (LP) 14: 1.5625Hz (LP) 15: 0.78125Hz (LP) This field can be changed on-the-fly even if accel sensor is already on

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16.12 GYRO_CONFIG0

Name: GYRO_CONFIG0
Address: 13 (0Dh)
Serial IF: R/W
Reset value: 0x06

BIT	NAME	FUNCTION
7:4	SREG_UI_GYRO_FS_SEL[3:0]	[Supports Dynamic Change] Set the UI/AP signal path gyro full scale 1: ±2000dps 2: ±1000dps 3: ±500dps 4: ±250dps Others: Reserved
3:0	GYRO_ODR[3:0]	[Supports Dynamic Change] Gyro Output Data Rate: 0: Reserved 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: 800Hz 6: 400Hz (default)) 7: 200Hz 8: 100Hz 9: 50Hz 10: 25Hz 11: 12.5Hz Others: Reserved This field can be changed on-the-fly even if gyro sensor is already on

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16.13 ODR_DECIMATE_CONFIG

Name: ODR_DECIMATE_CONFIG
Address: 14 (0Eh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:4	GYRO_FIFO_ODR_DEC[3:0]	Down-Sampling factor for the Gyro FIFO: 0000: 1 (as input ODR rate) 0001: 2 0010: 4 0011: 8 0100: 16 0101: 32 0110: 64 0111: 128 1000: 256 Others: Reserved The final rate will be GYRO_ODR/2^(GYRO_FIFO_ODR_DEC), with a minimum down-sampled rate equal to the minimum ODR.
3:0	ACCEL_FIFO_ODR_DEC[3:0]	Down-Sampling factor for the Accel FIFO: 0000: 1 (as input ODR rate) 0001: 2 0010: 4 0011: 8 0100: 16 0101: 32 0110: 64 0111: 128 1000: 256 Others: Reserved The final rate will be ACCEL_ODR/2^(ACCEL_FIFO_ODR_DEC), with a minimum down-sampled rate equal to the minimum ODR.

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16.14 PWR_MGMT0

Name: PWR_MGMT0
Address: 15 (0Fh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:5	-	Reserved
4	ACCEL_LP_CLK_SEL[0]	0: Selects wake-up oscillator for Accelerometer in LP mode 1: Selects RC oscillator for Accelerometer in LP mode
3:2	GYRO_MODE[1:0]	[Supports Dynamic Change] Gyroscope Power-Mode: 00: Off 01: Reserved 10: Reserved 11: Low Noise (LN) Mode
1:0	ACCEL_MODE[1:0]	[Supports Dynamic Change] Accelerometer Power-Mode: 00: Off 01: Reserved 10: Low Power (LP) Mode 11: Low Noise (LN) Mode

16.15 PWR_MGMT1

Name: PWR_MGMT1
Address: 16 (10h)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:6	-	Reserved
5:4	GYRO_UI_STATUS_PM[1:0]	Gyroscope Power-Mode Status: 00: Off 01: Reserved 10: Reserved 11: Low Noise (LN) Mode
3:2	ACCEL_UI_STATUS_PM[1:0]	Accelerometer Power-Mode Status: 00: Off 01: Reserved 10: Low Power (LP) Mode 11: Low Noise (LN) Mode
1	GYRO_UI_STATUS_CONF_INVALID[0]	Asserted if an invalid configuration is detected for the Gyroscope sensor at the UI/AP interface
0	ACCEL_UI_STATUS_CONF_INVALID[0]	Asserted if an invalid configuration is detected for the Accelerometer sensor at the UI/AP interface

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16.16 SMC_ODR_STAT

Name: SMC_ODR_STAT
Address: 17 (11h)
Serial IF: R
Reset value: 0x66

BIT	NAME	FUNCTION
7:4	GYRO_AP_STATUS_ODR[3:0]	Gyroscope Output Data Rate Status: 0: Reserved 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: 800Hz (LN) 6: 400Hz (default) 7: 200Hz 8: 100Hz 9: 50Hz 10: 25Hz 11: 12.5Hz Others: Reserved
3:0	ACCEL_AP_STATUS_ODR[3:0]	Accelerometer Output Data Rate Status: 0: Reserved 1: Reserved 2: Reserved 3: Reserved 4: Reserved 5: 800Hz (LN) 6: 400Hz (LN/LP (default)) 7: 200Hz (LN/LP) 8: 100Hz (LN/LP) 9: 50Hz (LN/LP) 10: 25Hz (LN/LP) 11: 12.5Hz (LN/LP) 12: 6.25Hz (LP) 13: 3.125Hz (LP) 14: 1.5625Hz (LP) 15: 0.78125Hz (LP)

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16.17 INT1_CONFIG0

Name: INT1_CONFIG0
Address: 18 (12h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:3	-	Reserved
2	INT1_DURATION[0]	INT1 Minimum Assertion and De-assertion Time 0: 100µs 1: 8µs Note: The setting can be changed when all the interrupt event sources are disabled.
1	INT1_INTERRUPT_POLARITY[0]	INT1 configuration bit to change the output interrupt polarity 0: Active low polarity interrupt 1: Active high polarity interrupt Note: The setting can be changed when all the interrupt event sources are disabled.
0	INT1_INTERRUPT_MODE[0]	INT1 configuration bit to change the interrupt mode 0: Level mode 1: Pulse mode Note: The setting can be changed when all the interrupt event sources are disabled.

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16.18 INT1_CONFIG1

Name: INT1_CONFIG1
Address: 19 (13h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:6	-	Reserved
5	INT1_EN_GYRO_STALL[0]	Gyroscope Stall Interrupt enable on INT1 0: Disable Interrupt 1: Enable Interrupt
4	INT1_EN_APEX_EVENT[0]	APEX Event Interrupt enable on INT1 0: Disable Interrupt 1: Enable Interrupt
3	INT1_EN_I3C_PROTOCOL_ERR[0]	I3C Protocol Error Interrupt enable on INT1 0: Disable Interrupt 1: Enable Interrupt
2	INT1_EN_FIFO_FULL[0]	FIFO Full Interrupt enable on INT1 0: Disable Interrupt 1: Enable Interrupt
1	INT1_EN_FIFO_THS[0]	FIFO Threshold Interrupt enable on INT1 0: Disable Interrupt 1: Enable Interrupt
0	INT1_EN_DRDY[0]	Data Ready Interrupt enable on INT1 0: Disable Interrupt 1: Enable Interrupt

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16.19 INT2_CONFIG0

Name: INT2_CONFIG0
Address: 20 (14h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:3	-	Reserved
2	INT2_DURATION[0]	INT2 Minimum Assertion and De-assertion Time 0: 100µs 1: 8µs Note: The setting can be changed when all the interrupt event sources are disabled.
1	INT2_INTERRUPT_POLARITY[0]	INT2 configuration bit to change the output interrupt polarity 0: Active low polarity interrupt 1: Active high polarity interrupt Note: The setting can be changed when all the interrupt event sources are disabled.
0	INT2_INTERRUPT_MODE[0]	INT2 configuration bit to change the interrupt mode 0: Level mode 1: Pulse mode Note: The setting can be changed when all the interrupt event sources are disabled.

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16.20 INT2_CONFIG1

Name: INT2_CONFIG1
Address: 21 (15h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:6	-	Reserved
5	INT2_EN_GYRO_STALL[0]	Gyroscope Stall Interrupt enable on INT2 0: Disable Interrupt 1: Enable Interrupt
4	INT2_EN_APEX_EVENT[0]	APEX Event Interrupt enable on INT2 0: Disable Interrupt 1: Enable Interrupt
3	INT2_EN_I3C_PROTOCOL_ERR[0]	I3C Protocol Error Interrupt enable on INT2 0: Disable Interrupt 1: Enable Interrupt
2	INT2_EN_FIFO_FULL[0]	FIFO Full Interrupt enable on INT2 0: Disable Interrupt 1: Enable Interrupt
1	INT2_EN_FIFO_THS[0]	FIFO Threshold Interrupt enable on INT2 0: Disable Interrupt 1: Enable Interrupt
0	INT2_EN_DRDY[0]	Data Ready Interrupt enable on INT2 0: Disable Interrupt 1: Enable Interrupt

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16.21 IBI_CONFIG0

Name: IBI_CONFIG0
Address: 22 (16h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:6	-	Reserved
5	IBI_INT_EN_GYRO_STALL[0]	Gyroscope Stall Interrupt enable on IBI 0: Disable Interrupt 1: Enable Interrupt
4	IBI_INT_EN_APEX_EVENT[0]	APEX Event Interrupt enable on IBI 0: Disable Interrupt 1: Enable Interrupt
3	IBI_INT_EN_I3C_PROTOCOL_ERR[0]	I3C Protocol Error Interrupt enable on IBI 0: Disable Interrupt 1: Enable Interrupt
2	IBI_INT_EN_FIFO_FULL[0]	FIFO Full Interrupt enable on IBI 0: Disable Interrupt 1: Enable Interrupt
1	IBI_INT_EN_FIFO_THS[0]	FIFO Threshold Interrupt enable on IBI 0: Disable Interrupt 1: Enable Interrupt
0	IBI_INT_EN_DRDY[0]	Data Ready Interrupt enable on IBI 0: Disable Interrupt 1: Enable Interrupt

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16.22 INT1_STATUS

Name: INT1_STATUS
Address: 25 (19h)
Serial IF: R/C
Reset value: 0x00

BIT	NAME	FUNCTION
7:6	-	Reserved
5	INT1_STATUS_GYRO_STALL[0]	Flags the occurrence of Gyro Stall event on INT1 0: Interrupt did not occur 1: Interrupt occurred
4	INT1_STATUS_APEX_EVENT[0]	Flags the occurrence of APEX event on INT1 0: Interrupt did not occur 1: Interrupt occurred
3	INT1_STATUS_I3C_PROTOCOL_ERR[0]	Flags the occurrence of I3C^{SM} Protocol Error event on INT1 0: Interrupt did not occur 1: Interrupt occurred
2	INT1_STATUS_FIFO_FULL[0]	Flags the occurrence of FIFO full event on INT1 0: Interrupt did not occur 1: Interrupt occurred
1	INT1_STATUS_FIFO_THS[0]	Flags the occurrence of FIFO count ≥ FIFO threshold event on INT1 0: Interrupt did not occur 1: Interrupt occurred
0	INT1_STATUS_DRDY[0]	Flags the occurrence of Data Ready event on INT1 0: Interrupt did not occur 1: Interrupt occurred

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16.23 INT2_STATUS

Name: INT2_STATUS
Address: 28 (1Ch)
Serial IF: R/C
Reset value: 0x00

BIT	NAME	FUNCTION
7:6	-	Reserved
5	INT2_STATUS_GYRO_STALL[0]	Flags the occurrence of Gyro Stall event on INT2 0: Interrupt did not occur 1: Interrupt occurred
4	INT2_STATUS_APEX_EVENT[0]	Flags the occurrence of APEX event on INT2 0: Interrupt did not occur 1: Interrupt occurred
3	INT2_STATUS_I3C_PROTOCOL_ERR[0]	Flags the occurrence of I3C^{SM} Protocol Error event on INT2 0: Interrupt did not occur 1: Interrupt occurred
2	INT2_STATUS_FIFO_FULL[0]	Flags the occurrence of FIFO full event on INT2 0: Interrupt did not occur 1: Interrupt occurred
1	INT2_STATUS_FIFO_THS[0]	Flags the occurrence of FIFO count ≥ FIFO threshold event on INT2 0: Interrupt did not occur 1: Interrupt occurred
0	INT2_STATUS_DRDY[0]	Flags the occurrence of Data Ready event on INT2 0: Interrupt did not occur 1: Interrupt occurred

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16.24 IBI_STATUS

Name: IBI_STATUS
Address: 31 (1Fh)
Serial IF: R/C
Reset value: 0x00

BIT	NAME	FUNCTION
7:6	-	Reserved
5	IBI_INT_STATUS_GYRO_STATUS[0]	Flags the occurrence of Gyro Stall event on IBI 0: Interrupt did not occur 1: Interrupt occurred
4	IBI_INT_STATUS_APEX_EVENT[0]	Flags the occurrence of APEX event on IBI 0: Interrupt did not occur 1: Interrupt occurred
3	IBI_INT_STATUS_I3C_PROTOCOL_ERR[0]	Flags the occurrence of I3C^{SM} Protocol Error event on IBI 0: Interrupt did not occur 1: Interrupt occurred
2	IBI_INT_STATUS_FIFO_FULL[0]	Flags the occurrence of FIFO full event on IBI 0: Interrupt did not occur 1: Interrupt occurred
1	IBI_INT_STATUS_FIFO_THS[0]	Flags the occurrence of FIFO count ≥ FIFO threshold event on IBI 0: Interrupt did not occur 1: Interrupt occurred
0	IBI_INT_STATUS_DRDY[0]	Flags the occurrence of Data Ready event on IBI 0: Interrupt did not occur 1: Interrupt occurred

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16.25 INT_PAD_CONFIG

Name: INT_PAD_CONFIG
Address: 37 (25h)
Serial IF: R/W
Reset value: 0x03

BIT	NAME	FUNCTION
7:2	-	Reserved
1	INT2_DRIVE[0]	Sets INT2 pin to Push-pull or Open-Drain 0: Push-pull 1: Open-drain Note: The setting can be changed when all the interrupt event sources are disabled
0	INT1_DRIVE[0]	Sets INT1 pin to Push-pull or Open-Drain 0: Push-pull 1: Open-drain Note: The setting can be changed when all the interrupt event sources are disabled

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16.26 PAD_SLEW0

Name: PAD_SLEW0
Address: 38 (26h)
Serial IF: R/W
Reset value: 0x2D

BIT	NAME	FUNCTION
7:6	-	Reserved
5:3	PADS_SPI_SLEW[2:0]	Slew rate when device is in SPI protocol. After device reset, the PADS_I2C_SLEW is used by default. The register setting takes effect 1.5µs after the LSB is received. 000: MIN: 25ns; TYP: 33ns; MAX: 115ns 001: MIN: 9ns; TYP: 13ns; MAX: 98ns 010: MIN: 6ns; TYP: 10ns; MAX: 34ns 011: MIN: 4ns; TYP: 7ns; MAX: 23ns 100: MIN: 3ns; TYP: 4ns; MAX: 10ns 101: MIN: 2ns; TYP: 3ns; MAX: 9ns 11x: MIN: 0.3ns; TYP: 0.6ns; MAX: 5ns
2:0	PADS_SLEW[2:0]	Slew rate when device is in OTP-copy operation. Whenever device is in OTP copy operation, PADS_SLEW is used to control SDO/SDIO pad. After OTP copy is done, PADS_I2C_SLEW is used by default. If the 1st operation from host is an SPI transaction, then device switches to PADS_SPI_SLEW automatically. The register setting takes effect 1.5µs after the LSB is received. 000: MIN: 25ns; TYP: 33ns; MAX: 115ns 001: MIN: 9ns; TYP: 13ns; MAX: 98ns 010: MIN: 6ns; TYP: 10ns; MAX: 34ns 011: MIN: 4ns; TYP: 7ns; MAX: 23ns 100: MIN: 3ns; TYP: 4ns; MAX: 10ns 101: MIN: 2ns; TYP: 3ns; MAX: 9ns 11x: MIN: 0.3ns; TYP: 0.6ns; MAX: 5ns

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16.27 PAD_SLEW1

Name: PAD_SLEW1
Address: 39 (27h)
Serial IF: R/W
Reset value: 0x2A

BIT	NAME	FUNCTION
7:6	-	Reserved
5:3	PADS_SDR_SLEW[2:0]	Slew rate when device is in I3C SDR protocol. After device reset, PADS_I2C_SLEW is used by default. If I3C feature is enabled, device automatically switches to PADS_SDR_SLEW after receiving 0x7E+W message (an I3C broadcast message). The register setting takes effect 1.5µs after the LSB is received. 000: MIN: 25ns; TYP: 33ns; MAX: 115ns 001: MIN: 9ns; TYP: 13ns; MAX: 98ns 010: MIN: 6ns; TYP: 10ns; MAX: 34ns 011: MIN: 4ns; TYP: 7ns; MAX: 23ns 100: MIN: 3ns; TYP: 4ns; MAX: 10ns 101: MIN: 2ns; TYP: 3ns; MAX: 9ns 11x: MIN: 0.3ns; TYP: 0.6ns; MAX: 5ns
2:0	PADS_I2C_SLEW[2:0]	Slew rate when device is in I2C protocol (when I2C Legacy slave is selected or when I3C is operating as I2C slave). After device reset, PADS_I2C_SLEW is used by default. If the 1st operation from host is an SPI transaction, then device automatically switches to PADS_SPI_SLEW. If I3C feature is enabled, device automatically switches to PADS_SDR_SLEW after receiving 0x7E+W message (an I3C broadcast message). The register setting takes effect 1.5µs after the LSB is received. 000: MIN: 7ns; TYP: 14ns; MAX: 81ns 010: MIN: 3ns; TYP: 6ns; MAX: 43ns Others: Reserved

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16.28 PAD_DELAY

Name: PAD_DELAY
Address: 40 (28h)
Serial IF: R/W
Reset value: 0x44

BIT	NAME	FUNCTION
7	GLITCH_FILTER_DIS[0]	This setting is only used when selected protocol is I2C. When using SPI or I3C, this register is ignored. 0: SCL & SDA 50ns input glitch filters are enabled 1: SCL & SDA 50ns input glitch filters are disabled
6:4	I3C_SDA_OUT_DLY[2:0]	When I3C mode is enabled, this register field is used to configure the propagation delay from the I3C IP to SDA. This provides flexibility to meet timing protocol requirements. Each increment increases the delay by 6.4 ns, up to a maximum of four increments. 000: 6.4ns 001: 12.8ns 010: 19.2ns 011: 25.6ns 1xx: 0ns (bypass)
3:0	I2C_SDA_OUT_DLY[3:0]	When I2C mode is enabled, I2C_SDA_OUT_DLY is used to configure the propagation delay from the I2C IP to SDA. This provides flexibility to meet timing protocol requirements. Each increment increases the delay by 6.4 ns, up to a maximum of eight increments. 0000: 6.4ns 0001: 12.8ns 0010: 19.2ns 0011: 25.6ns 0100: 32ns 0101: 38.4ns 0110: 44.8ns 0111: 51.2ns 1xxx: 0ns (bypass)

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16.29 EDMP_APEX_CONFIG

Name: EDMP_APEX_CONFIG
Address: 42 (2Ah)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7	LOWG_DET_EN[0]	0: Disable Low-g Detection APEX function 1: Enable Low-g Detection APEX function
6	HIGHG_DET_EN[0]	0: Disable High-g Detection APEX function 1: Enable High-g Detection APEX function
5	-	Reserved
4	TAP_DET_EN[0]	0: Disable Tap Detection APEX function 1: Enable Tap Detection APEX function
3	B2S_DET_EN[0]	0: Disable Bring to See APEX function 1: Enable Bring to See APEX function
2	FF_DET_EN[0]	0: Disable Freefall Detection APEX function 1: Enable Freefall Detection APEX function
1	WOM_DET_EN[0]	0: Disable Wake on Motion APEX function 1: Enable Wake on Motion APEX function
0	TILT_DET_EN[0]	0: Disable Tilt Detection APEX function 1: Enable Tilt Detection APEX function

16.30 EDMP_CFG_MISC

Name: EDMP_CFG_MISC
Address: 43 (2Bh)
Serial IF: R/W
Reset value: 0x03

BIT	NAME	FUNCTION
7:3	-	Reserved
2	APEX_PWR_SAVE_EN[0]	[Supports Dynamic Change] Set 1 to enable power save mode
1	FIFO_GYRO_EN[0]	[Supports Dynamic Change] FIFO Gyro enable for EDMP
0	FIFO_ACCEL_EN[0]	[Supports Dynamic Change] FIFO Accel enable for EDMP

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16.31 EDMP_APEX_STATUS0

Name: EDMP_APEX_STATUS0
Address: 46 (2Eh)
Serial IF: R/C
Reset value: 0x00

BIT	NAME	FUNCTION
7	REV_B2S_APEX_STATUS[0]	0: Reverse Bring to See APEX event did not occur 1: Reverse Bring to See APEX event occurred
6	B2S_APEX_STATUS[0]	0: Bring to See APEX event did not occur 1: Bring to See APEX event occurred
5	LOWG_APEX_STATUS[0]	0: Low-G Detection APEX event did not occur 1: Low-G Detection APEX event occurred
4	HIGHG_APEX_STATUS[0]	0: High-G Detection APEX event did not occur 1: High-G Detection APEX event occurred
3	-	Reserved
2	FF_APEX_STATUS[0]	0: Freefall Detection APEX event did not occur 1: Freefall Detection APEX event occurred
1	INACTIVE_APEX_STATUS[0]	0: Inactivity Detection APEX event did not occur 1: Inactivity Detection APEX event occurred
0	ACTIVE_APEX_STATUS[0]	0: Activity Detection APEX event did not occur 1: Activity Detection APEX event occurred

16.32 EDMP_APEX_STATUS1

Name: EDMP_APEX_STATUS1
Address: 47 (2Fh)
Serial IF: R/C
Reset value: 0x00

BIT	NAME	FUNCTION
7:2	-	Reserved
2	TAP_APEX_STATUS[0]	0: Tap Detection APEX event did not occur 1: Tap Detection APEX event occurred
1	TILT_APEX_STATUS[0]	0: Tilt Detection APEX event did not occur 1: Tilt Detection APEX event occurred
0	WOM_APEX_STATUS[0]	0: Wake on Motion APEX event did not occur 1: Wake on Motion APEX event occurred

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16.33 EDMP_MODE_STATUS

Name: EDMP_MODE_STATUS
Address: 49 (31h)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7	EDMP_BUSY[0]	EDMP busy indicator
6:4	-	Reserved
3:2	EDMP_FIFO_MODE[1:0]	Indicated FIFO mode that EDMP is in: 00: Bypass (disabled) 01: Stream mode - Frames are overwritten when the FIFO full condition is reached. 10: Stop-on-full mode - Frames are not stored in FIFO once the FIFO full condition is reached. 11: Reserved
1:0	-	Reserved

16.34 WHOAMI

Name: WHOAMI
Address: 114 (72h)
Serial IF: R
Reset value: 0x86

BIT	NAME	FUNCTION
7:0	WHOAMI[7:0]	Register to indicate to user which device is being accessed

Description:

This register is used to verify the identity of the device. The contents of WHOAMI is an 8-bit device ID. The default value of the register is 0x86. This is different from the I^2C address of the device as seen on the slave I^2C controller by the applications processor

16.35 INTF_CONFIG0

Name: INTF_CONFIG0
Address: 119 (77h)
Serial IF: R/W
Reset value: 0x02

BIT	NAME	FUNCTION
7:2	-	Reserved
1	AP_SPI_34_MODE[0]	0: AP interface uses 3-wire SPI mode 1: AP interface uses 4-wire SPI mode
0	AP_SPI_MODE[0]	SPI mode selection 0: Mode 0 and Mode 3 1: Mode 1 and Mode 2

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16.36 IREG_ADDR_15_8

Name: IREG_ADDR_15_8
Address: 124 (7Ch)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	IREG_ADDR_15_8[7:0]	Address bit[15:8] of the 16-bit indirect address for assessing indirect access registers (IREG) Can be changed on-the-fly.

16.37 IREG_ADDR_7_0

Name: IREG_ADDR_7_0
Address: 125 (7Dh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	IREG_ADDR_7_0[7:0]	Address bit[7:0] of the 16-bit indirect address for assessing indirect access registers (IREG) Can be changed on-the-fly.

16.38 IREG_DATA

Name: IREG_DATA
Address: 126 (7Eh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	IREG_DATA[7:0]	Register for indirect access registers (IREG) data read/write operations. Can be changed on-the-fly.

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16.39 REG_MISC2

Name: REG_MISC2
Address: 127 (7Fh)
Serial IF: R/W
Reset value: 0x0B

BIT	NAME	FUNCTION
7:3	-	Reserved
2	SOFT_RST[0]	0: Soft reset not enabled. 1: Triggers soft reset operation. The programmed value of 1 is self-cleared to 0 upon completion of soft reset operation. Can be changed on-the-fly.
1	IREG_AUTOINC[0]	0: IREG address auto-increment is disabled. 1: IREG address auto-increment is enabled after each IREG read or write operation. Can be changed on-the-fly.
0	IREG_DONE[0]	0: Indicates that an indirect register access operation is in progress. No new indirect register access should be triggered. 1: Indirect register access has completed. New indirect register access can be triggered. Can be changed on-the-fly.

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17 USER BANK IMEM_SRAM_APEX REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within user bank IMEM_SRAM_APEX. The registers described in this section are indirect access registers. Section 14 describes the procedure for accessing indirect access registers.

17.1 IMEM_SRAM_APEX_REG_210

Name: IMEM_SRAM_APEX_REG_210
Address: 210 (D2h)
Serial IF: R/W
Reset value: Variable

BIT	NAME	FUNCTION
7:0	FF_DURATION[7:0]	Duration of the freefall Unit: Time in sample number Format: int16_t

17.2 IMEM_SRAM_APEX_REG_211

Name: IMEM_SRAM_APEX_REG_211
Address: 211 (D3h)
Serial IF: R/W
Reset value: Variable

BIT	NAME	FUNCTION
7:0	FF_DURATION[15:8]	Duration of the freefall Unit: Time in sample number Format: int16_t

17.3 IMEM_SRAM_APEX_REG_212

Name: IMEM_SRAM_APEX_REG_212
Address: 212 (D4h)
Serial IF: R/W
Reset value: 0x32

BIT	NAME	FUNCTION
7:0	ODR_B2S[7:0]	Specify ODR of feature Bring-to-See Unit: Hertz Default value: 50 Format: int16_t

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17.4 IMEM_SRAM_APEX_REG_213

Name: IMEM_SRAM_APEX_REG_213
Address: 213 (D5h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ODR_B2S[15:8]	Specify ODR of feature Bring-to-See Unit: Hertz Default value: 50 Format: int16_t

17.5 IMEM_SRAM_APEX_REG_214

Name: IMEM_SRAM_APEX_REG_214
Address: 214 (D6h)
Serial IF: R/W
Reset value: 0x32

BIT	NAME	FUNCTION
7:0	ODR_AID[7:0]	Specify ODR of feature AID Unit: Hertz Default value: 50 Format: int16_t

17.6 IMEM_SRAM_APEX_REG_215

Name: IMEM_SRAM_APEX_REG_215
Address: 215 (D7h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ODR_AID[15:8]	Specify ODR of feature AID Unit: Hertz Default value: 50 Format: int16_t

17.7 IMEM_SRAM_APEX_REG_216

Name: IMEM_SRAM_APEX_REG_216
Address: 216 (D8h)
Serial IF: R/W
Reset value: Variable

BIT	NAME	FUNCTION
7:0	WOM_STATE[7:0]	Indicates which axes trigger the WOM event. Valid only with WOM_ANDORLOGIC set to OR logic. Bit 0: X-axis Bit 1: Y-axis Bit 2: Z-axis Bits 3 to 7: Unused Format: uint8_t

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17.8 IMEM_SRAM_APEX_REG_217

Name: IMEM_SRAM_APEX_REG_217
Address: 217 (D9h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	TILT_RESET_EN[7:0]	Set 1 to reset tilt prior to any further tilt processing on next sensor data. Format: uint8_t

17.9 IMEM_SRAM_APEX_REG_218

Name: IMEM_SRAM_APEX_REG_218
Address: 218 (DAh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ODR_TILT[7:0]	Specify ODR of feature Tilt Unit: Hertz Default value: 50 Format: int16_t

17.10 IMEM_SRAM_APEX_REG_219

Name: IMEM_SRAM_APEX_REG_219
Address: 219 (DBh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ODR_TILT[15:8]	Specify ODR of feature Tilt Unit: Hertz Default value: 50 Format: int16_t

17.11 IMEM_SRAM_APEX_REG_234

Name: IMEM_SRAM_APEX_REG_234
Address: 234 (EAh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	TAP_NUM[7:0]	Type of last reported TAP event: 0: No Tap 1: Single Tap 2: Double Tap 3: Triple Tap

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17.12 IMEM_SRAM_APEX_REG_235

Name: IMEM_SRAM_APEX_REG_235
Address: 235 (EBh)
Serial IF: R/W
Reset value: Variable

BIT	NAME	FUNCTION
7:0	TAP_AXIS[7:0]	Indicate the axis of the tap in the device frame 0: AX 1: AY 2: AZ

17.13 IMEM_SRAM_APEX_REG_236

Name: IMEM_SRAM_APEX_REG_236
Address: 236 (ECh)
Serial IF: R/W
Reset value: Variable

BIT	NAME	FUNCTION
7:0	TAP_DIR[7:0]	Indicate the direction of the tap in the device frame 0: Positive 1: Negative

17.14 IMEM_SRAM_APEX_REG_237

Name: IMEM_SRAM_APEX_REG_237
Address: 237 (EDh)
Serial IF: R/W
Reset value: Variable

BIT	NAME	FUNCTION
7:0	DOUBLE_TAP_TIMING[7:0]	The sample count of second pulse in detection window

17.15 IMEM_SRAM_APEX_REG_238

Name: IMEM_SRAM_APEX_REG_238
Address: 238 (EEh)
Serial IF: R/W
Reset value: Variable

BIT	NAME	FUNCTION
7:0	TRIPLE_TAP_TIMING[7:0]	The sample count of third pulse in detection window

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17.16 IMEM_SRAM_APEX_REG_260

Name: IMEM_SRAM_APEX_REG_260
Address: 260 (104h)
Serial IF: R/W
Reset value: 0x33

BIT	NAME	FUNCTION
7:0	WOM_THRESHOLD_X[7:0]	WOM threshold setting for X-axis Unit: In LSB, with 1 LBS = 1g / 2^12 Default value: 819 corresponding to 200mg Recommended range value: [0 - 4096] Format: uint16_t

17.17 IMEM_SRAM_APEX_REG_261

Name: IMEM_SRAM_APEX_REG_261
Address: 261 (105h)
Serial IF: R/W
Reset value: 0x03

BIT	NAME	FUNCTION
7:0	WOM_THRESHOLD_X[15:8]	WOM threshold setting for X-axis Unit: In LSB, with 1 LBS = 1g / 2^12 Default value: 819 corresponding to 200mg Recommended range value: [0 - 4096] Format: uint16_t

17.18 IMEM_SRAM_APEX_REG_262

Name: IMEM_SRAM_APEX_REG_262
Address: 262 (106h)
Serial IF: R/W
Reset value: 0x33

BIT	NAME	FUNCTION
7:0	WOM_THRESHOLD_Y[7:0]	WOM threshold setting for Y-axis Unit: In LSB, with 1 LBS = 1g / 2^12 Default value: 819 corresponding to 200mg Recommended range value: [0 - 4096] Format: uint16_t

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17.19 IMEM_SRAM_APEX_REG_263

Name: IMEM_SRAM_APEX_REG_263
Address: 263 (107h)
Serial IF: R/W
Reset value: 0x03

BIT	NAME	FUNCTION
7:0	WOM_THRESHOLD_Y[15:8]	WOM threshold setting for Y-axis Unit: In LSB, with 1 LBS = 1g / 2^12 Default value: 819 corresponding to 200mg Recommended range value: [0 - 4096] Format: uint16_t

17.20 IMEM_SRAM_APEX_REG_264

Name: IMEM_SRAM_APEX_REG_264
Address: 264 (108h)
Serial IF: R/W
Reset value: 0x33

BIT	NAME	FUNCTION
7:0	WOM_THRESHOLD_Z[7:0]	WOM threshold setting for Z-axis Unit: In LSB, with 1 LBS = 1g / 2^12 Default value: 819 corresponding to 200mg Recommended range value: [0 - 4096] Format: uint16_t

17.21 IMEM_SRAM_APEX_REG_265

Name: IMEM_SRAM_APEX_REG_265
Address: 265 (109h)
Serial IF: R/W
Reset value: 0x03

BIT	NAME	FUNCTION
7:0	WOM_THRESHOLD_Z[15:8]	WOM threshold setting for Z-axis Unit: In LSB, with 1 LBS = 1g / 2^12 Default value: 819 corresponding to 200mg Recommended range value: [0 - 4096] Format: uint16_t

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17.22 IMEM_SRAM_APEX_REG_266

Name: IMEM_SRAM_APEX_REG_266
Address: 266 (10Ah)
Serial IF: R/W
Reset value: 0x05

BIT	NAME	FUNCTION
7:0	WOM_WAIT_TIME[7:0]	WOM wait time, internal WOM event count required before interrupt Unit: In sample number - ODR dependent Default value: 5 Recommended range value: [1 - 4000] Format: uint16_t

17.23 IMEM_SRAM_APEX_REG_267

Name: IMEM_SRAM_APEX_REG_267
Address: 267 (10Bh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	WOM_WAIT_TIME[15:8]	WOM wait time, internal WOM event count required before interrupt Unit: In sample number - ODR dependent Default value: 1 Recommended range value: [1 - 4000] Format: uint16_t

17.24 IMEM_SRAM_APEX_REG_268

Name: IMEM_SRAM_APEX_REG_268
Address: 268 (10Ch)
Serial IF: R/W
Reset value: 0x01

BIT	NAME	FUNCTION
7:0	WOM_ANDORLOGIC[7:0]	WOM interrupt mode, select if the threshold needs to be met on all axis or any one axis to allow triggering an interrupt Unit: In Enum Default value: 1 corresponding to (OR) Acceptable value: 0 (AND) or 1 (OR) Format: uint8_t

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17.25 IMEM_SRAM_APEX_REG_280

Name: IMEM_SRAM_APEX_REG_280
Address: 280 (118h)
Serial IF: R/W
Reset value: 0x96

BIT	NAME	FUNCTION
7:0	AID_UPDATEWIN[7:0]	Time window to decide Activity or Inactivity Activity or Inactivity will trigger after this time window Unit: Number of samples Default value: 150, corresponding to 3 seconds at 50Hz Format: uint32_t

17.26 IMEM_SRAM_APEX_REG_281

Name: IMEM_SRAM_APEX_REG_281
Address: 281 (119h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	AID_UPDATEWIN[15:8]	Time window to decide Activity or Inactivity Activity or Inactivity will trigger after this time window Unit: Number of samples Default value: 150, corresponding to 3 seconds at 50Hz Format: uint32_t

17.27 IMEM_SRAM_APEX_REG_282

Name: IMEM_SRAM_APEX_REG_282
Address: 282 (11Ah)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	AID_UPDATEWIN[23:16]	Time window to decide Activity or Inactivity Activity or Inactivity will trigger after this time window Unit: Number of samples Default value: 150, corresponding to 3 seconds at 50Hz Format: uint32_t

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17.28 IMEM_SRAM_APEX_REG_283

Name: IMEM_SRAM_APEX_REG_283
Address: 283 (11Bh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	AID_UPDATEWIN[31:24]	Time window to decide Activity or Inactivity Activity or Inactivity will trigger after this time window Unit: Number of samples Default value: 150, corresponding to 3 seconds at 50Hz Format: uint32_t

17.29 IMEM_SRAM_APEX_REG_284

Name: IMEM_SRAM_APEX_REG_284
Address: 284 (11Ch)
Serial IF: R/W
Reset value: 0x03

BIT	NAME	FUNCTION
7:0	AID_ENABLE_OUTPUT[7:0]	Bitwise enable output: Bit 0 for enable activity detection, bit 1 for inactivity, bit 2 for alert Unit: N/A Default value: 3 Acceptable value: 0 (AND) or 1 (OR) Format: uint8_t

17.30 IMEM_SRAM_APEX_REG_285

Name: IMEM_SRAM_APEX_REG_285
Address: 285 (11Dh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	AID_DISABLE_MULTIPLE_OUTPUT[7:0]	Option to disable output after each internal decision of algorithm. Output will trigger after each time window corresponding to UPDATEWIN Unit: N/A Default value: 0, corresponding to all decisions are triggered Acceptable value: 0 or 1 Format: uint8_t

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17.31 IMEM_SRAM_APEX_REG_316

Name: IMEM_SRAM_APEX_REG_316
Address: 316 (13Ch)
Serial IF: R/W
Reset value: 0x39

BIT	NAME	FUNCTION
7:0	FF_MIN_DURATION[7:0]	Minimum duration between a LowG and HighG event to trigger freefall Unit: In sample number, ODR dependent Default value: 57, corresponding to 142ms at 400Hz Recommended range value: [4 - 420] Format: uint32_t

17.32 IMEM_SRAM_APEX_REG_317

Name: IMEM_SRAM_APEX_REG_317
Address: 317 (13Dh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	FF_MIN_DURATION[15:8]	Minimum duration between a LowG and HighG event to trigger freefall Unit: In sample number, ODR dependent Default value: 57, corresponding to 142ms at 400Hz Recommended range value: [4 - 420] Format: uint32_t

17.33 IMEM_SRAM_APEX_REG_318

Name: IMEM_SRAM_APEX_REG_318
Address: 318 (13Eh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	FF_MIN_DURATION[23:16]	Minimum duration between a LowG and HighG event to trigger freefall Unit: In sample number, ODR dependent Default value: 57, corresponding to 142ms at 400Hz Recommended range value: [4 - 420] Format: uint32_t

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17.34 IMEM_SRAM_APEX_REG_319

Name: IMEM_SRAM_APEX_REG_319
Address: 319 (13Fh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	FF_MIN_DURATION[31:24]	Minimum duration between a LowG and HighG event to trigger freefall Unit: In sample number, ODR dependent Default value: 57, corresponding to 142ms at 400Hz Recommended range value: [4 - 420] Format: uint32_t

17.35 IMEM_SRAM_APEX_REG_320

Name: IMEM_SRAM_APEX_REG_320
Address: 320 (140h)
Serial IF: R/W
Reset value: 0x1D

BIT	NAME	FUNCTION
7:0	FF_MAX_DURATION[7:0]	Maximum duration after a LowG event to wait HighG event before reset freefall algorithm Unit: In sample number, ODR dependent Default value: 285, corresponding to 712ms at 400Hz Recommended range value [12 - 1040] Format: uint32_t

17.36 IMEM_SRAM_APEX_REG_321

Name: IMEM_SRAM_APEX_REG_321
Address: 321 (141h)
Serial IF: R/W
Reset value: 0x01

BIT	NAME	FUNCTION
7:0	FF_MAX_DURATION[15:8]	Maximum duration after a LowG event to wait HighG event before reset freefall algorithm Unit: In sample number, ODR dependent Default value: 295, corresponding to 712ms at 400Hz Recommended range value [12 - 1040] Format: uint32_t

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17.37 IMEM_SRAM_APEX_REG_322

Name: IMEM_SRAM_APEX_REG_322
Address: 322 (142h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	FF_MAX_DURATION[23:16]	Maximum duration after a LowG event to wait HighG event before reset freefall algorithm Unit: In sample number, ODR dependent Default value: 295, corresponding to 712ms at 400Hz Recommended range value [12 - 1040] Format: uint32_t

17.38 IMEM_SRAM_APEX_REG_323

Name: IMEM_SRAM_APEX_REG_323
Address: 323 (143h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	FF_MAX_DURATION[31:24]	Maximum duration after a LowG event to wait HighG event before reset freefall algorithm Unit: In sample number, ODR dependent Default value: 295, corresponding to 712ms at 400Hz Recommended range value [12 - 1040] Format: uint32_t

17.39 IMEM_SRAM_APEX_REG_324

Name: IMEM_SRAM_APEX_REG_324
Address: 324 (144h)
Serial IF: R/W
Reset value: 0x20

BIT	NAME	FUNCTION
7:0	FF_DEBOUNCE_DURATION [7:0]	Wait duration after freefall event detected (to avoid false freefall event) Algorithm is in "pause" during this time Unit: In sample number, ODR dependent Default value: 800, corresponding to 2s at 400Hz Recommended range value: [75 - 3000] Format: uint32_t

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17.40 IMEM_SRAM_APEX_REG_325

Name: IMEM_SRAM_APEX_REG_325
Address: 325 (145h)
Serial IF: R/W
Reset value: 0x03

BIT	NAME	FUNCTION
7:0	FF_DEBOUNCE_DURATION [15:8]	Wait duration after freefall event detected (to avoid false freefall event) Algorithm is in "pause" during this time Unit: In sample number, ODR dependent Default value: 800, corresponding to 2s at 400Hz Recommended range value: [75 - 3000] Format: uint32_t

17.41 IMEM_SRAM_APEX_REG_326

Name: IMEM_SRAM_APEX_REG_326
Address: 326 (146h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	FF_DEBOUNCE_DURATION [23:16]	Wait duration after freefall event detected (to avoid false freefall event) Algorithm is in "pause" during this time Unit: In sample number, ODR dependent Default value: 800, corresponding to 2s at 400Hz Recommended range value: [75 - 3000] Format: uint32_t

17.42 IMEM_SRAM_APEX_REG_327

Name: IMEM_SRAM_APEX_REG_327
Address: 327 (147h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	FF_DEBOUNCE_DURATION [31:24]	Wait duration after freefall event detected (to avoid false freefall event) Algorithm is in "pause" during this time Unit: In sample number, ODR dependent Default value: 800, corresponding to 2s at 400Hz Recommended range value: [75 - 3000] Format: uint32_t

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17.43 IMEM_SRAM_APEX_REG_334

Name: IMEM_SRAM_APEX_REG_334
Address: 334 (14Eh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	LOWG_PEAK_TH[7:0]	Sum of absolute accelerometer axis falls LOWG_PEAK_TH will potentially trigger the start of LowG state Unit: In LSB, with 1 LSB = 1g / 2^12 Default value: 2048 (corresponding to 0.5g) Recommended range value: [128 - 4096] Format: int16_t

17.44 IMEM_SRAM_APEX_REG_335

Name: IMEM_SRAM_APEX_REG_335
Address: 335 (14Fh)
Serial IF: R/W
Reset value: 0x08

BIT	NAME	FUNCTION
7:0	LOWG_PEAK_TH[15:8]	Sum of absolute accelerometer axis falls LOWG_PEAK_TH will potentially trigger the start of LowG state Unit: In LSB, with 1 LSB = 1g / 2^12 Default value: 2048 (corresponding to 0.5g) Recommended range value: [128 - 4096] Format: int16_t

17.45 IMEM_SRAM_APEX_REG_336

Name: IMEM_SRAM_APEX_REG_336
Address: 336 (150h)
Serial IF: R/W
Reset value: 0x80

BIT	NAME	FUNCTION
7:0	LOWG_PEAK_TH_HYST[7:0]	Hysteresis added to the threshold to confirm the triggering of the LowG state Unit: In LSB, with 1 LSB = 1g / 2^12 Default value: 128 (corresponding to 31.2mg) Recommended range value: [128 - 1024] Format: int16_t

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17.46 IMEM_SRAM_APEX_REG_337

Name: IMEM_SRAM_APEX_REG_337
Address: 337 (151h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	LOWG_PEAK_TH_HYST[15:8]	Hysteresis added to the threshold to confirm the triggering of the LowG state Unit: In LSB, with 1 LSB = 1g / 2^12 Default value: 128 (corresponding to 31.2mg) Recommended range value: [128 - 1024] Format: int16_t

17.47 IMEM_SRAM_APEX_REG_338

Name: IMEM_SRAM_APEX_REG_338
Address: 338 (152h)
Serial IF: R/W
Reset value: 0x0D

BIT	NAME	FUNCTION
7:0	LOWG_TIME_TH[7:0]	The number of samples device should stay below (LOWG_PEAK_TH + LOWG_PEAK_TH_HYST) before LowG state is triggered Unit: In sample number - ODR dependent Default value: 13 (corresponding to 32ms at 400Hz) Recommended range value: [1 - 300] Format: int16_t

17.48 IMEM_SRAM_APEX_REG_339

Name: IMEM_SRAM_APEX_REG_339
Address: 339 (153h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	LOWG_TIME_TH[15:8]	The number of samples device should stay below (LOWG_PEAK_TH + LOWG_PEAK_TH_HYST) before LowG state is triggered Unit: In sample number - ODR dependent Default value: 13 (corresponding to 32ms at 400Hz) Recommended range value: [1 - 300] Format: int16_t

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17.49 IMEM_SRAM_APEX_REG_346

Name: IMEM_SRAM_APEX_REG_346
Address: 346 (15Ah)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	HIGHG_PEAK_TH[7:0]	Any of the absolute accelerometer axis surpasses HIGH_PEAK_THRES will potentially trigger the start of HighG state Unit: In LSB, with 1 LSB = 1g / 2^12 Default value: 29696 (corresponding to 7.25g) Recommended range value: [1024-32768]

17.50 IMEM_SRAM_APEX_REG_347

Name: IMEM_SRAM_APEX_REG_347
Address: 347 (15Bh)
Serial IF: R/W
Reset value: 0x74

BIT	NAME	FUNCTION
7:0	HIGHG_PEAK_TH[15:8]	Any of the absolute accelerometer axis surpasses HIGH_PEAK_THRES will potentially trigger the start of HighG state Unit: In LSB, with 1 LSB = 1g / 2^12 Default value: 29696 (corresponding to 7.25g) Recommended range value: [1024-32768]

17.51 IMEM_SRAM_APEX_REG_348

Name: IMEM_SRAM_APEX_REG_348
Address: 348 (15Ch)
Serial IF: R/W
Reset value: 0x80

BIT	NAME	FUNCTION
7:0	HIGHG_PEAK_TH_HYST[7:0]	A hysteresis HIGH_PEAK_THRES_HYST is subtracted from the threshold (HIGH_PEAK_THRES) after the initial threshold is met Unit: In LSB, with 1 LSB = 1g / 2^12 Default value: 640 (corresponding to 0.1563g) Recommended range value: [128 - 1024] Format: int16_t

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17.52 IMEM_SRAM_APEX_REG_349

Name: IMEM_SRAM_APEX_REG_349
Address: 349 (15Dh)
Serial IF: R/W
Reset value: 0x02

BIT	NAME	FUNCTION
7:0	HIGHG_PEAK_TH_HYST[15:8]	A hysteresis HIGH_PEAK_THRES_HYST is subtracted from the threshold (HIGH_PEAK_THRES) after the initial threshold is met Unit: In LSB, with 1 LSB = 1g / 2^12 Default value: 640 (corresponding to 0.1563g) Recommended range value: [128 - 1024] Format: int16_t

17.53 IMEM_SRAM_APEX_REG_350

Name: IMEM_SRAM_APEX_REG_350
Address: 350 (15Eh)
Serial IF: R/W
Reset value: 0x01

BIT	NAME	FUNCTION
7:0	HIGHG_TIME_TH[7:0]	The number of samples the device should stay above (HIGHG_PEAK_TH - HIGHG_PEAK_TH_HYST) before HighG state is triggered Unit: In sample number - ODR dependent Default value: 1 (corresponding to 2.5ms at 400Hz) Recommended range value: [1 - 300] Format: int16_t

17.54 IMEM_SRAM_APEX_REG_351

Name: IMEM_SRAM_APEX_REG_351
Address: 351 (15Fh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	HIGHG_TIME_TH[15:8]	The number of samples the device should stay above (HIGHG_PEAK_TH - HIGHG_PEAK_TH_HYST) before HighG state is triggered Unit: In sample number - ODR dependent Default value: 1 (corresponding to 2.5ms at 400Hz) Recommended range value: [1 - 300] Format: int16_t

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17.55 IMEM_SRAM_APEX_REG_364

Name: IMEM_SRAM_APEX_REG_364
Address: 364 (16Ch)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_MOUNTING_MATRIX[7:0]	Used for b2smounting matrix. 3 bits are used [b2 b1 b0]: when b2 = 1 swap X and Y, when b1 = 1 flip X sign, when b0 = 1 flip Y sign, Format: uint8_t

17.56 IMEM_SRAM_APEX_REG_368

Name: IMEM_SRAM_APEX_REG_368
Address: 368 (170h)
Serial IF: R/W
Reset value: 0xBC

BIT	NAME	FUNCTION
7:0	B2S_DEV_NORM_MAX[7:0]	Hysteresis added or removed to norm estimate and Y axis constrains value for RevB2S Unit: In LSB, with 1 LBS = 1g / 2^12 Default value: 700 (corresponding to 0.1709g) Recommended range value: [1 - 2048] Format: int32_t

17.57 IMEM_SRAM_APEX_REG_369

Name: IMEM_SRAM_APEX_REG_369
Address: 369 (171h)
Serial IF: R/W
Reset value: 0x02

BIT	NAME	FUNCTION
7:0	B2S_DEV_NORM_MAX[15:8]	Hysteresis added or removed to norm estimate and Y axis constrains value for RevB2S Unit: In LSB, with 1 LBS = 1g / 2^12 Default value: 700 (corresponding to 0.1709g) Recommended range value: [1 - 2048] Format: int32_t

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17.58 IMEM_SRAM_APEX_REG_370

Name: IMEM_SRAM_APEX_REG_370
Address: 370 (172h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_DEV_NORM_MAX[23:16]	Hysteresis added or removed to norm estimate and Y axis constrains value for RevB2S Unit: In LSB, with 1 LBS = 1g / 2^12 Default value: 700 (corresponding to 0.1709g) Recommended range value: [1 - 2048] Format: int32_t

17.59 IMEM_SRAM_APEX_REG_371

Name: IMEM_SRAM_APEX_REG_371
Address: 371 (173h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_DEV_NORM_MAX[31:24]	Hysteresis added or removed to norm estimate and Y axis constrains value for RevB2S Unit: In LSB, with 1 LBS = 1g / 2^12 Default value: 700 (corresponding to 0.1709g) Recommended range value: [1 - 2048] Format: int32_t

17.60 IMEM_SRAM_APEX_REG_372

Name: IMEM_SRAM_APEX_REG_372
Address: 372 (174h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_SIN_LIMIT[7:0]	Defines the maximum allowed X-axis value in the B2S position. Detections are rejected when |X_axis| exceeds this threshold Unit: In LSB, with 1 LBS = 1g / 2^12 Default value: 2048 (corresponding to 30°) Recommended range value: [300 - 3000] Format: int32_t

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17.61 IMEM_SRAM_APEX_REG_373

Name: IMEM_SRAM_APEX_REG_373
Address: 373 (175h)
Serial IF: R/W
Reset value: 0x08

BIT	NAME	FUNCTION
7:0	B2S_SIN_LIMIT[15:8]	Defines the maximum allowed X-axis value in the B2S position. Detections are rejected when |X_axis| exceeds this threshold Unit: In LSB, with 1 LBS = 1g / 2^12 Default value: 2048 (corresponding to 30°) Recommended range value: [300 - 3000] Format: int32_t

17.62 IMEM_SRAM_APEX_REG_374

Name: IMEM_SRAM_APEX_REG_374
Address: 374 (176h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_SIN_LIMIT[23:16]	Defines the maximum allowed X-axis value in the B2S position. Detections are rejected when |X_axis| exceeds this threshold Unit: In LSB, with 1 LBS = 1g / 2^12 Default value: 2048 (corresponding to 30°) Recommended range value: [300 - 3000] Format: int32_t

17.63 IMEM_SRAM_REG_375

Name: IMEM_SRAM_APEX_REG_375
Address: 375 (177h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_SIN_LIMIT[31:24]	Defines the maximum allowed X-axis value in the B2S position. Detections are rejected when |X_axis| exceeds this threshold Unit: In LSB, with 1 LBS = 1g / 2^12 Default value: 2048 (corresponding to 30°) Recommended range value: [300 - 3000] Format: int32_t

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17.64 IMEM_SRAM_APEX_REG_376

Name: IMEM_SRAM_APEX_REG_376
Address: 376 (178h)
Serial IF: R/W
Reset value: 0x14

BIT	NAME	FUNCTION
7:0	B2S_FAST_MOTION_AGE_LIMIT[7:0]	Time limit between last "Fast motion" and b2s position Unit: In sample number - ODR dependent Default value: 20 (corresponding to 400ms at 50Hz) Format: int32_t

17.65 IMEM_SRAM_APEX_REG_377

Name: IMEM_SRAM_APEX_REG_377
Address: 377 (179h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_FAST_MOTION_AGE_LIMIT[15:8]	Time limit between last "Fast motion" and b2s position Unit: In sample number - ODR dependent Default value: 20 (corresponding to 400ms at 50Hz) Format: int32_t

17.66 IMEM_SRAM_APEX_REG_378

Name: IMEM_SRAM_APEX_REG_378
Address: 378 (17Ah)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_FAST_MOTION_AGE_LIMIT[23:16]	Time limit between last "Fast motion" and b2s position Unit: In sample number - ODR dependent Default value: 20 (corresponding to 400ms at 50Hz) Format: int32_t

17.67 IMEM_SRAM_APEX_REG_379

Name: IMEM_SRAM_APEX_REG_379
Address: 379 (17Bh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_FAST_MOTION_AGE_LIMIT[31:24]	Time limit between last "Fast motion" and b2s position Unit: In sample number - ODR dependent Default value: 20 (corresponding to 400ms at 50Hz) Format: int32_t

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17.68 IMEM_SRAM_APEX_REG_380

Name: IMEM_SRAM_APEX_REG_380
Address: 380 (17Ch)
Serial IF: R/W
Reset value: 0xC8

BIT	NAME	FUNCTION
7:0	B2S_FAST_LIMIT[7:0]	Threshold of minimal motion to be detected as "Fast motion" Unit: No unit, filtered data Default value: 200 Format: int32_t

17.69 IMEM_SRAM_APEX_REG_381

Name: IMEM_SRAM_APEX_REG_381
Address: 381 (17Dh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_FAST_LIMIT[15:8]	Threshold of minimal motion to be detected as "Fast motion" Unit: No unit, filtered data Default value: 200 Format: int32_t

17.70 IMEM_SRAM_APEX_REG_382

Name: IMEM_SRAM_APEX_REG_382
Address: 382 (17Eh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_FAST_LIMIT[23:16]	Threshold of minimal motion to be detected as "Fast motion" Unit: No unit, filtered data Default value: 200 Format: int32_t

17.71 IMEM_SRAM_APEX_REG_383

Name: IMEM_SRAM_APEX_REG_383
Address: 383 (17Fh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_FAST_LIMIT[31:24]	Threshold of minimal motion to be detected as "Fast motion" Unit: No unit, filtered data Default value: 200 Format: int32_t

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17.72 IMEM_SRAM_APEX_REG_384

Name: IMEM_SRAM_APEX_REG_384
Address: 384 (180h)
Serial IF: R/W
Reset value: 0x04

BIT	NAME	FUNCTION
7:0	B2S_FAST_MOTION_TIME_LIMIT[7:0]	Minimum time where the criterion is above the threshold to be classified as "Fast motion" Unit: In sample number - ODR dependent Default value: 4 (corresponding to 80ms at 50Hz) Format: int32_t

17.73 IMEM_SRAM_APEX_REG_385

Name: IMEM_SRAM_APEX_REG_385
Address: 385 (181h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_FAST_MOTION_TIME_LIMIT[15:8]	Minimum time where the criterion is above the threshold to be classified as "Fast motion" Unit: In sample number - ODR dependent Default value: 4 (corresponding to 80ms at 50Hz) Format: int32_t

17.74 IMEM_SRAM_APEX_REG_386

Name: IMEM_SRAM_APEX_REG_386
Address: 386 (182h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_FAST_MOTION_TIME_LIMIT[23:16]	Minimum time where the criterion is above the threshold to be classified as "Fast motion" Unit: In sample number - ODR dependent Default value: 4 (corresponding to 80ms at 50Hz) Format: int32_t

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17.75 IMEM_SRAM_APEX_REG_387

Name: IMEM_SRAM_APEX_REG_387
Address: 387 (183h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_FAST_MOTION_TIME_LIMIT[31:24]	Minimum time where the criterion is above the threshold to be classified as "Fast motion" Unit: In sample number - ODR dependent Default value: 4 (corresponding to 80ms at 50Hz) Format: int32_t

17.76 IMEM_SRAM_APEX_REG_388

Name: IMEM_SRAM_APEX_REG_388
Address: 388 (184h)
Serial IF: R/W
Reset value: 0x32

BIT	NAME	FUNCTION
7:0	B2S_AGE_LIMIT[7:0]	Minimum time between 2 events b2s Unit: In sample number - ODR dependent Default value: 50 (corresponding to 1s at 50Hz) Format: int32_t

17.77 IMEM_SRAM_APEX_REG_389

Name: IMEM_SRAM_APEX_REG_389
Address: 389 (185h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_AGE_LIMIT[15:8]	Minimum time between 2 events b2s Unit: In sample number - ODR dependent Default value: 50 (corresponding to 1s at 50Hz) Format: int32_t

17.78 IMEM_SRAM_APEX_REG_390

Name: IMEM_SRAM_APEX_REG_390
Address: 390 (186h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_AGE_LIMIT[23:16]	Minimum time between 2 events b2s Unit: In sample number - ODR dependent Default value: 50 (corresponding to 1s at 50Hz) Format: int32_t

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17.79 IMEM_SRAM_APEX_REG_391

Name: IMEM_SRAM_APEX_REG_391
Address: 391 (187h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_AGE_LIMIT[31:24]	Minimum time between 2 events b2s Unit: In sample number - ODR dependent Default value: 50 (corresponding to 1s at 50Hz) Format: int32_t

17.80 IMEM_SRAM_APEX_REG_392

Name: IMEM_SRAM_APEX_REG_392
Address: 392 (188h)
Serial IF: R/W
Reset value: 0x78

BIT	NAME	FUNCTION
7:0	B2S_STATIC_LIMIT[7:0]	Threshold to determine static phase required after the gesture B2S to validate it Unit: No unit, filtered data Default value: 1400 Format: int32_t

17.81 IMEM_SRAM_APEX_REG_393

Name: IMEM_SRAM_APEX_REG_393
Address: 393 (189h)
Serial IF: R/W
Reset value: 0x05

BIT	NAME	FUNCTION
7:0	B2S_STATIC_LIMIT[15:8]	Threshold to determine static phase required after the gesture B2S to validate it Unit: No unit, filtered data Default value: 1400 Format: int32_t

17.82 IMEM_SRAM_APEX_REG_394

Name: IMEM_SRAM_APEX_REG_394
Address: 394 (18Ah)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_STATIC_LIMIT[23:16]	Threshold to determine static phase required after the gesture B2S to validate it Unit: No unit, filtered data Default value: 1400 Format: int32_t

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17.83 IMEM_SRAM_APEX_REG_395

Name: IMEM_SRAM_APEX_REG_395
Address: 395 (18Bh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_STATIC_LIMIT[31:24]	Threshold to determine static phase required after the gesture B2S to validate it Unit: No unit, filtered data Default value: 1400 Format: int32_t

17.84 IMEM_SRAM_APEX_REG_396

Name: IMEM_SRAM_APEX_REG_396
Address: 396 (18Ch)
Serial IF: R/W
Reset value: 0x19

BIT	NAME	FUNCTION
7:0	B2S_THR_COS_ANGLE[7:0]	RevB2S threshold, condition satisfied when moving away from bring2see orientation position by more than threshold angle corresponding to the cosine value Unit: Cosine value of angle in q30 Default value: 1057429273 corresponding to 10° Format: int32_t

17.85 IMEM_SRAM_APEX_REG_397

Name: IMEM_SRAM_APEX_REG_397
Address: 397 (18Dh)
Serial IF: R/W
Reset value: 0x17

BIT	NAME	FUNCTION
7:0	B2S_THR_COS_ANGLE[15:8]	RevB2S threshold, condition satisfied when moving away from bring2see orientation position by more than threshold angle corresponding to the cosine value Unit: Cosine value of angle in q30 Default value: 1057429273 corresponding to 10° Format: int32_t

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17.86 IMEM_SRAM_APEX_REG_398

Name: IMEM_SRAM_APEX_REG_398
Address: 398 (18Eh)
Serial IF: R/W
Reset value: 0x07

BIT	NAME	FUNCTION
7:0	B2S_THR_COS_ANGLE[23:16]	RevB2S threshold, condition satisfied when moving away from bring2see orientation position by more than threshold angle corresponding to the cosine value Unit: Cosine value of angle in q30 Default value: 1057429273 corresponding to 10° Format: int32_t

17.87 IMEM_SRAM_APEX_REG_399

Name: IMEM_SRAM_APEX_REG_399
Address: 399 (18Fh)
Serial IF: R/W
Reset value: 0x3F

BIT	NAME	FUNCTION
7:0	B2S_THR_COS_ANGLE[31:24]	RevB2S threshold, condition satisfied when moving away from bring2see orientation position by more than threshold angle corresponding to the cosine value Unit: Cosine value of angle in q30 Default value: 1057429273 corresponding to 10° Format: int32_t

17.88 IMEM_SRAM_APEX_REG_400

Name: IMEM_SRAM_APEX_REG_400
Address: 400 (190h)
Serial IF: R/W
Reset value: 0x19

BIT	NAME	FUNCTION
7:0	B2S_REVB2S_LATENCY_THR[7:0]	Condition of RevB2S should be maintained at least during this period Unit: In sample number - ODR dependent Default value: 25 (corresponding to 0.5s at 50Hz) Format: int32_t

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17.89 IMEM_SRAM_APEX_REG_401

Name: IMEM_SRAM_APEX_REG_401
Address: 401 (191h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_REVB2S_LATENCY_THR[15:8]	Condition of RevB2S should be maintained at least during this period Unit: In sample number - ODR dependent Default value: 25 (corresponding to 0.5s at 50Hz) Format: int32_t

17.90 IMEM_SRAM_APEX_REG_402

Name: IMEM_SRAM_APEX_REG_402
Address: 402 (192h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_REVB2S_LATENCY_THR[23:16]	Condition of RevB2S should be maintained at least during this period Unit: In sample number - ODR dependent Default value: 25 (corresponding to 0.5s at 50Hz) Format: int32_t

17.91 IMEM_SRAM_APEX_REG_403

Name: IMEM_SRAM_APEX_REG_403
Address: 403 (193h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_REVB2S_LATENCY_THR[31:24]	Condition of RevB2S should be maintained at least during this period Unit: In sample number - ODR dependent Default value: 25 (corresponding to 0.5s at 50Hz) Format: int32_t

17.92 IMEM_SRAM_APEX_REG_404

Name: IMEM_SRAM_APEX_REG_404
Address: 404 (194h)
Serial IF: R/W
Reset value: 0x60

BIT	NAME	FUNCTION
7:0	B2S_REVB2S_X_LIMIT[7:0]	Defines the minimum allowed X-axis value in the rev-B2S position to confirm the user-arm is pointing down. Detections are rejected when |X_axis| is below this threshold. Unit: In LSB, with 1 LBS = 1g / 2^12 Default value: 3680 (corresponding to 0.8984g) Format: int32_t

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17.93 IMEM_SRAM_APEX_REG_405

Name: IMEM_SRAM_APEX_REG_405
Address: 405 (195h)
Serial IF: R/W
Reset value: 0x0E

BIT	NAME	FUNCTION
7:0	B2S_REVB2S_X_LIMIT[15:8]	Defines the minimum allowed X-axis value in the rev-B2S position to confirm the user-arm is pointing down. Detections are rejected when |X_axis| is below this threshold. Unit: In LSB, with 1 LBS = 1g / 2^12 Default value: 3680 (corresponding to 0.8984g) Format: int32_t

17.94 IMEM_SRAM_APEX_REG_406

Name: IMEM_SRAM_APEX_REG_406
Address: 406 (196h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_REVB2S_X_LIMIT[23:16]	Defines the minimum allowed X-axis value in the rev-B2S position to confirm the user-arm is pointing down. Detections are rejected when |X_axis| is below this threshold. Unit: In LSB, with 1 LBS = 1g / 2^12 Default value: 3680 (corresponding to 0.8984g) Format: int32_t

17.95 IMEM_SRAM_APEX_REG_407

Name: IMEM_SRAM_APEX_REG_407
Address: 407 (197h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_REVB2S_X_LIMIT[31:24]	Defines the minimum allowed X-axis value in the rev-B2S position to confirm the user-arm is pointing down. Detections are rejected when |X_axis| is below this threshold. Unit: In LSB, with 1 LBS = 1g / 2^12 Default value: 3680 (corresponding to 0.8984g) Format: int32_t

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17.96 IMEM_SRAM_APEX_REG_408

Name: IMEM_SRAM_APEX_REG_408
Address: 408 (198h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_SIN_FLAT_ANGLE[7:0]	Condition to detect the flat position and reject B2S interrupt at return to rest position Unit in LSB, with 1 LSB = 1g / 2^12 Default value 2048 (corresponding to 30) Format: int32_t

17.97 IMEM_SRAM_APEX_REG_409

Name: IMEM_SRAM_APEX_REG_409
Address: 409 (199h)
Serial IF: R/W
Reset value: 0x08

BIT	NAME	FUNCTION
7:0	B2S_SIN_FLAT_ANGLE[15:8]	Condition to detect the flat position and reject B2S interrupt at return to rest position Unit in LSB, with 1 LSB = 1g / 2^12 Default value 2048 (corresponding to 30) Format: int32_t

17.98 IMEM_SRAM_APEX_410

Name: IMEM_SRAM_APEX_REG_410
Address: 410 (19Ah)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_SIN_FLAT_ANGLE[23:16]	Condition to detect the flat position and reject B2S interrupt at return to rest position Unit in LSB, with 1 LSB = 1g / 2^12 Default value 2048 (corresponding to 30) Format: int32_t

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17.99 IMEM_SRAM_APEX_REG_411

Name: IMEM_SRAM_APEX_REG_411
Address: 411 (19Bh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_SIN_FLAT_ANGLE[31:24]	Condition to detect the flat position and reject B2S interrupt at return to rest position Unit in LSB, with 1 LSB = 1g / 2^12 Default value 2048 (corresponding to 30) Format: int32_t

17.100 IMEM_SRAM_APEX_REG_412

Name: IMEM_SRAM_APEX_REG_412
Address: 412 (19Ch)
Serial IF: R/W
Reset value: 0x5E

BIT	NAME	FUNCTION
7:0	B2S_TIMER_FLAT_REJECT[7:0]	A timer to disable flat rejection when age of the last no-flat B2S detection is over the timer Unit in sample number - ODR dependent Default value 350 (corresponding to 7 seconds at 50Hz) Format: int32_t

17.101 IMEM_SRAM_APEX_REG_413

Name: IMEM_SRAM_APEX_REG_413
Address: 413 (19Dh)
Serial IF: R/W
Reset value: 0x01

BIT	NAME	FUNCTION
7:0	B2S_TIMER_FLAT_REJECT[15:8]	A timer to disable flat rejection when age of the last no-flat B2S detection is over the timer Unit in sample number - ODR dependent Default value 350 (corresponding to 7 seconds at 50Hz) Format: int32_t

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17.102 IMEM_SRAM_APEX_REG_414

Name: IMEM_SRAM_APEX_REG_414
Address: 414 (19Eh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_TIMER_FLAT_REJECT[23:16]	A timer to disable flat rejection when age of the last no-flat B2S detection is over the timer Unit in sample number - ODR dependent Default value 350 (corresponding to 7 seconds at 50Hz) Format: int32_t

17.103 IMEM_SRAM_APEX_REG_415

Name: IMEM_SRAM_APEX_REG_415
Address: 415 (19Fh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	B2S_TIMER_FLAT_REJECT[31:24]	A timer to disable flat rejection when age of the last no-flat B2S detection is over the timer Unit in sample number - ODR dependent Default value 350 (corresponding to 7 seconds at 50Hz) Format: int32_t

17.104 IMEM_SRAM_APEX_REG_642

Name: IMEM_SRAM_APEX_REG_642
Address: 642 (282h)
Serial IF: R/W
Reset value: 0xC8

BIT	NAME	FUNCTION
7:0	TILT_WAIT_TIME[7:0]	Wait time in sample number before triggering the tilt event when the tilt threshold is reached or passed Unit: In sample number - ODR dependent Default value: 200 (corresponding to 4s at 50Hz) Recommended range value: [25 - 1000] Format: int16_t

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17.105 IMEM_SRAM_APEX_REG_643

Name: IMEM_SRAM_APEX_REG_643
Address: 643 (283h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	TILT_WAIT_TIME[15:8]	Wait time in sample number before triggering the tilt event when the tilt threshold is reached or passed Unit: In sample number - ODR dependent Default value: 200 (corresponding to 4s at 50Hz) Recommended range value: [25 - 1000] Format: int16_t

17.106 IMEM_SRAM_APEX_REG_644

Name: IMEM_SRAM_APEX_REG_644
Address: 644 (284h)
Serial IF: R/W
Reset value: 0xB2

BIT	NAME	FUNCTION
7:0	TILT_ANGLE_TH[7:0]	Tilt angle threshold to trigger tilt event Unit: Cosine value of angle in q30 Default value: 879557810 corresponding to 35 degrees Format: int32_t

17.107 IMEM_SRAM_APEX_REG_645

Name: IMEM_SRAM_APEX_REG_645
Address: 645 (285h)
Serial IF: R/W
Reset value: 0xFC

BIT	NAME	FUNCTION
7:0	TILT_ANGLE_TH[15:8]	Tilt angle threshold to trigger tilt event Unit: Cosine value of angle in q30 Default value: 879557810 corresponding to 35 degrees Format: int32_t

17.108 IMEM_SRAM_APEX_REG_646

Name: IMEM_SRAM_APEX_REG_646
Address: 646 (286h)
Serial IF: R/W
Reset value: 0x6C

BIT	NAME	FUNCTION
7:0	TILT_ANGLE_TH[23:16]	Tilt angle threshold to trigger tilt event Unit: Cosine value of angle in q30 Default value: 879557810 corresponding to 35 degrees Format: int32_t

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17.109 IMEM_SRAM_APEX_REG_647

Name: IMEM_SRAM_APEX_REG_647
Address: 647 (287h)
Serial IF: R/W
Reset value: 0x34

BIT	NAME	FUNCTION
7:0	TILT_ANGLE_TH[31:24]	Tilt angle threshold to trigger tilt event Unit: Cosine value of angle in q30 Default value: 879557810 corresponding to 35 degrees Format: int32_t

17.110 IMEM_SRAM_APEX_REG_648

Name: IMEM_SRAM_APEX_REG_648
Address: 648 (288h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	TAP_MIN_JERK[7:0]	The minimal value of jerk to be considered as a tap candidate Unit in LSB with 1 LSB = 1g / 2^12 (of the jerk value) Default for Tap config: 4608 corresponding to 1.125 g Default for Tap on Face config: 1400 corresponding to 0.342 g

17.111 IMEM_SRAM_APEX_REG_649

Name: IMEM_SRAM_APEX_REG_649
Address: 649 (289h)
Serial IF: R/W
Reset value: 0x12

BIT	NAME	FUNCTION
7:0	TAP_MIN_JERK[15:8]	The minimal value of jerk to be considered as a tap candidate Unit in LSB with 1 LSB = 1g / 2^12 (of the jerk value) Default for Tap config: 4608 corresponding to 1.125 g Default for Tap on Face config: 1400 corresponding to 0.342 g

17.112 IMEM_SRAM_APEX_REG_650

Name: IMEM_SRAM_APEX_REG_650
Address: 650 (28Ah)
Serial IF: R/W
Reset value: 0xFA

BIT	NAME	FUNCTION
7:0	TAP_TMAX[7:0]	Time window since the jerk maximum value, used to observe a single-tap, double-tap, triple-tap or rejection of the tap event Unit in sample number, ODR dependent Default for Tap config: 250 at 400Hz, corresponding to 0.625s Default for Tap on Face config: 800 at 800Hz corresponding to 1s

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17.113 IMEM_SRAM_APEX_REG_651

Name: IMEM_SRAM_APEX_REG_651
Address: 651 (28Bh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	TAP_TMAX[15:8]	Time window since the jerk maximum value, used to observe a single-tap, double-tap, triple-tap or rejection of the tap event Unit in sample number, ODR dependent Default for Tap config: 198 at 400Hz, corresponding to 0.495s Default for Tap on Face config: 800 at 800Hz corresponding to 1s

17.114 IMEM_SRAM_APEX_REG_652

Name: IMEM_SRAM_APEX_REG_652
Address: 652 (28Ch)
Serial IF: R/W
Reset value: 0x42

BIT	NAME	FUNCTION
7:0	TAP_TMIN[7:0]	Single tap window, sub-window within the TAP_TMAX to detect tap event Unit in sample number, ODR dependent Default for Tap config: 66 at 400Hz, representing 0.1650s Default for Tap on Face config: 110 at 800Hz, representing 0.138

17.115 IMEM_SRAM_APEX_REG_653

Name: IMEM_SRAM_APEX_REG_653
Address: 653 (28Dh)
Serial IF: R/W
Reset value: 0x22

BIT	NAME	FUNCTION
7:0	TAP_SMUDGE_REJECT_THR[7:0]	Corresponding to the maximum time spent over a threshold before rejecting the tap candidate, at the end of TAP_TMIN window, if internal counter of number of samples over the smudge threshold is below the TAP_SMUDGE_REJECT_TH, single-tap is detected. Unit in sample number, ODR dependent Default for Tap config: 34 at 400Hz, representing 0.085 s Default for Tap on Face config: 40 at 800Hz, representing 0.05s

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17.116 IMEM_SRAM_APEX_REG_654

Name: IMEM_SRAM_APEX_REG_654
Address: 654 (28Eh)
Serial IF: R/W
Reset value: 0x02

BIT	NAME	FUNCTION
7:0	TAP_MAX_PEAK_TOL[7:0]	Maximum peak tolerance is the percentage of pulse amplitude to get the smudge threshold of rejection Unit is enum - use range [1 - 4] Default for Tap config: 2 (corresponding to 25%) Default for Tap on Face config: 2 (corresponding to 25%)

17.117 IMEM_SRAM_APEX_REG_655

Name: IMEM_SRAM_APEX_REG_655
Address: 655 (28Fh)
Serial IF: R/W
Reset value: 0x08

BIT	NAME	FUNCTION
7:0	TAP_TAVG[7:0]	Energy measurement window size to determine the tap axis associated with the 1st tap Unit in sample number, ODR dependent Use value limited to [1, 2, 4, 8] Default for Tap config: 8 Default for Tap on Face config: 8 (axis discrimination is not used in this config)

17.118 IMEM_SRAM_APEX_REG_656

Name: IMEM_SRAM_APEX_REG_656
Address: 656 (290h)
Serial IF: R/W
Reset value: 0x02

BIT	NAME	FUNCTION
7:0	TAP_MAX[7:0]	Maximal number of tap quantity detected to be valid Unit is enum Range is [1, 2, 3] corresponding to [single, double, triple] Default for Tap config: 2 (double tap) Default for Tap on Face config: 3 (triple tap)

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17.119 IMEM_SRAM_APEX_REG_657

Name: IMEM_SRAM_APEX_REG_657
Address: 657 (291h)
Serial IF: R/W
Reset value: 0x02

BIT	NAME	FUNCTION
7:0	TAP_MIN[7:0]	Minimal number of tap quantity detected to be valid Unit is enum Range is [1, 2, 3] corresponding to [single, double, triple] Default for Tap config: 2 (double tap) Default for Tap on Face config: 2 (double tap)

17.120 IMEM_SRAM_APEX_REG_658

Name: IMEM_SRAM_APEX_REG_658
Address: 658 (292h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	TAP_ODR[7:0]	Enum for accelerometer ODR Acceptable value 0: 200Hz, 1: 400Hz, 2: 800Hz Default for Tap config: 1: 400Hz Default for Tap on Face config: 2: 800Hz

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18 USER BANK IMEM_SRAM_STC REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within user bank IMEM_SRAM_STC. The registers described in this section are indirect access registers. Section 14 describes the procedure for accessing indirect access registers.

18.1 IMEM_SRAM_STC_REG_1792

Name: IMEM_SRAM_STC_REG_1792
Address: 1792 (700h)
Serial IF: R/W
Reset value: Variable, depends on individual device trim

BIT	NAME	FUNCTION
7:0	GYRO_X_STR_FT[7:0]	Trimmed response for use in gyro X-axis self-test calculations.

18.2 IMEM_SRAM_STC_REG_1793

Name: IMEM_SRAM_STC_REG_1793
Address: 1793 (701h)
Serial IF: R/W
Reset value: Variable, depends on individual device trim

BIT	NAME	FUNCTION
7:0	GYRO_X_STR_FT[15:8]	Trimmed response for use in gyro X-axis self-test calculations.

18.3 IMEM_SRAM_STC_REG_1794

Name: IMEM_SRAM_STC_REG_1794
Address: 1794 (702h)
Serial IF: R/W
Reset value: Variable, depends on individual device trim

BIT	NAME	FUNCTION
7:0	GYRO_Y_STR_FT[7:0]	Trimmed response for use in gyro Y-axis self-test calculations.

18.4 IMEM_SRAM_STC_REG_1795

Name: IMEM_SRAM_STC_REG_1795
Address: 1795 (703h)
Serial IF: R/W
Reset value: Variable, depends on individual device trim

BIT	NAME	FUNCTION
7:0	GYRO_Y_STR_FT[15:8]	Trimmed response for use in gyro Y-axis self-test calculations.

18.5 IMEM_SRAM_STC_REG_1796

Name: IMEM_SRAM_STC_REG_1796
Address: 1796 (704h)
Serial IF: R/W
Reset value: Variable, depends on individual device trim

BIT	NAME	FUNCTION
7:0	GYRO_Z_STR_FT[7:0]	Trimmed response for use in gyro Z-axis self-test calculations.

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18.6 IMEM_SRAM_STC_REG_1797

Name: IMEM_SRAM_STC_REG_1797
Address: 1797 (705h)
Serial IF: R/W
Reset value: Variable, depends on individual device trim

BIT	NAME	FUNCTION
7:0	GYRO_Z_STR_FT[15:8]	Trimmed response for use in gyro Z-axis self-test calculations.

18.7 IMEM_SRAM_STC_REG_1798

Name: IMEM_SRAM_STC_REG_1798
Address: 1798 (706h)
Serial IF: R/W
Reset value: Variable, depends on individual device trim

BIT	NAME	FUNCTION
7:0	ACCEL_X_STR_FT[7:0]	Trimmed response for use in accel X-axis self-test calculations.

18.8 IMEM_SRAM_STC_REG_1799

Name: IMEM_SRAM_STC_REG_1799
Address: 1799 (707h)
Serial IF: R/W
Reset value: Variable, depends on individual device trim

BIT	NAME	FUNCTION
7:0	ACCEL_X_STR_FT[15:8]	Trimmed response for use in accel X-axis self-test calculations.

18.9 IMEM_SRAM_STC_REG_1800

Name: IMEM_SRAM_STC_REG_1800
Address: 1800 (708h)
Serial IF: R/W
Reset value: Variable, depends on individual device trim

BIT	NAME	FUNCTION
7:0	ACCEL_Y_STR_FT[7:0]	Trimmed response for use in accel Y-axis self-test calculations.

18.10 IMEM_SRAM_STC_REG_1801

Name: IMEM_SRAM_STC_REG_1801
Address: 1801 (709h)
Serial IF: R/W
Reset value: Variable, depends on individual device trim

BIT	NAME	FUNCTION
7:0	ACCEL_Y_STR_FT[15:8]	Trimmed response for use in accel Y-axis self-test calculations.

18.11 IMEM_SRAM_STC_REG_1802

Name: IMEM_SRAM_STC_REG_1802
Address: 1802 (70Ah)
Serial IF: R/W
Reset value: Variable, depends on individual device trim

BIT	NAME	FUNCTION
7:0	ACCEL_Z_STR_FT[7:0]	Trimmed response for use in accel Z-axis self-test calculations.

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18.12 IMEM_SRAM_STC_REG_1803

Name: IMEM_SRAM_STC_REG_1803
Address: 1803 (70Bh)
Serial IF: R/W
Reset value: Variable, depends on individual device trim

BIT	NAME	FUNCTION
7:0	ACCEL_Z_STR_FT[15:8]	Trimmed response for use in accel Z-axis self-test calculations.

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19 USER BANK IMEM_SIGP REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within user bank IMEM_SIGP. The registers described in this section are indirect access registers. Section 14 describes the procedure for accessing indirect access registers.

19.1 IMEM_SIGP_REG_128

Name: IMEM_SIGP_REG_128
Address: 128 (80h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_X_GOS_GAIN_USER [7:0]	[Supports Dynamic Change] Accel X axis User gain adjustment Range: 0 to 2 Resolution: 2^-11 (~0.05%) [Extended from unsigned 12 bit(s) to signed 16 bit(s)]

19.2 IMEM_SIGP_REG_129

Name: IMEM_SIGP_REG_129
Address: 129 (81h)
Serial IF: R/W
Reset value: 0x08

BIT	NAME	FUNCTION
7:0	ACCEL_X_GOS_GAIN_USER [15:8]	[Supports Dynamic Change] Accel X axis User gain adjustment Range: 0 to 2 Resolution: 2^-11 (~0.05%) [Extended from unsigned 12 bit(s) to signed 16 bit(s)]

19.3 IMEM_SIGP_REG_148

Name: IMEM_SIGP_REG_148
Address: 148 (94h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_X_GOS_OFF_USER[7:0]	[Supports Dynamic Change] Accel X axis User Offset adjustment Range: ±1 gee Resolution: 0.122 mg [Extended from signed 14 bit(s) to signed 16 bit(s)]

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19.4 IMEM_SIGP_REG_149

Name: IMEM_SIGP_REG_149
Address: 149 (95h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_X_GOS_OFF_USER[15:8]	[Supports Dynamic Change] Accel X axis User Offset adjustment Range: ±1 gee Resolution: 0.122 mg [Extended from signed 14 bit(s) to signed 16 bit(s)]

19.5 IMEM_SIGP_REG_328

Name: IMEM_SIGP_REG_328
Address: 328 (148h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_Y_GOS_GAIN_USER[7:0]	[Supports Dynamic Change] Accel Y axis User gain adjustment Range: 0 to 2 Resolution: 2^-11 (~0.05%) [Extended from unsigned 12 bit(s) to signed 16 bit(s)]

19.6 IMEM_SIGP_REG_329

Name: IMEM_SIGP_REG_329
Address: 329 (149h)
Serial IF: R/W
Reset value: 0x08

BIT	NAME	FUNCTION
7:0	ACCEL_Y_GOS_GAIN_USER[15:8]	[Supports Dynamic Change] Accel Y axis User gain adjustment Range: 0 to 2 Resolution: 2^-11 (~0.05%) [Extended from unsigned 12 bit(s) to signed 16 bit(s)]

19.7 IMEM_SIGP_REG_348

Name: IMEM_SIGP_REG_348
Address: 348 (15Ch)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_Y_GOS_OFF_USER[7:0]	[Supports Dynamic Change] Accel Y axis User Offset adjustment Range: ±1 gee Resolution: 0.122 mg [Extended from signed 14 bit(s) to signed 16 bit(s)]

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19.8 IMEM_SIGP_REG_349

Name: IMEM_SIGP_REG_349
Address: 349 (15Dh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_Y_GOS_OFF_USER[15:8]	[Supports Dynamic Change] Accel Y axis User Offset adjustment Range: ±1 gee Resolution: 0.122 mg [Extended from signed 14 bit(s) to signed 16 bit(s)]

19.9 IMEM_SIGP_REG_528

Name: IMEM_SIGP_REG_528
Address: 528 (210h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_Z_GOS_GAIN_USER[7:0]	[Supports Dynamic Change] Accel Z axis User gain adjustment Range: 0 to 2 Resolution: 2^-11 (~0.05%) [Extended from unsigned 12 bit(s) to signed 16 bit(s)]

19.10 IMEM_SIGP_REG_529

Name: IMEM_SIGP_REG_529
Address: 529 (211h)
Serial IF: R/W
Reset value: 0x08

BIT	NAME	FUNCTION
7:0	ACCEL_Z_GOS_GAIN_USER[15:8]	[Supports Dynamic Change] Accel Z axis User gain adjustment Range: 0 to 2 Resolution: 2^-11 (~0.05%) [Extended from unsigned 12 bit(s) to signed 16 bit(s)]

19.11 IMEM_SIGP_REG_548

Name: IMEM_SIGP_REG_548
Address: 548 (224h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_Z_GOS_OFF_USER[7:0]	[Supports Dynamic Change] Accel Z axis User Offset adjustment Range: ±1 gee Resolution: 0.122 mg [Extended from signed 14 bit(s) to signed 16 bit(s)]

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19.12 IMEM_SIGP_REG_549

Name: IMEM_SIGP_REG_549
Address: 549 (225h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ACCEL_Z_GOS_OFF_USER[15:8]	[Supports Dynamic Change] Accel Z axis User Offset adjustment Range: ±1 gee Resolution: 0.122 mg [Extended from signed 14 bit(s) to signed 16 bit(s)]

19.13 IMEM_SIGP_REG_728

Name: IMEM_SIGP_REG_728
Address: 728 (2D8h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	GYRO_X_GOS_GAIN_USER[7:0]	[Supports Dynamic Change] Gyro X axis User gain Range: 0 to 2 Resolution: 2^-11 (~0.05%) [Extended from unsigned 12 bit(s) to signed 16 bit(s)]

19.14 IMEM_SIGP_REG_729

Name: IMEM_SIGP_REG_729
Address: 729 (2D9h)
Serial IF: R/W
Reset value: 0x08

BIT	NAME	FUNCTION
7:0	GYRO_X_GOS_GAIN_USER[15:8]	[Supports Dynamic Change] Gyro X axis User gain Range: 0 to 2 Resolution: 2^-11 (~0.05%) [Extended from unsigned 12 bit(s) to signed 16 bit(s)]

19.15 IMEM_SIGP_REG_748

Name: IMEM_SIGP_REG_748
Address: 748 (2ECh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	GYRO_X_GOS_OFF_USER[7:0]	[Supports Dynamic Change] Gyro X axis User offset adjustment Range: ±62.5 dps Resolution: 7.63 mdps [Extended from signed 14 bit(s) to signed 16 bit(s)]

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19.16 IMEM_SIGP_REG_749

Name: IMEM_SIGP_REG_749
Address: 749 (2EDh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	GYRO_X_GOS_OFF_USER[15:8]	[Supports Dynamic Change] Gyro X axis User offset adjustment Range: ±62.5 dps Resolution: 7.63 mdps [Extended from signed 14 bit(s) to signed 16 bit(s)]

19.17 IMEM_SIGP_REG_976

Name: IMEM_SIGP_REG_976
Address: 976 (3D0h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	GYRO_Y_GOS_GAIN_USER[7:0]	[Supports Dynamic Change] Gyro Y axis User gain Range: 0 to 2 Resolution: 2^-11 (~0.05%) [Extended from unsigned 12 bit(s) to signed 16 bit(s)]

19.18 IMEM_SIGP_REG_977

Name: IMEM_SIGP_REG_977
Address: 977 (3D1h)
Serial IF: R/W
Reset value: 0x08

BIT	NAME	FUNCTION
7:0	GYRO_Y_GOS_GAIN_USER[15:8]	[Supports Dynamic Change] Gyro Y axis User gain Range: 0 to 2 Resolution: 2^-11 (~0.05%) [Extended from unsigned 12 bit(s) to signed 16 bit(s)]

19.19 IMEM_SIGP_REG_996

Name: IMEM_SIGP_REG_996
Address: 996 (3E4h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	GYRO_Y_GOS_OFF_USER[7:0]	[Supports Dynamic Change] Gyro Y axis User offset adjustment Range: ±62.5 dps Resolution: 7.63 mdps [Extended from signed 14 bit(s) to signed 16 bit(s)]

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19.20 IMEM_SIGP_REG_997

Name: IMEM_SIGP_REG_997
Address: 997 (3E5h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	GYRO_Y_GOS_OFF_USER[15:8]	[Supports Dynamic Change] Gyro Y axis User offset adjustment Range: ±62.5 dps Resolution: 7.63 mdps [Extended from signed 14 bit(s) to signed 16 bit(s)]

19.21 IMEM_SIGP_REG_1224

Name: IMEM_SIGP_REG_1224
Address: 1224 (4C8h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	GYRO_Z_GOS_GAIN_USER[7:0]	[Supports Dynamic Change] Gyro Z axis User gain Range: 0 to 2 Resolution: 2^-11 (~0.05%) [Extended from unsigned 12 bit(s) to signed 16 bit(s)]

19.22 IMEM_SIGP_REG_1225

Name: IMEM_SIGP_REG_1225
Address: 1225 (4C9h)
Serial IF: R/W
Reset value: 0x08

BIT	NAME	FUNCTION
7:0	GYRO_Z_GOS_GAIN_USER[15:8]	[Supports Dynamic Change] Gyro Z axis User gain Range: 0 to 2 Resolution: 2^-11 (~0.05%) [Extended from unsigned 12 bit(s) to signed 16 bit(s)]

19.23 IMEM_SIGP_REG_1244

Name: IMEM_SIGP_REG_1244
Address: 1244 (4DCh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	GYRO_Z_GOS_OFF_USER[7:0]	[Supports Dynamic Change] Gyro Z axis User offset adjustment Range: ±62.5 dps Resolution: 7.63 mdps [Extended from signed 14 bit(s) to signed 16 bit(s)]

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19.24 IMEM_SIGP_REG_1245

Name: IMEM_SIGP_REG_1245
Address: 1245 (4DDh)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	GYRO_Z_GOS_OFF_USER[15:8]	[Supports Dynamic Change] Gyro Z axis User offset adjustment Range: ±62.5 dps Resolution: 7.63 mdps [Extended from signed 14 bit(s) to signed 16 bit(s)]

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20 USER BANK IPREG_BAR REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within user bank IPREG_BAR. The registers described in this section are indirect access registers. Section 14 describes the procedure for accessing indirect access registers.

20.1 IPREG_BAR_REG_94

Name: IPREG_BAR_REG_94
Address: 94 (5Eh)
Serial IF: R/W
Reset value: 0xD9

BIT	NAME	FUNCTION
7	PADS_AP_SCLK_PUD_TRIM_D2A[0]	Selects internal resistor pull direction for AP_SCLK pin (pin 12) 0: Down 1: Up Can be changed on-the-fly.
6	PADS_AP_SCLK_PE_TRIM_D2A[0]	Enables internal pull resistor to pull up or down for AP_SCLK pin (pin 12), depending on direction selected by bit 7 0: Not enabled 1: Enabled Can be changed on-the-fly.
5	-	Reserved
4	PADS_AP_CS_PUD_TRIM_D2A[0]	Selects internal resistor pull direction for AP_CS pin (pin 10) 0: Down 1: Up Can be changed on-the-fly.
3	PADS_AP_CS_PE_TRIM_D2A[0]	Enables internal pull resistor to pull up or down for AP_CS pin (pin 10), depending on direction selected by bit 4. 0: Not enabled 1: Enabled Can be changed on-the-fly.
2:0	-	Reserved

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20.2 IPREG_BAR_REG_95

Name: IPREG_BAR_REG_95
Address: 95 (5Fh)
Serial IF: R/W
Reset value: 0x56

BIT	NAME	FUNCTION
7:6	-	Reserved
5	PADS_AP_SDO_PUD_TRIM_D2A[0]	Selects internal resistor pull direction for AP_SDO pin (pin 1) 0: Down 1: Up Can be changed on-the-fly.
4	PADS_AP_SDO_PE_TRIM_D2A[0]	Enables internal pull resistor to pull up or down for AP_SDO pin (pin 1), depending on direction selected by bit 5. 0: Not enabled 1: Enabled Can be changed on-the-fly.
3	-	Reserved
2	PADS_AP_SDI_PUD_TRIM_D2A[0]	Selects internal resistor pull direction for AP_SDI pin (pin 2) 0: Down 1: Up Can be changed on-the-fly.
1	PADS_AP_SDI_PE_TRIM_D2A[0]	Enables internal pull resistor to pull up or down for AP_SDI pin (pin 2), depending on direction selected by bit 2. 0: Not enabled 1: Enabled Can be changed on-the-fly.
0	-	Reserved

20.3 IPREG_BAR_REG_237

Name: IPREG_BAR_REG_237
Address: 237 (EDh)
Serial IF: R/W
Reset value: 0x04

BIT	NAME	FUNCTION
7:4	-	Reserved
3	TEMP_FORCE_ON_RR_TIMING_TRIM_D2D[0]	Controls the duty-cycling of the Temperature Sensor amplifier: 0: Temperature Sensor amplifier is disabled between measurements, to save power. 1: Temperature Sensor amplifier remains enabled between measurements. Must be set to 1 (remains enabled) when using Off-Grid mode.
2:0	-	Reserved

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21 USER BANK IPREG_SYS1 REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within user bank IPREG_SYS1. The registers described in this section are indirect access registers. Section 14 describes the procedure for accessing indirect access registers.

21.1 IPREG_SYS1_REG_9

Name: IPREG_SYS1_REG_9
Address: 09 (09h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:3	-	Reserved
2:0	GYRO_LPF_BW_SEL[2:0]	[Supports Dynamic Change] Gyro UI path: Low Pass Filter nominal cutoff frequency 0: ODR/2 1: ODR/4 2: ODR/8 3: ODR/16 4: ODR/32 5: ODR/64 6,7: ODR/128 NOTE: The real bandwidth is smaller than the nominal one at high ODR or BW

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22 USER BANK IPREG_SYS2 REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within user bank IPREG_SYS2. The registers described in this section are indirect access registers. Section 14 describes the procedure for accessing indirect access registers.

22.1 IPREG_SYS2_REG_6

Name: IPREG_SYS2_REG_6
Address: 06 (06h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:3	-	Reserved
2:0	ACCEL_LPF_BW_SEL[2:0]	[Supports Dynamic Change] Accel UI path: Low Pass Filter nominal cutoff frequency 0: ODR/2 1: ODR/4 2: ODR/8 3: ODR/16 4: ODR/32 5: ODR/64 6,7: ODR/128 NOTE: The real bandwidth is smaller than the nominal one at high ODR or BW

22.2 IPREG_SYS2_REG_8

Name: IPREG_SYS2_REG_8
Address: 08 (08h)
Serial IF: R/W
Reset value: 0x01

BIT	NAME	FUNCTION
7:4	-	Reserved
3:0	ACCEL_LP_AVG_SEL[3:0]	[Supports Dynamic Change] Accel Low Power Mode Average Selection 0: 1 sample average 1: 2 sample average 2: 3 sample average 3: 4 sample average 4: 5 sample average 5: 7 sample average 6: 8 sample average 7: 10 sample average 8: 11 sample average 9: 16 sample average 10: 18 sample average 11: 20 sample average 12: 32 sample average 13-15: 64 sample average

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23 USER BANK IPREG_TOP1 REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within user bank IPREG_TOP1. The registers described in this section are indirect access registers. Section 14 describes the procedure for accessing indirect access registers.

23.1 I3C_CONFIG

Name: I3C_CONFIG
Address: 06 (06h)
Serial IF: R/W
Reset value: 0x0B

BIT	NAME	FUNCTION
7:2	-	Reserved
1	IBI_EN[0]	0: Disable IBI operation 1: Enable IBI operation
0	SDR_EN[0]	0: I3C SDR operation disabled – I3C IP operates only in I2C mode 1: I3C SDR operation enabled

23.2 SMC_CONTROL_0

Name: SMC_CONTROL_0
Address: 07 (07h)
Serial IF: R/W
Reset value: 0x05

BIT	NAME	FUNCTION
7:3	-	Reserved
2:0	ULP_ED_RCOSC_WU_TRIM [2:0]	Number of ODR ticks (under the WU-osc) required for the RC-osc to turn on from a complete OFF state.

23.3 SMC_CONTROL_1

Name: SMC_CONTROL_1
Address: 08 (08h)
Serial IF: R/W
Reset value: 0x0C

BIT	NAME	FUNCTION
7:5	-	Reserved
4	RESERVED	Must be 0
3	GYRO_AP_EN[0]	1: Enable the Gyroscope signal path at the UI/AP interface
2	ACCEL_AP_EN[0]	1: Enable the Accelerometer signal path at the UI/AP interface
1	EN_OFFGRID_MODE[0]	Enable the “Off-Grid” mode: 0: ODRs are “On-Grid”, per the ODR table. 1: ODRs are “Off-Grid”, skewed by the ODR Tick period programmed in TICK_PER_FRC/TICK_PER_FRC_SUB, relative to the nominal ODR Tick of 6.4kHz.
0	TEMP_DIS[0]	1: Disable temperature sensor

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23.4 FIFO_CONFIG0

Name: FIFO_CONFIG0
Address: 23 (17h)
Serial IF: R/W
Reset value: 0x03

BIT	NAME	FUNCTION
7:2	-	Reserved
1:0	FIFO_DEPTH[1:0]	Sets the FIFO depth in bytes and FIFO base address. 0: 256 bytes 1: 512 bytes 2: 768 bytes 3: 1024 bytes

23.5 SREG_CONFIG1

Name: SREG_CONFIG1
Address: 24 (18h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:4	-	Reserved
3:2	NXT_WR_BNK[1:0]	Points to bank available for new SREG data write.
1:0	NXT_NEW_BNK[1:0]	Points to the bank where new SREG data was written. Can be changed on-the-fly.

23.6 EDMP_INT_ENABLE

Name: EDMP_INT_ENABLE
Address: 25 (19h)
Serial IF: R/W
Reset value: 0x03

BIT	NAME	FUNCTION
7:2	-	Reserved
1	EDMP_INT_EN_ON_DEMAND_REQ[0]	On demand_req interrupt enable bit for eDMP
0	EDMP_INT_EN_ODR_EVENT[0]	ODR event interrupt enable bit for eDMP

23.7 EDMP_INT_STATUS

Name: EDMP_INT_STATUS
Address: 27 (1Bh)
Serial IF: R/C
Reset value: 0x00

BIT	NAME	FUNCTION
7:2	-	Reserved
1	EDMP_INT_STATUS_ON_DEMAND_REQ[0]	On demand_req interrupt status bit for eDMP
0	EDMP_INT_STATUS_ODR_EVENT[0]	ODR event interrupt status bit for eDMP

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23.8 SELFTEST

Name: SELFTEST
Address: 51 (33h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:6	-	Reserved
5	EN_GZ_ST[0]	Gyro Z-axis self-test mode enable 0: Gyro Z-axis operates in normal mode 1: Gyro Z-axis operates in self-test mode
4	EN_GY_ST[0]	Gyro Y-axis self-test mode enable 0: Gyro Y-axis operates in normal mode 1: Gyro Y-axis operates in self-test mode
3	EN_GX_ST[0]	Gyro X-axis self-test mode enable 0: Gyro X-axis operates in normal mode 1: Gyro X-axis operates in self-test mode
2	EN_AZ_ST[0]	Accel Z-axis self-test mode enable 0: Accel Z-axis operates in normal mode 1: Accel Z-axis operates in self-test mode
1	EN_AY_ST[0]	Accel Y-axis self-test mode enable 0: Accel Y-axis operates in normal mode 1: Accel Y-axis operates in self-test mode
0	EN_AX_ST[0]	Accel X-axis self-test mode enable 0: Accel X-axis operates in normal mode 1: Accel X-axis operates in self-test mode

23.9 EDMP_PRGRM_IRQ0_0

Name: EDMP_PRGRM_IRQ0_0
Address: 230 (E6h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	PRGRM_STRT_ADDR_IRQ_0[7:0]	[Supports Dynamic Change] Start address of IRQ_0 vector

23.10 EDMP_PRGRM_IRQ0_1

Name: EDMP_PRGRM_IRQ0_1
Address: 231 (E7h)
Serial IF: R/W
Reset value: 0x0C

BIT	NAME	FUNCTION
7:5	-	Reserved
4:0	PRGRM_STRT_ADDR_IRQ_0[12:8]	[Supports Dynamic Change] Start address of IRQ_0 vector

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23.11 EDMP_SP_START_ADDR

Name: EDMP_SP_START_ADDR
Address: 232 (E8h)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7	-	Reserved
6:0	SP_START_ADDR[6:0]	[Supports Dynamic Change] Bit [12:6] of AHB address of SRAM allocated for DMP stack. Default=0x0

23.12 EDMP_CFG

Name: EDMP_CFG
Address: 233 (E9h)
Serial IF: RWS
Reset value: 0x00

BIT	NAME	FUNCTION
7:3	-	Reserved
2	EDMP_AUTH[0]	EDMP Authentication register Host programs register to '1'. This starts eDMP's authentication operation. Once complete, eDMP writes register value to '0'
1	EDMP_INIT[0]	EDMP Init register Host programs register to '1'. This starts eDMP's initialization operation. Once complete, eDMP writes register value to '0'
0	FORCED_ODR[0]	Forced ODR register for debugging, not for mission mode operation Generates ODR event interrupt. Self-cleared register will always read ‘0’

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24 SMARTMOTION PRODUCT FAMILY

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25 REFERENCE

Please refer to the following application notes for additional information.

- IMU PCB Design and MEMS Assembly Guidelines (AN-000393)
- Understanding IMU Sensor Offset (AN-000257)
- TDK InvenSense IMU Calibration Application Note (AN-000265)
- ICM-51607 and T-3488 User Guide (AN-000529)
- ICM-506xx ICM-516xx T-34xx Errata (AN-000524)

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26 REVISION HISTORY

REVISION DATE	REVISION	DESCRIPTION
01/14/2026	0.1	Initial Release
03/11/2026	1.0	Updated Specifications (Cover Page; Tables 1, 2, 3)

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