Datasheet

ADS6133

1D Time of Flight Sensor

Version 1.2 | Jun. 3, 2026

[Note]

Please be aware that most values written in the datasheet are in the **preliminary stages**.

As continual tests and improvements are being implemented, Adapts Photonics reserves the right to change any information without prior notice.

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Introduction

Features & Benefits

- **High accuracy multi object detection ranging sensor**
  - Single Photon Avalanche Photodiode (SPAD) histogram-based architecture
  - Typical full FoV: 24° single zone detect with multi-objects detection (three objects).
  - High accurate detection with long and short distance.
  - Up to 5000 mm detection with full FoV (Field of View).
  - 30 Hz frame rate capability (turn the laser pulse to option the different frame rate).

- **Fully integrated miniature module with an MCU**
  - Size: 4.4 mm x 2.4 mm x 1.0 mm.
  - Invisible light vertical cavity surface emitting 940nm laser (VCSEL) and integrated pulse laser driver.
  using metalens on both transmitter and receiver.
  - Receiving array of single photon avalanche diodes (SPADs).
  - Low-power microcontroller running firmware.



- **Easy integration**
  - Single reflowable component.
  - I²C interface (up to 1MHz).
  - I²C communication interface is compatible with 1.2V, 1.8V and 3.3V.
  - Provide interruption pin for frame ready events.
  - Flexible power supply options, 2.8V to 3.3V.
  - Works with many types of cover glass materials and compensate for smudge on glass.
  - Class 1 Eye Safety.

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Description

ADS6133is a direct time-of-flight (DToF), multi object ranging sensor that can range up to 3 objects. The sensor module is housed in a miniature reflowable package, integrating a SPAD array, physical infrared filters, and metalens. The sensor is based on SPAD, TDC and histogram technology. All processing of the raw data is performed on-chip and it provides distance information together with confidence values on its interface.

Applications

This sensor can be used in many applications including:

- Assist camera auto-focus, enhance the camera auto-focus (AF) system performance.

  Improve camera performance in low light and low contrast scenes.
- Presence detection.
- Collision avoidance for robots.
- Keystone correction for video projectors.
- 1D gesture recognition.
- Distance measurement.
- IoT (User and object detection).

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1. Module Description

1.1. Block Diagram

The functional blocks of this device are shown below:

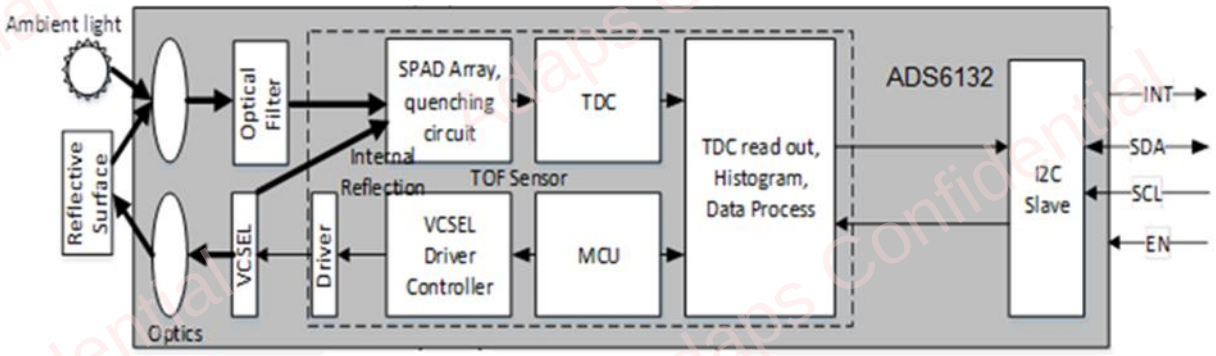


Figure 1-1 ADS6133 Block Diagram

1.2. Pin Diagram

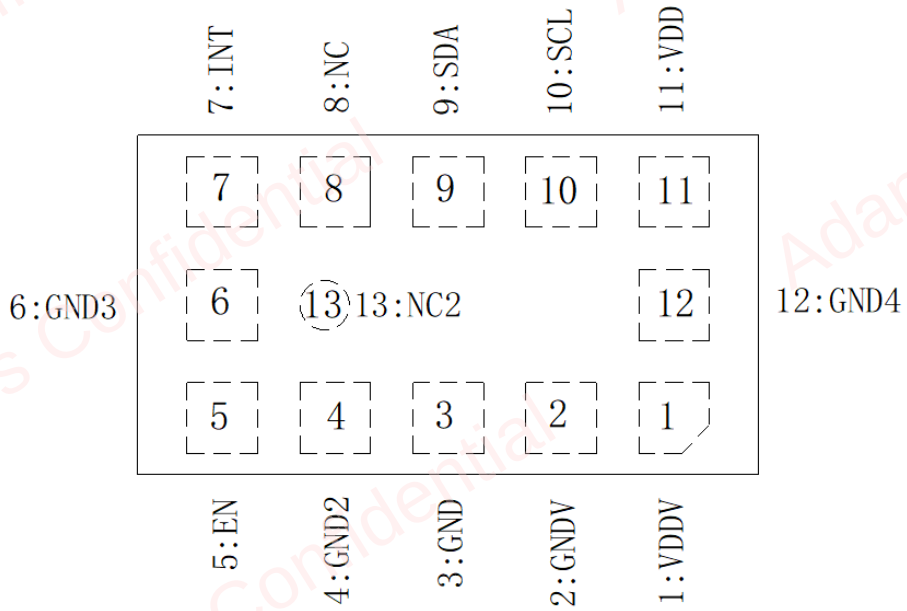


Figure 1-2 ADS6133 Pin Diagram (TOP VIEW)

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1.3. Pin Description

Table 1-1 Pin Description

Pin Name	OLGA12	Signal Type	Description
VDDV	1	Power supply	VCSEL supply, to be connected to main supply
GNDV	2	Ground	VCSEL ground, to be connected to main ground
GND	3	Ground	to be connected to main ground
GND2	4	Ground	to be connected to main ground
EN	5	Digital input	Chip enable pin, active low
GND3	6	Ground	to be connected to main ground
INT(1)	7	Digital output	Interrupt pin
NC	8		Don't connect.
SDA (1)	9	Digital IO	I²C data
SCL (1)	10	Digital input	I²C clock input
VDD	11	Power supply	Chip Power Supply, to be connected to main supply
GND4	12	Ground	to be connected to main ground
NC2	13		Don't connect.

Note(1) : IO voltage of chip can be set 1.2V, 1.8V and 3.3V by IO_LVL_CFG register, it is recommended to keep same with the VCCIO.

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2. Application Information

2.1. Application Schematic

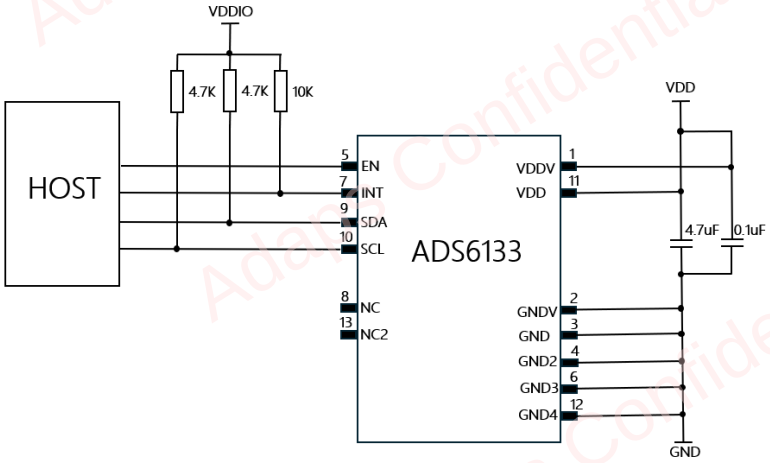


Figure 2-1 ADS6133 Application Schematic

Notes:

1. INT pulled-up recommended value is 10k Ohms.

2. At an I²C operating speed of 400kHz, the recommended pull-up resistor value of the SDA and SCL lines is 4.7k ohms. For other speeds, the resistor value should be adjusted based on the specific application requirements.

2.2. PCB Layout Recommendation

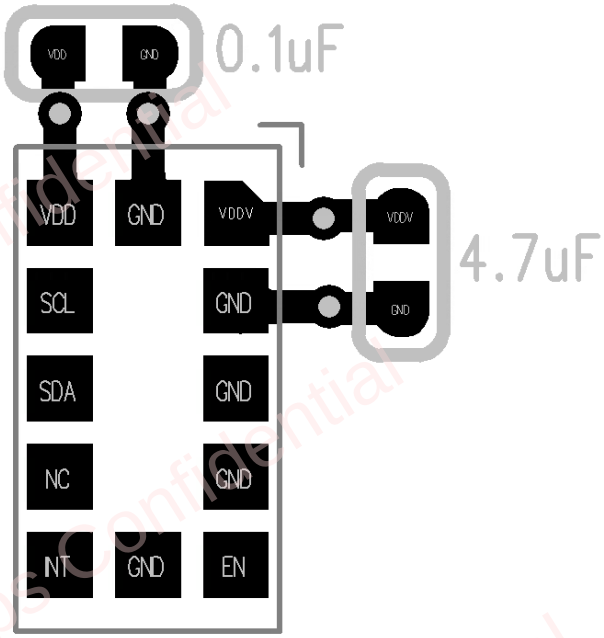


Figure 2-2 ADS6133 PCB Layout Recommendation

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Note:

1.Bypass capacitors should be placed as close as possible to the supply and ground pins.

2.The output voltage ripple of the TOF power supply IC shall not exceed 1%.

3.Each module power pin shall be routed independently without daisy-chain connections. Star-topology power routing is recommended to minimize supply coupling and noise.

3. Electrical Characteristics

3.1. Absolute Maximum Ratings

Table 3-1 Electrical Parameters

Symbol	Parameter	Min.	Max.	Unit
VDD, VDDV	Supply 3V Voltage to GND	-0.3	3.6	V
GND, GND2, GND3, GND4, GNDV	Ground	0	0	V
INT	Digital output	-0.3	3.6	V
SDA	Digital I/O	-0.3	3.6	V
SCL	Digital input	-0.3	3.6	V
EN	Analog input	-0.3	3.6	V

3.2. Digital input and output

Table 3-2 Electrical Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
INT, SCL, SDA					
VIL	Low level input voltage	-0.3	-	0.3 * VCCIO	V
VIH	High level input voltage	0.7 * VCCIO		VCCIO	
VOL	Low level output voltage (I_{out} = 6mA)	-		0.4	
VOH	High level output voltage (I_{out} = 6mA)	0.8 * VCCIO		-	
IIL	Low level input leakage@ Vi = 0V	-0.15		0.15	uA
IIH	High level input leakage@ Vi=1.1*VCCIO	-10		10	
EN					
VIL	Low level input voltage	-0.3	-	0.3 * VCCIO	V
VIH	High level input voltage	0.7 * VCCIO		VCCIO	
IIL	Low level input leakage@ Vi = 0V	-0.15		0.15	uA
IIH	High level input leakage@ Vi=1.1*VCCIO	-10		10	

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3.3. ESD

Electrostatic discharge

The ADS6133 module is compliant with electrostatic discharge (ESD) values presented in the table below.

Table 3-3 ESD Performance

Parameter	Specification	Condition
Human body model	ANS/ESDA/JEDEC JS-001-2023	± 2000V, 1500 Ohms, 100pF
Charged device model	ANSI/ESDA/JEDEC JS-002-2022	± 500 V

3.4. Temperature

Table 3-4 Temperature Ranges and Storage Conditions

Symbol	Parameter	Min.	Max.	Unit	Comments
T_{STRG}	Storage Temperature Range	-40	85	°C	
T_{BODY}	Package Body Temperature		260 °C (max)	°C	IPC / JEDEC J-STD-020 The reflow peak soldering temperature (body temperature) is specified according to IPC / JEDEC J-STD-020 “Moisture / Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices.”
RH_{NC}	Relative Humidity (non-condensing)		85	%	

3.5. MSL

Moisture sensitivity level

Moisture sensitivity level (MSL) is level 3 as described in IPC/JEDEC JSTD-020-C.

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3.6. Typical Operating Conditions

Device parameters are guaranteed at nominal conditions unless otherwise noted. While the device is operational across the temperature range, functionality will vary with temperature.

Table 3-5 Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
AVDD, AVDDVSCEL	Power Supply to GND	2.8	3.3	3.6	V
Temperature Range	Free-air temperature	-20	25	85	°C

3.7. Power Consumption

Table 3-6 Power consumption with typical condition

Mode	Typ.	Unit
HW Standby	2	uA
SW Standby	15.8	uA
Active Ranging	22	mA

3.8. Power Sequence

There are two options available for device power up/boot.

Option1: The EN pin is connected and controlled by host. HW standby is defined as the period when VDD is present and EN is low.

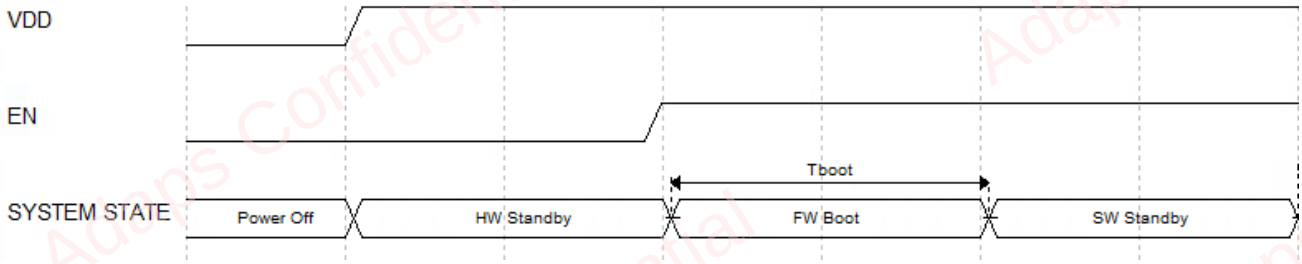


Figure 3-1 Power up and boot sequence (EN is controlled)

Option2: The EN pin is not controlled by host, it is tied to VDD through the pull-up resistor. In this case, the device goes to SW standby automatically after FW BOOT, without HW standby.

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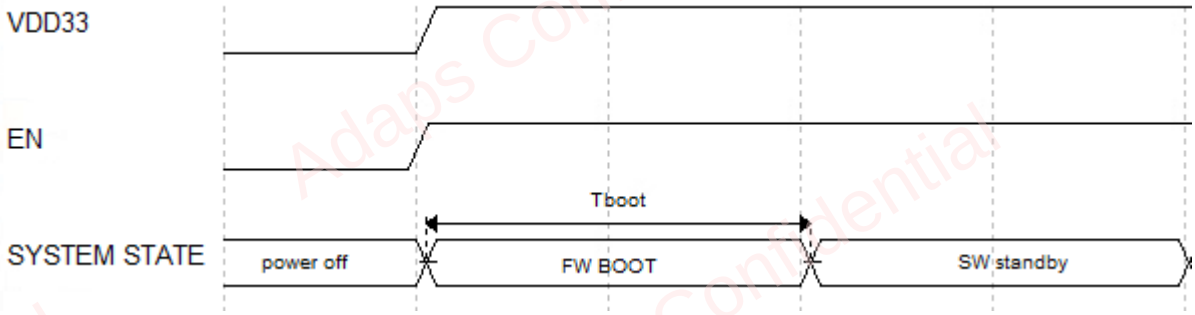


Figure 3-2 Power up and boot sequence (EN is not controlled)

3.9. State Machine

The diagram of the state machine is shown below:

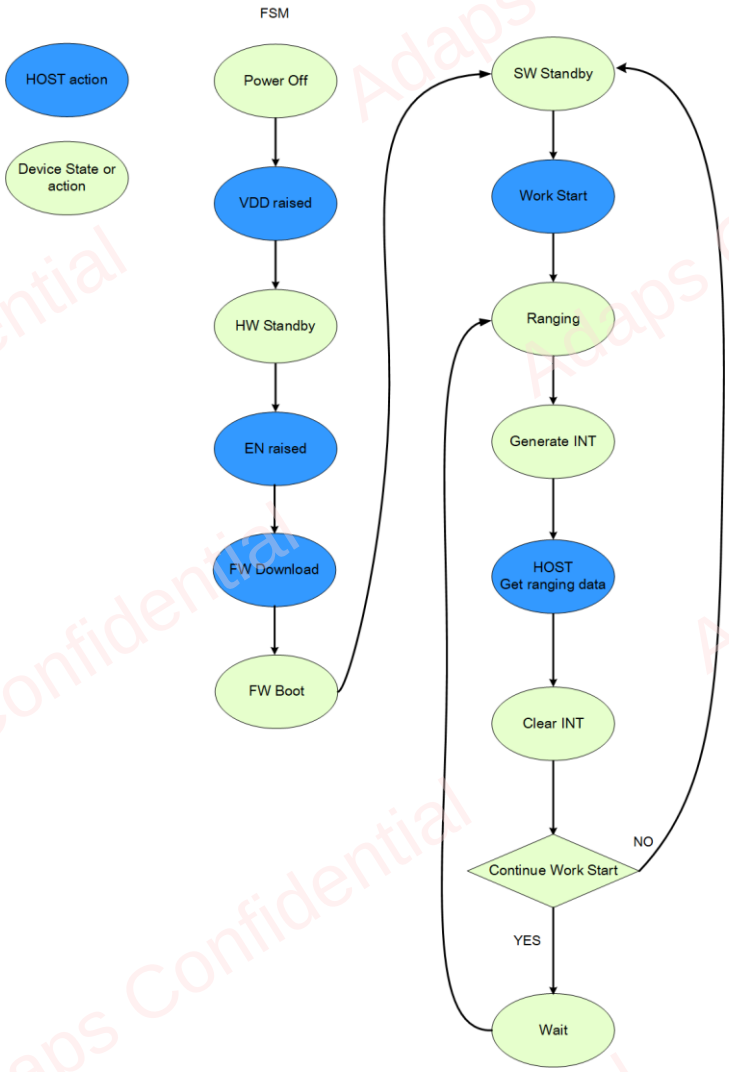


Figure 3-3 State Machine

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3.10. Interrupt Behavior and Ranging Timing

The INT pin is controlled by MCU, which level width and the polarity are configured by register. The interruption will be active at the end of each frame and can be cleared by MCU after host gets ranging data.

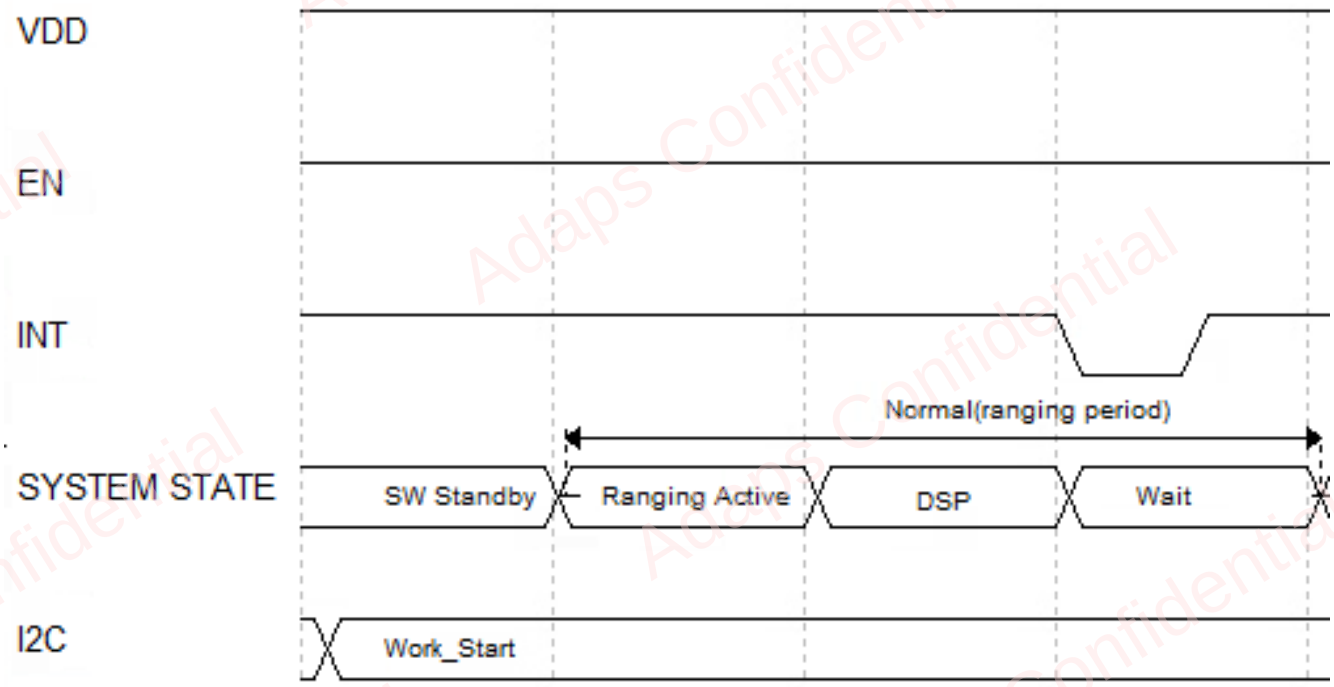


Figure 3-4 Interrupt Behavior and Timing

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4. Communication Interfaces

4.1. I²C interface

The device is controlled by an I²C bus. It supports 7bits device addressing and standard mode (100Kbps), fast mode (400Kbps) and fast mode plus mode (1Mbps). Read and Write transactions comply with the standard I²C format.

The I²C interface uses two signals: serial data line (SDA) and serial clock line (SCL). Each device connected to the bus uses a unique address and a simple master/slave relationship exists.

Both SDA and SCL lines are connected to a positive supply voltage using pull-up resistors located on the host. Lines are only actively driven low. A high condition occurs when lines are floating, and the pull-up resistors pull lines up. When no data is transmitted, both lines are high.

Clock signal (SCL) generation is performed by the master device. The master device initiates data transfer. The I²C bus on the product device has a maximum speed of 1 Mbits/s.

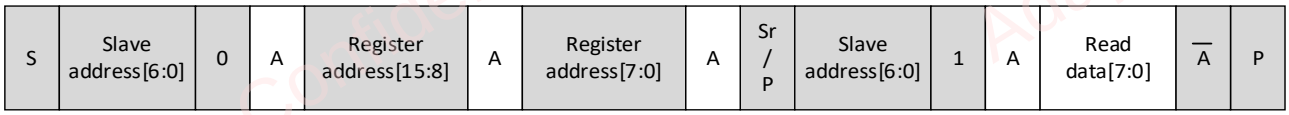
During a write/read sequence, the 2nd~3rd byte received provides a 16-bit register address, which points to one of the internal 8-bit registers.

The I²C interface supports 4 read/write operation:

- Single read
- Sequential read
- Single write
- Sequential write

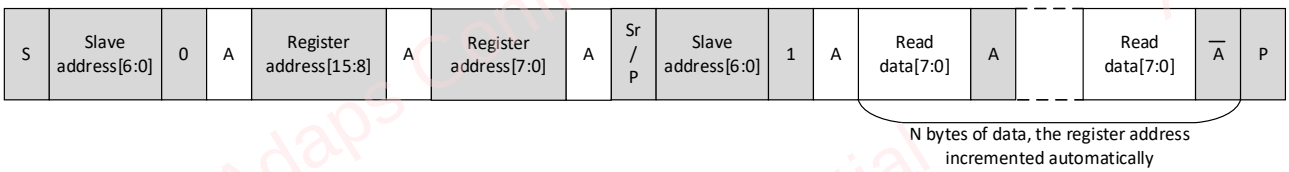
4.1.1. Single Read

The host read data from a random address. The data format is as following.



4.1.2. Sequential Read

The host reads data from the successive addresses, the data format is like the single read, the only difference is there are several read bytes before STOP asserted. The address will be incremented internally.



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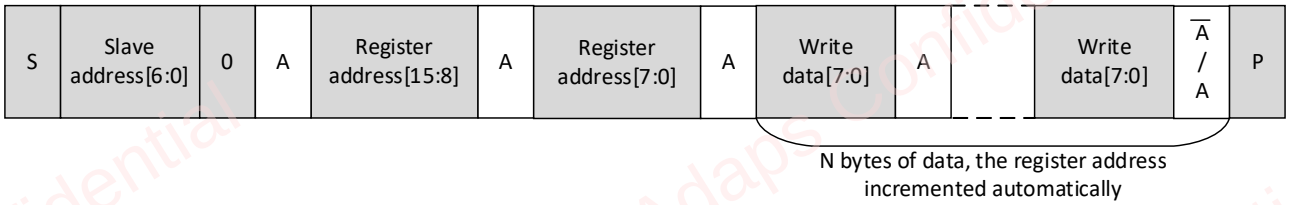
4.1.3. Single write

The host write data to a random address. The data format is as following.

S	Slave address[6:0]	0	A	Register address[15:8]	A	Register address[7:0]	A	Write data[7:0]	$\overline{A}$ / A	P

4.1.4. Sequential write

The host write data to the successive addresses, the data format is like the single write, the only difference is there are several write bytes before STOP asserted. The address will be incremented internally.



4.1.5. I²C device address

The default 7bit I²C device address is **0x19**. The address can be changed after power-up. Use the enable pin to enable only one device at a time to provide unique I²C device address.

4.2. Several chips on a single I²C bus

Several ADS6133 devices can share a single I²C bus if there are dedicated EN pad to each device.

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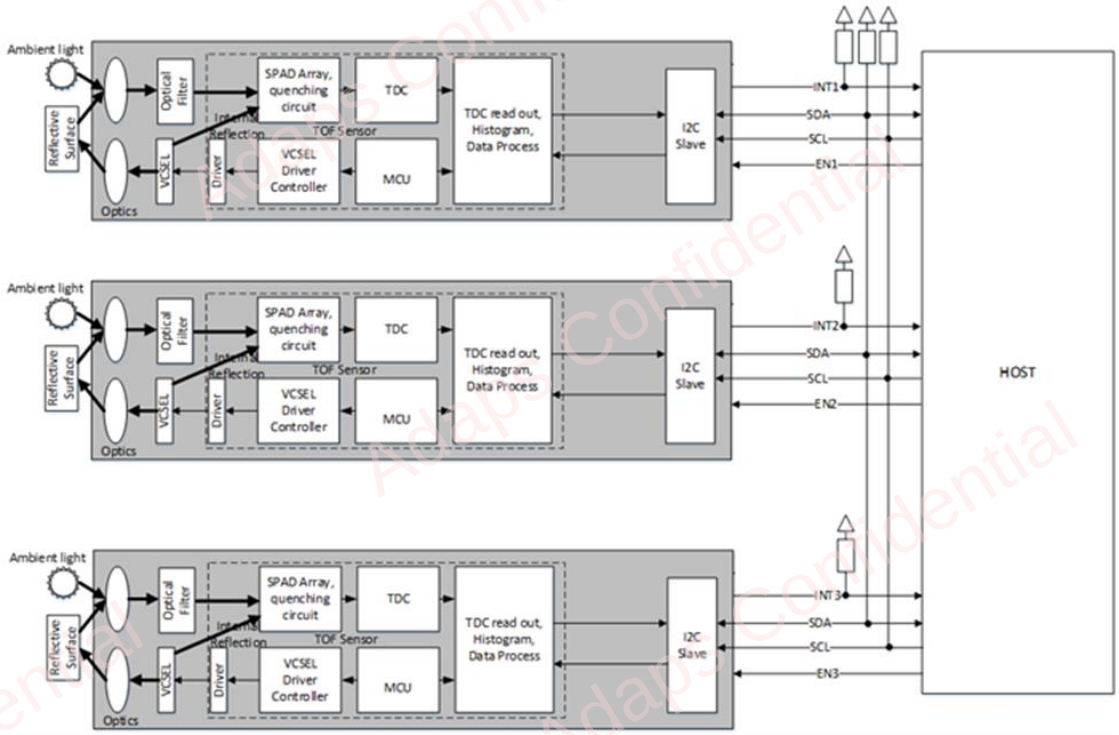


Figure 4-2 Sharing a single I²C bus for several chips

The procedure to initialize the devices to different I²C addresses is as follows:

1. Set EN1=0, EN2=0, EN3=0 (shutdown all devices),
2. Set EN1=1,
3. Download firmware patch to first ADS6133 device,
4. Reprogram I2C address for first device,
5. Set EN2=1,
6. Download firmware patch to second device,
7. Reprogram I2C address for second device,
8. Set EN3=1,
9. Download firmware patch to third device,
10. Reprogram I2C address for third device,
11. If there are further devices, repeat last three steps accordingly.

Note: I²C device address is stored in configuration register, it will be lost when power off, so must repeat the above steps when devices power on again.

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4.3. I²C Timing Specification

The I²C Timing Specification is as shown.

Figure 4-1 I²C Timing Specification

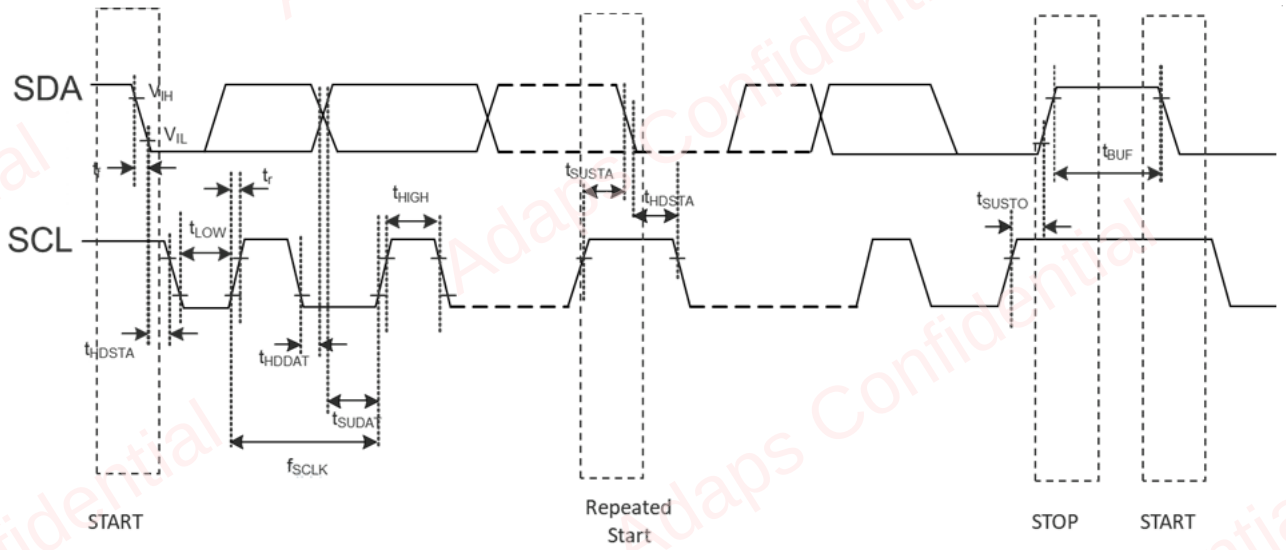


Table 4-2 I²C Timing Specification

Symbol	Parameter	Standard Mode		Fast Mode		Fast Plus Mode		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
F_{SCL}	SCL clock frequency	0	100	0	400	0	1000	KHz
$t_{HD.STA}$	Hold time after (repeated) start condition. After this period, the first clock is generated.	4.0	-	0.6	-	0.26	-	us
t_{LOW}	Low period of the SCL clock	4.7	-	1.3	-	0.5	-	us
t_{HIGH}	HIGH period of the SCL clock	4.0	-	0.6	-	0.26	-	us
$t_{SU.STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	0.26	-	us
$t_{HD.DAT}$	Data in hold time	10	-	10	-	40	-	ns
$t_{SU.DAT}$	Data in setup time	250	-	100	-	50	-	ns
t_R	Rise time of both SDA and SCL signals	-	1000	-	300	-	120	ns
t_F	Fall time of both SDA and SCL signals	-	300	-	300	-	120	ns
$t_{SU.STO}$	Set-up time for STOP condition	4.0	-	0.6	-	0.26	-	us
t_{BUF}	Bus free time between STOP and START condition	4.7	-	1.3	-	0.5	-	us

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5. Ranging Performances

5.1. Ranging Accuracy

1. **Measurement conditions for dark:**

- The full FoV (Filed of View) is covered by 24 degrees.
- Targets used are grey (17 % reflectance) and white (88 % reflectance).
- Normal voltage supply (2.8V) and temperature (23 °C).
- Indoor: No external light within the wavelength band 940nm, +/- 30nm.
- All tests are performed without cover glass.
- Range 20 mm~5000 mm.
- Typical samples used.

2. **Measurement conditions for ambient light:**

- The full FoV (Field of View) is covered by 24 degrees.
- Targets used are grey (17 % reflectance) and white (88 % reflectance).
- Normal voltage supply (2.8V) and temperature (23 °C).
- Tests are performed with 710 lux Halogen Lamp on (is equivalent to 5kLux sunlight).
- All tests are performed without cover glass.

Table 5-1 Summary of ADS6133 ranging performances.

Target reflectance (%)	Dark		Ambient light (5k Lux)	
	Range	Accuracy	Range	Accuracy
White 88 %	5-200mm	±5mm	5-200mm	±5mm
	200-5000mm	±3%	200-3000mm	±3%
Grey 17 %	5-200mm	±5mm	5-200mm	±6mm
	200-4500mm	±3%	200-3000mm	±5%

Note: IR light represents 5k sunlight equivalence, light on object only.

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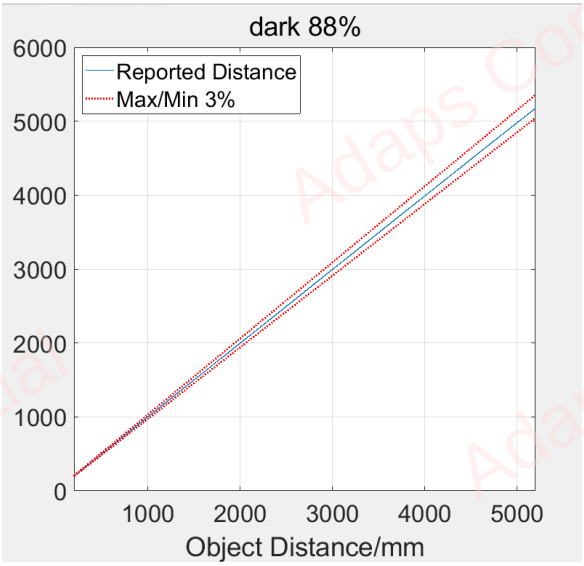


Figure 5-1 88 % White Card ranging performance

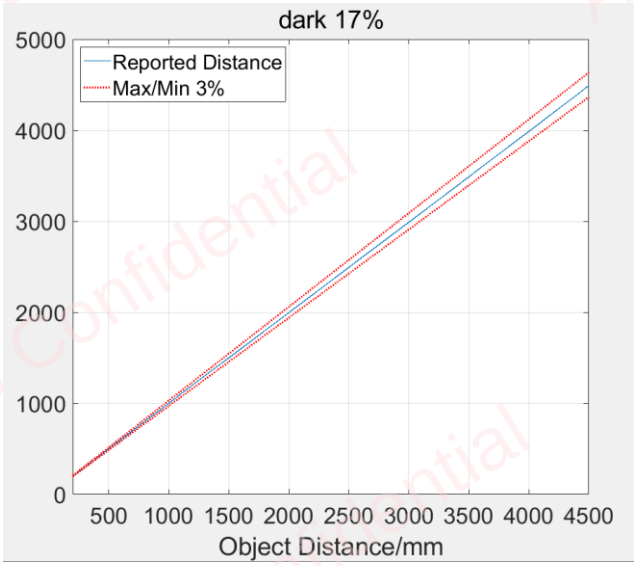


Figure 5-2 17 % Grey Card ranging performance

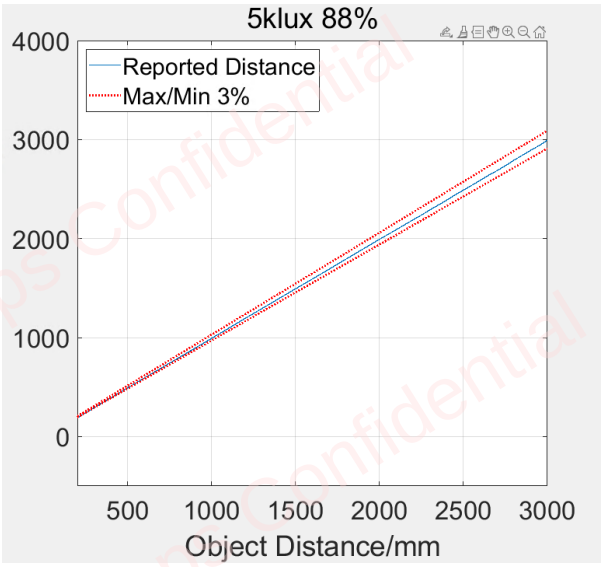


Figure 5-3 Ranging performance on an 88% white card under 5 klux ambient light

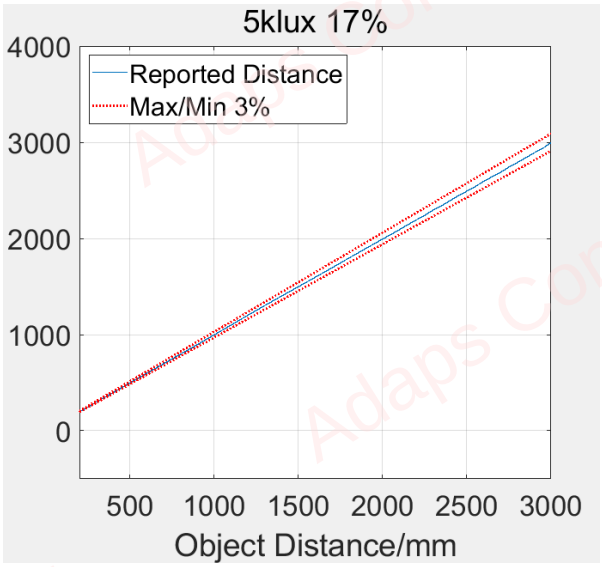


Figure 5-4 Ranging performance on an 17% gray card under 5 klux ambient light

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6. Register Description

6.1. I²C_ADDR Register (Address 0x00)

Bit	Bit Name	Default	Access	Bit Description
7	Reserved	0	RW	Reserved.
6:0	I²C_ADDR	0x19	RW	7bit I²C address

6.2. CHIP_IDH Register (Address 0x01)

Bit	Bit Name	Default	Access	Bit Description
7:0	CHIP_IDH	0x17	R	The high byte of Chip ID.

6.3. CHIP_IDL Register (Address 0x02)

Bit	Bit Name	Default	Access	Bit Description
7:0	CHIP_IDL	0x0	R	The low byte of Chip ID.

6.4. PSN_H Register (Address 0x03)

Bit	Bit Name	Default	Access	Bit Description
7:0	PSN_H	0x61	R	The High byte of the product serial number.

6.5. PSN_L Register (Address 0x04)

Bit	Bit Name	Default	Access	Bit Description
7:0	PSN_L	0x34	R	The low byte of the product serial number.

6.6. CHIP_WORK Register (Address 0x05)

Bit	Bit Name	Default	Access	Bit Description
7:3	Reserved	0x0	R/W	Reserved
2	CHIP_SRST	0x0	W	If the bit is set to 1, chip is software reset.
1	FRM_END_INT	0x0	W	After the completion of one ranging frame, this bit is set to 1 to clear the interruption.
0	WORK_START	0x0	R/W	0: standby 1: ranging

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6.7. INIT_STATE Register (Address 0x06)

Bit	Bit Name	Default	Access	Bit Description
7:6	CORE_WORK_MODE	0x3	R	00: deep sleep 01: sleep 10: reserved 11: active
5	FW_DL_DONE_RSTN_FLAG	0x0	R	0: core reset assert 1: core reset release
4	CHIP_RST_N	0x0	R	0: chip reset assert 1: chip reset release
3	GLB4_RST_N	0x0	R	0: internal reset assert 1: internal reset release
2	GLB3_RST_N	0x0	R	0: internal reset assert 1: internal reset release
1	GLB2_RST_N	0x0	R	0: internal reset assert 1: internal reset release
0	GLB_RST_N	0x0	R	0: internal reset assert 1: internal reset release

6.8. FW_CRC_VALH Register (Address 0x0F)

Bit	Bit Name	Default	Access	Bit Description
7:0	FW_CRC_VALH	0x0	R	The high byte of firmware CRC value.

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6.9. FW_CRC_VALL Register (Address 0x10)

Bit	Bit Name	Default	Access	Bit Description
7:0	FW_CRC_VALL	0x0	R	The low byte of firmware CRC value.

6.10. IO_LVL_CFG Register (Address 0x13)

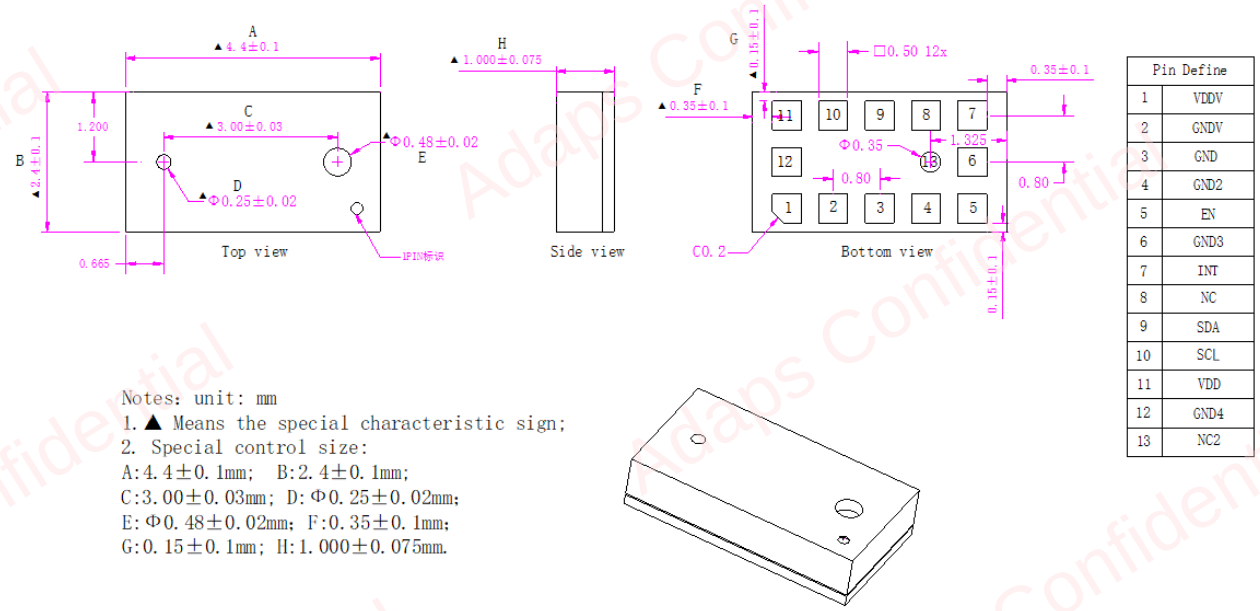
Bit	Bit Name	Default	Access	Bit Description
7:4	Reserved	0x0	R	Reserved
3	EN_SCHMG	0x0	R/W	0: initial Schmitt Trigger 1: general Schmitt Trigger
2	DEG_SEL	0x0	R/W	Reserved
1:0	IO_LVL	0x0	R/W	IO circuit supply voltage selection. Switching the IO level requires a wait of 120 μs. 0: default (1.8V) 2: 2.8-3.3V 1: 1.2V 3: 1.8V

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7. Package Information

7.1. package outline drawing

The ADS6133 module size is 4.4 mm x 2.4 mm x 1.0 mm. The package is reflowable component. The customer can integrate the ADS6133 in the system easily.



Pin Define	
1	VDDV
2	GNDV
3	GND
4	GND2
5	EN
6	GND3
7	INT
8	NC
9	SDA
10	SCL
11	VDD
12	GND4
13	NC2

Figure 7-2 Package Outline Drawing

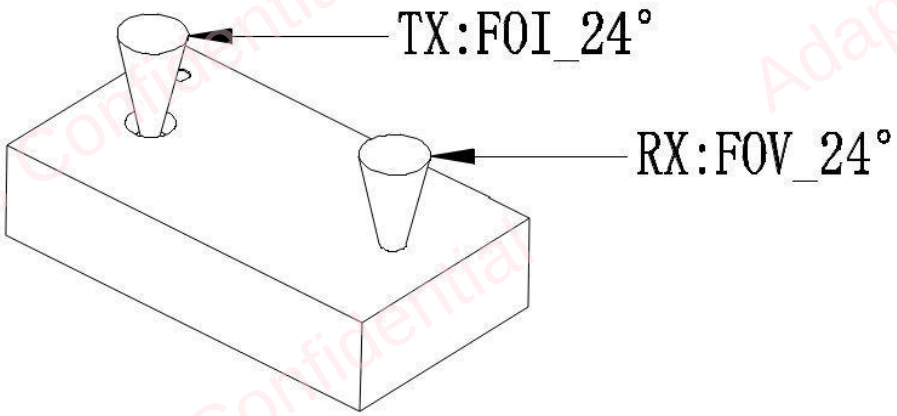


Figure 7-3 FoV/FoI Drawing

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7.2. Tape and outline drawing

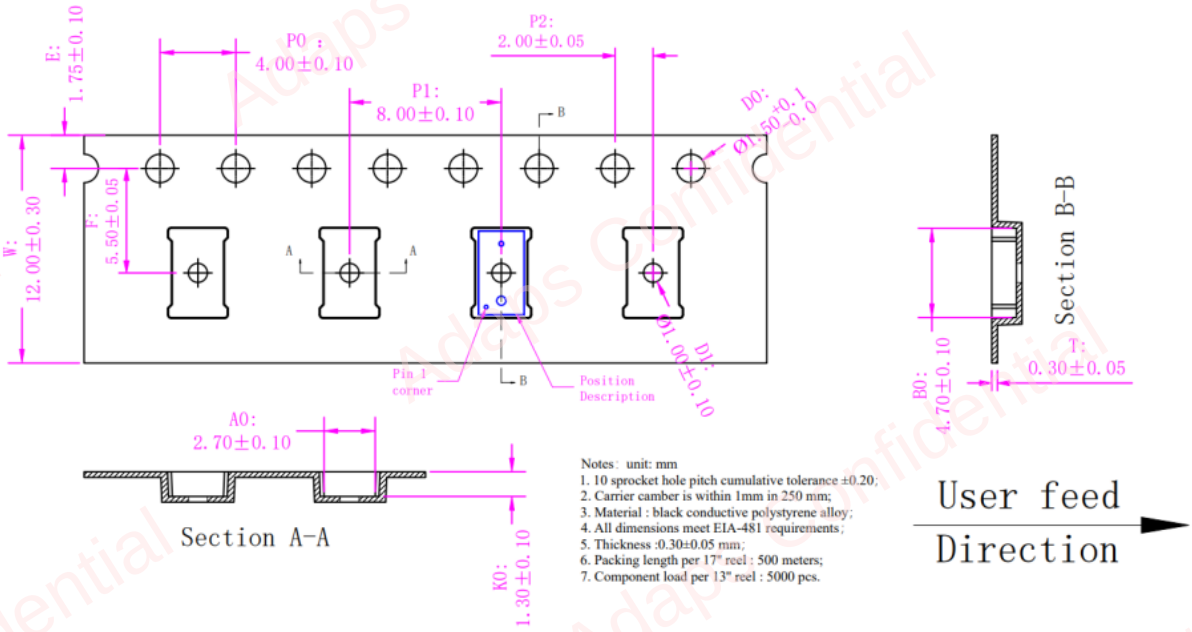


Figure 7-4 ADS6133 OLGA Tape and outline drawing

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8. Lead-free solder reflow process

Table 8-1 Reflow Soldering

Reflow Soldering	
Pre-heat	150~200°C
Pre-heat time	Max. 120 seconds
Peak temperature	Max. 260°C
Soldering time	Max. 10 seconds (Max. 3 times)

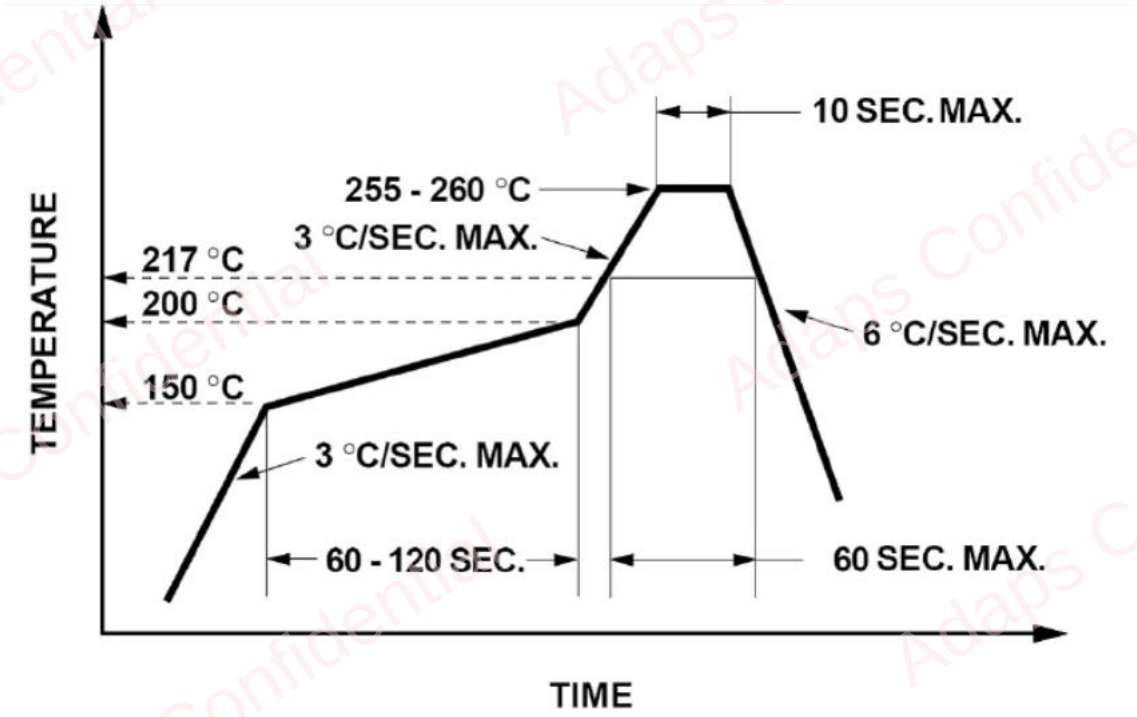


Figure 8-1 Reflow Soldering

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9. Laser Eye Safety

The ADS6133 contains a laser emitter and corresponding drive circuitry. The laser output is designed to remain within Class 1 laser safety limits under all reasonably foreseeable conditions including single faults in compliance with IEC 60825-1:2007 and IEC 60825-1:2014.

The laser output power must not be increased by any means, and no optics should be used with the intention of focusing on the laser beam.

Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.



Figure 9-1 Class 1 laser label

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10. Revision History

Table 10-1 Document revision history

Version	Date	Description
1.0	Sep.19, 2025	Initial version
1.1	Jan.30,2026	Modify ranging performance
1.2	May.29,2026	Updated hardware notes and supply voltage specifications

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