CX25601 I²C Controlled 3-A Single Cell Battery Charger for High Input Voltage

1 Features

- High-Efficiency, 1.5-MHz, Synchronous Switch-Mode Buck Charger
  - 92% Charge Efficiency at 2 A from 5-V Input
  - Optimized for USB Voltage Input (5 V)
  - Low Power Pulse Frequency Modulation (PFM) Mode for Light Load Operations
- Single Input to Support USB Input and High Voltage Adapters
  - Support 3.9-V to 13.5-V Input Voltage Range With 22-V Absolute Maximum Input Voltage Rating
  - Programmable Input Current Limit (100 mA to 3.2 A With 100-mA Resolution) to Support USB 2.0, USB 3.0 Standards and High Voltage Adaptors (IINDPM)
  - VINDPM Threshold Automatically Tracks Battery Voltage
  - Auto Detect USB SDP, DCP and Non-Standard Adaptors
- High Battery Discharge Efficiency With 19.5-mΩ Battery Discharge MOSFET
- Flexible Autonomous and I2C Mode for Optimal System Performance
- High Integration Includes All MOSFETs, Current Sensing and Loop Compensation
- 17-μA Low Battery Leakage Current
- High Accuracy
  - ±0.5% Charge Voltage Regulation
  - ±5% at 1.5-A Charge Current Regulation
  - ±10% at 0.9-A Input Current Regulation

2 Applications

- Smart Phones
- Portable Internet Devices and Accessory

3 Description

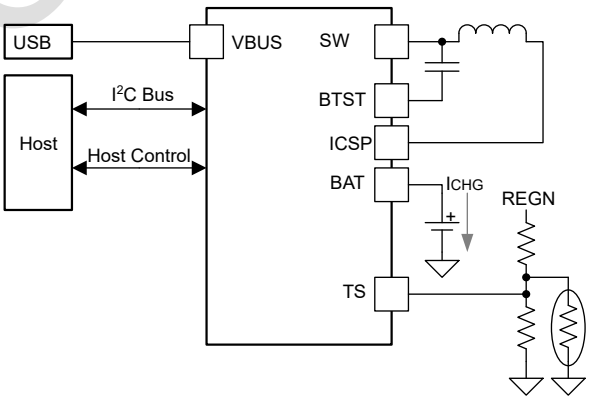
The CX25601 device is a highly-integrated 3-A switch-mode battery charge management device for single cell Li-Ion and Li-polymer battery. The low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life during discharging phase. The I²C serial interface with charging and system settings makes the device a truly flexible solution.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CX25601	WQFN (24)	4.00mm x 4.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application



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4 Revision History

DATE	REVISION	NOTES
December 2020	*	Initial release.

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5 Description (continued)

The CX25601 is a highly-integrated 3.0-A switch-mode battery charge management device for single cell Li-Ion and Li-polymer battery. It features fast charging with high input voltage support for a wide range of smart phones, tablets and portable devices. Its low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life during discharging phase. Its input voltage and current regulation deliver maximum charging power to battery. The solution is highly integrated with input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4) between ICSP and battery. It also integrates the bootstrap diode for the high-side gate drive for simplified system design. The I^2C serial interface with charging and system settings makes the device a truly flexible solution.

The device supports a wide range of input sources, including standard USB host port, USB charging port, and USB compliant high voltage adapter. The device sets default input current limit based on the built-in USB interface. To set the default input current limit, the device takes the result from detection circuit in the system, such as USB PHY device. The device is compliant with USB 2.0 and USB 3.0 power spec with input current and voltage regulation.

The device initiates and completes a charging cycle without software control. It senses the battery voltage and charges the battery in three phases: pre-conditioning, constant current and constant voltage. At the end of the charging cycle, the charger automatically terminates when the charge current is below a preset limit and the battery voltage is higher than recharge threshold. If the fully charged battery falls below the recharge threshold, the charger automatically starts another charging cycle.

The charger provides various safety features for battery charging and system operations, including battery negative temperature coefficient thermistor monitoring, charging safety timer and overvoltage and overcurrent protections. The thermal regulation reduces charge current when the junction temperature exceeds 110°C (programmable). The STAT output reports the charging status and any fault conditions. Other safety features include battery temperature sensing for charge mode, thermal regulation and thermal shutdown and input UVLO and overvoltage protection. The VBUS_GD bit indicates if a good power source is present. The INT output Immediately notifies host when fault occurs.

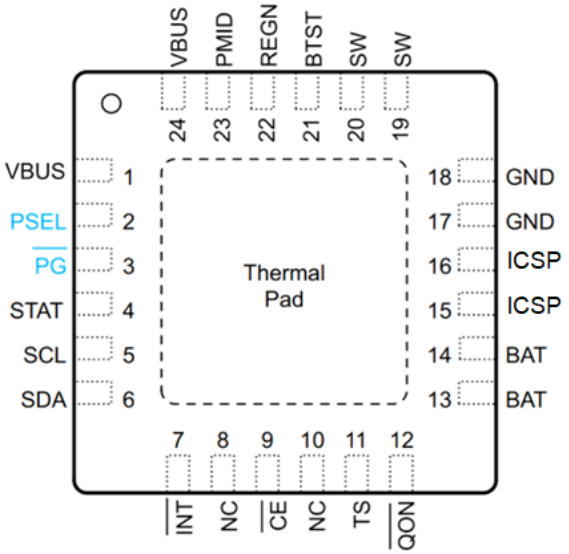
The device is available in 24-pin, 4 mm × 4 mm x 0.75 mm thin WQFN package.

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6 Pin Configuration and Function

CX25601 RTW Package
24-Pin WQFN
Top View



Pin		TYPE(1)	DESCRIPTION
NAME	CX25601		
BAT	13 14	P	Battery connection point to the positive terminal of the battery pack. The internal BATFET and current sensing is connected between ICSP and BAT. Connect a 10μF close to the BAT pin.
BTST	21	P	PWM high side driver positive supply. Internally, the BTST pin is connected to the cathode of the boost-strap diode. Connect the 0.047-μF bootstrap capacitor from SW to BTST.
$\overline{CE}$	9	DI	Charge enable pin. When this pin is driven low, battery charging is enabled.
GND	17 18	—	Ground pins.
$\overline{INT}$	7	DO	Open-drain interrupt Output. Connect the INT to a logic rail through 10-kΩ resistor. The INT pin sends an active low, 256-μs pulse to host to report charger device status and fault.
NC	8 10 12	—	No Connect. Keep the pins float.
$\overline{PG}$	3	DO	Open drain active low power good indicator. Connect to the pull up rail through 10-kΩ resistor. LOW indicates a good input source if the input voltage is between UVLO and ACOV, above SLEEP mode threshold, and current limit is above 30 mA.
PMID	23	DO	Connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Put 10μF ceramic capacitor on PMID to GND.
PSEL	2	DI	Power source selection input. Set 500 mA input current limit by pulling this pin high and set 2.4A input current limit by pulling this pin low. Once the device gets into host mode, the host can program different input current limits to IINDPM register.
REGN	22	P	LSFET driver and internal supply output. Internally, REGN is connected to the anode of the boost-strap diode. Connect a 4.7-μF (10-V rating) ceramic capacitor from REGN to GND. The capacitor should be placed close to the IC.
SCL	5	DI	I^2C interface clock. Connect SCL to the logic rail through a 10-kΩ resistor.
SDA	6	DIO	I^2C interface data. Connect SDA to the logic rail through a 10-kΩ resistor.

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STAT	4	DO	Open-drain charge status output. Connect the STAT pin to a logic rail via 10-kΩ resistor. The STAT pin indicates charger status. Collect a current limit resister and a LED from a rail to this pin. Charge in progress: LOW Charge complete or charger in SLEEP mode: HIGH Charge suspend (fault response): 1-Hz, 50% duty cycle pulses. This pin can be disabled via EN_ICHG_MON[1:0] register bits.
SW	19 20	P	Switching node output. Connected to output inductor. Connect the 0.047-μF bootstrap capacitor from SW to BTST.
ICSP	15 16	P	Converter output connection point. The internal current sensing network is connected between ICSP and BAT. Connect a 20 μF capacitor close to the ICSP pin.
TS	11	AI	Temperature qualification voltage input to support JEITA profile. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS to GND. Charge suspends when TS pin is out of range. When TS pin is not used, connect a 10-kΩ resistor from REGN to TS and connect a 10-kΩ resistor from TS to GND. It is recommended to use a 103AT-2 thermistor.
VBUS	1 24	P	Charger input. The internal n-channel reverse block MOSFET (RBFET) is connected between VBUS and PMID pins. Place a 1-uF ceramic capacitor from VBUS to GND close to device.
Thermal Pad	—	P	Thermal pad and ground reference. This pad is ground reference for the device and it is also the thermal pad used to conduct heat from the device. This pad should be tied externally to a ground plane through PCB vias under the pad.

(1) AI = Analog input, AO = Analog Output, AIO = Analog input Output, DI = Digital input, DO = Digital Output, DIO = Digital input Output, P = Power

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage Range (with respect to GND)	VBUS (converter not switching)(2)	–2	22	V
Voltage Range (with respect to GND)	BTST, PMID (converter not switching)(2)	–0.3	22	V
Voltage Range (with respect to GND)	SW	–2	16	V
Voltage Range (with respect to GND)	BTST to SW	–0.3	7	V
Voltage Range (with respect to GND)	PSEL	–0.3	7	V
Voltage Range (with respect to GND)	REGN, TS, $\overline{CE}$, $\overline{PG}$, BAT, ICSP (converter not switching)	–0.3	7	V
Output Sink Current	STAT		6	mA
Voltage Range (with respect to GND)	SDA, SCL, $\overline{INT}$, STAT	–0.3	7	V
Voltage Range (with respect to GND)	PGND to GND (QFN package only)	–0.3	0.3	V
Output Sink Current	$\overline{INT}$		6	mA
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under Absolute maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

(2) VBUS is specified up to 22 V for a maximum of one hour at room temperature

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{BUS}	Input voltage	3.9		13.5(1)	V
I_{in}	Input current (VBUS)			3.25	A

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I_{SWOP}	Output current (SW)			3.25	A
V_{BATOP}	Battery voltage			4.624	V
I_{BATOP}	Fast charging current			3.0	A
I_{BATOP}	Discharging current (continuous)			6	A
T_A	Operating ambient temperature	–40		85	°C

（1）The inherent switching noise voltage spikes should not exceed the absolute maximum voltage rating on either the BTST or SW pins. A tight layout minimizes switching noise.

7.4 Thermal information

THERMAL METRIC		CX25601(D) RTW (WQFN) 24 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	12	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.6	°C/W

7.5 Electrical Characteristics

$V_{VAC_UVLOZ} < V_{VBUS} < V_{VAC_OV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
I_{BAT}	Battery discharge current (BAT, SW, ICSP) in buck mode	V_{BAT} = 4.5 V, $V_{BUS} < V_{AC-UVLOZ}$, leakage between BAT and VBUS, T_J< 85°C			5	μA
I_{BAT}	Battery discharge current (BAT) in buck mode	V_{BAT} = 4.5 V, HIZ Mode and OVPFET_DIS = 1 or No VBUS, I2C disabled, BATFET Disabled. T_J < 85°C		17	33	μA
I_{BAT}	Battery discharge current (BAT, SW, ICSP)	V_{BAT} = 4.5 V, HIZ Mode and OVPFET_DIS = 1 or No VBUS, I2C Disabled, BATFET Enabled. T_J < 85°C		58	85	μA
I_{VBUS_HIZ}	Input supply current (VBUS) in buck mode	V_{VBUS} = 5 V, High-Z Mode and OVPFET_DIS = 1, No battery		37	50	μA
I_{VBUS_HIZ}	Input supply current (VBUS) in buck mode	V_{VBUS} = 12 V, High-Z Mode and OVPFET_DIS = 1, No battery		68	90	μA
I_{VBUS}	Input supply current (VBUS) in buck mode	V_{VBUS} = 12 V, $V_{VBUS} > V_{VBAT}$, converter not switching		1.5	3	mA
I_{VBUS}	Input supply current (VBUS) in buck mode	$V_{VBUS} >$ VUVLO, $V_{VBUS} > V_{VBAT}$, converter switching, VBAT = 3.8V, IICSP = 0A		3		mA

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VBUS AND BAT PIN POWER-UP						
V_{BUS_OP}	VBUS operating range	V_{VBUS} rising	3.9		13.5	V
V_{VAC_UVLOZ}	VBUS for active I²C, no battery Sense VBUS pin voltage	V_{VBUS} rising		3.3	3.6	V
$V_{VAC_UVLOZ_HYS}$	I²C active hysteresis	VBUS falling from above V_{VAC_UVLOZ}		300		mV
$V_{VAC_PRESENT}$	One of the conditions to turn on REGN	V_{VBUS} rising		3.65	3.9	V
$V_{VAC_PRESENT_HYS}$	One of the conditions to turn on REGN	V_{VBUS} falling		500		mV
V_{SLEEP}	Sleep mode falling threshold	(V_{VBUS}–V_{VBAT}), $V_{BUSMIN_FALL} \le V_{BAT} \le V_{REG}$, VBUS falling	15	60	110	mV
V_{SLEEPZ}	Sleep mode rising threshold	(V_{VBUS}–V_{VBAT}), $V_{BUSMIN_FALL} \le V_{BAT} \le V_{REG}$, VBUS rising	115	220	340	mV
$V_{VAC_OV_RISE}$	VBUS 6.5-V Overvoltage rising threshold	VBUS rising; OVP (REG06[7:6]) = '01'	6.1	6.4	6.7	V
$V_{VAC_OV_RISE}$	VBUS 10.5-V Overvoltage rising threshold	VBUS rising, OVP (REG06[7:6]) = '10'	10.35	10.9	11.5	V
$V_{VAC_OV_RISE}$	VBUS 14-V Overvoltage rising threshold	VBUS rising, OVP (REG06[7:6]) = '11'	13.5	14.2	14.85	V
$V_{VAC_OV_HYS}$	VBUS 6.5-V Overvoltage hysteresis	VBUS falling, OVP (REG06[7:6]) = '01'		320		mV
$V_{VAC_OV_HYS}$	VBUS 10.5-V Overvoltage hysteresis	VBUS falling, OVP (REG06[7:6]) = '10'		250		mV
$V_{VAC_OV_HYS}$	VBUS 14-V Overvoltage hysteresis	VBUS falling, OVP (REG06[7:6]) = '11'		300		mV
V_{BAT_UVLOZ}	BAT for active I²C, no adapter	V_{BAT} rising	2.5			V
$V_{BAT_DPL_FALL}$	Battery Depletion Threshold	V_{BAT} falling	2.2		2.6	V
$V_{BAT_DPL_RISE}$	Battery Depletion Threshold	V_{BAT} rising	2.35		2.8	V
$V_{BAT_DPL_HYST}$	Battery Depletion rising hysteresis	V_{BAT} rising		180		mV
V_{BUSMIN_FALL}	Bad adapter detection falling threshold	V_{BUS} falling	3.75	3.9	4.0	V
V_{BUSMIN_HYST}	Bad adapter detection hysteresis			80		mV
I_{BADSRC}	Bad adapter detection current source	Sink current from VBUS to GND		30		mA
POWER-PATH						
$R_{ON(RBFET)}$	Top reverse blocking MOSFET on-resistance between VBUS and PMID - Q1	-40°C≤ T_A ≤ 125°C		45		mΩ
$R_{ON(HSFET)}$	Top switching MOSFET onresistance between PMID and SW - Q2	V_{REGN} = 5 V , -40°C≤ T_A ≤ 125°C		62		mΩ

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$R_{ON(LSFET)}$	Bottom switching MOSFET onresistance between SW and GND - Q3	V_{REGN} = 5 V , -40°C≤ T_A ≤ 125°C		71		mΩ
$R_{ON(BAT-ICSP)}$	ICSP-BAT MOSFET on-resistance	QFN package, Measured from BAT to ICSP, V_{BAT} = 4.2V, T_J = 25°C		19.5	24	mΩ
$R_{ON(BAT-ICSP)}$	ICSP-BAT MOSFET on-resistance	QFN package, Measured from BAT to ICSP, V_{BAT} = 4.2V, T_J = –40~125°C		19.5	30	mΩ
BATTERY CHARGER						
V_{BATREG_RANGE}	Charge voltage program range		3.856		4.624	V
V_{BATREG_STEP}	Charge voltage step			32		mV
V_{BATREG}	Charge voltage setting	VREG (REG04[7:3]) = 4.208 V (01011), V, –40 ≤ T_J ≤ 85°C	4.187	4.208	4.229	V
		VREG (REG04[7:3]) = 4.352 V (01111), V, –40 ≤ T_J ≤ 85°C	4.330	4.352	4.374	V
V_{BATREG_ACC}	Charge voltage setting accuracy	V_{BAT} = 4.208 V or V_{BAT} = 4.352 V, –40 ≤ T_J ≤ 85°C	–0.5%		0.5%	
$I_{CHG_REG_RANGE}$	Charge current regulation range		0		3000	mA
$I_{CHG_REG_STEP}$	Charge current regulation step			60		mA
I_{CHG_REG}	Charge current regulation setting	I_{CHG} = 240 mA, V_{VBAT} = 3.1V or V_{VBAT} = 3.8 V	0.216	0.24	0.264	A
$I_{CHG_REG_ACC}$	Charge current regulation accuracy	I_{CHG} = 240 mA, V_{VBAT} = 3.1 V or V_{VBAT} = 3.8 V	–10%		10%	
I_{CHG_REG}	Charge current regulation setting	I_{CHG} = 720 mA, V_{VBAT} = 3.1 V or V_{VBAT} = 3.8 V	0.685	0.720	0.755	A
I_{CHG_REG}	Charge current regulation accuracy	I_{CHG_REG} = 720 mA, V_{BAT} = 3.1 V or V_{BAT} = 3.8 V	-5%		5%	
I_{CHG_REG}	Charge current regulation setting	I_{CHG} = 1.38 A, V_{VBAT} = 3.1 V or V_{VBAT} = 3.8 V	1.311	1.380	1.449	A
$I_{CHG_REG_ACC}$	Charge current regulation accuracy	I_{CHG} = 720 mA or I_{CHG} = 1.38 A, V_{VBAT} = 3.1 V or V_{VBAT} = 3.8 V	–5%		5%	
$V_{BATLOWV_FALL}$	Battery LOWV falling threshold	I_{CHG} = 240 mA	2.7	2.8	2.9	V
$V_{BATLOWV_RISE}$	Battery LOWV rising threshold	Pre-charge to fast charge	3.0	3.12	3.24	V
I_{PRECHG}	Precharge current regulation	IPRECHG[3:0] = '0010' = 180 mA	153	171	189	mA
I_{PRECHG_ACC}	Precharge current regulation accuracy	IPRECHG[3:0] = '0010' = 180 mA	–15		5	%
I_{TERM}	Termination current regulation	I_{CHG} > 780 mA, ITERM[3:0] = '0010' = 180 mA, V_{VBAT} = 4.208 V	135	180	225	mA
I_{TERM_ACC}	Termination current regulation accuracy	I_{CHG} > 780 mA, , ITERM[3:0] = '0010' = 180 mA, V_{VBAT} = 4.208 V	-25%		25%	
V_{SHORT}	Battery short voltage	V_{VBAT} falling	1.85	2	2.15	V
V_{SHORTZ}	Battery short voltage	V_{VBAT} rising	2.15	2.25	2.35	V
I_{SHORT}	Battery short current	V_{VBAT} < V_{SHORTZ}		100		mA
V_{RECHG}	Recharge Threshold below V_{BAT_REG}	V_{BAT} falling, REG04[0] = 0		100		mV

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V_{RECHG}	Recharge Threshold below V_{BAT_REG}	V_{BAT} falling, REG04[0] = 1		200		mV
INPUT VOLTAGE AND CURRENT REGULATION						
V_{DPM_VBAT}	Input voltage regulation limit tracking VBAT	VDPM_VBAT_TRACK = 300mV, VBAT = 4.0V	4.171	4.3	4.43	V
$V_{DPM_VBAT_ACC}$	Input voltage regulation accuracy tracking VBAT		–3%		3%	
I_{INDPM}	USB input current regulation limit	V_{VBUS} = 5 V, current pulled from SW, I_{INDPM} (REG[4:0] = 00100) = 500 mA, –40 ≤ T_J ≤ 85°C	450		500	mA
		V_{VBUS} = 5 V, current pulled from SW, IINDPM (REG[4:0] = 01000) = 900 mA, –40 ≤ T_J ≤ 85°C	750		900	mA
		V_{VBUS} = 5 V, current pulled from SW, IINDPM (REG[4:0] = 01110) = 1.5 A, –40 ≤ T_J ≤ 85°C	1.3		1.5	A
BAT PIN OVERVOLTAGE PROTECTION						
V_{BATOVP_RISE}	Battery overvoltage threshold	V_{BAT} rising, as percentage of V_{BAT_REG}	103	104	105	%
V_{BATOVP_FALL}	Battery overvoltage threshold	V_{BAT} falling, as percentage of V_{BAT_REG}	101	102	103	%
THERMAL REGULATION AND THERMAL SHUTDOWN						
$T_{JUNCTION_REG}$	Junction Temperature Regulation Threshold	Temperature Increasing, TREG (REG05[1] = 1) = 110℃		110		°C
$T_{JUNCTION_REG}$	Junction Temperature Regulation Threshold	Temperature Increasing, TREG (REG05[1] = 0) = 90℃		90		°C
T_{SHUT}	Thermal Shutdown Rising Temperature	Temperature Increasing		160		°C
T_{SHUT_HYST}	Thermal Shutdown Hysteresis			30		°C
JEITA Thermistor Comparator (BUCK MODE)						
V_{T1}	T1 (0°C) threshold, Charge suspended T1 below this temperature.	Charger suspends charge. As Percentage to V_{REGN}	72.4%	73.3%	74.2%	
V_{T1}	Falling	As Percentage to V_{REGN}	69%	71.5%	74%	
V_{T2}	T2 (10°C) threshold, Charge back to I_{CHG}/2 and 4.2 V below this temperature	As percentage of V_{REGN}	67.2%	68%	69%	
V_{T2}	Falling	As Percentage to V_{REGN}	66%	66.8%	67.7%	
V_{T3}	T3 (45°C) threshold, charge back to ICHG and 4.05V above this temperature.	Charger suspends charge. As Percentage to V_{REGN}	43.8%	44.7%	45.8%	
V_{T3}	Falling	As Percentage to V_{REGN}	45.1%	45.7%	46.2%	
V_{T5}	T5 (60°C) threshold, charge suspended above this temperature.	As Percentage to V_{REGN}	33.7%	34.2%	35.1%	
V_{T5}	Falling	As Percentage to V_{REGN}	34.5%	35.3%	36.2%	

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CHARGE OVERCURRENT COMPARATOR (CYCLE-BY-CYCLE)						
I_{HSFET_OCP}	HSFET cycle-by-cycle overcurrent threshold		5.2		8.0	A
I_{BATFET_OCP}	Battery over load threshold		6.0			A
CHARGE UNDER-CURRENT COMPARATOR (CYCLE-BY-CYCLE)						
V_{LSFET_UCP}	LSFET under-current falling threshold	From sync mode to non-sync mode			160	mA
REGN LDO						
V_{REGN}	REGN LDO output voltage	V_{VBUS} = 9V, I_{REGN} = 40mA	5.6	6	6.55	V
V_{REGN}	REGN LDO output voltage	V_{VBUS} = 5V, I_{REGN} = 20mA	4.6	4.7	4.8	V
LOGIC I/O PIN CHARACTERISTICS $\overline{CE}$ PSEL, ($\overline{PG}$, STAT, $\overline{INT}$))						
V_{ILO}	Input low threshold				0.4	V
V_{IH}	Input high threshold		1.3			V
I_{BIAS}	High-level leakage current	Pull up rail 1.8 V			1	μA
V_{OL}	Low-level output voltage				0.4	V
I2C Interface (SCL, SDA)						
V_{IH}	Input high threshold level	Pull up rail 1.8 V	1.3			V
V_{IL}	Input t low threshold level	Pull up rail 1.8 V			0.4	V
V_{OL}	Output low threshold level	Sink current = 5 mA,			0.4	V

(1)Specified by design. Not production tested.

7.6 Timing Requirements

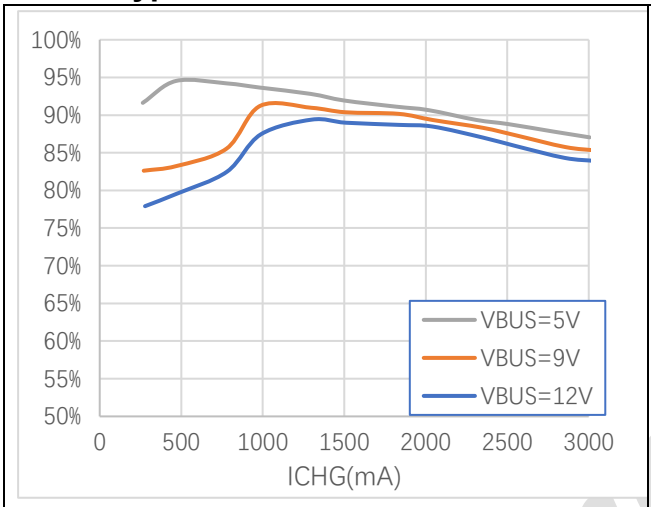
			MIN	NOM	MAX	UNIT
VBUS/BAT POWER UP						
t_{ACOV}	VBUS OVP reaction time	VBUS rising above ACOV threshold to turn off Q2		200		ns
t_{BADSRC}	Bad adapter detection duration			30		ms
BATTERY CHARGER						
t_{TERM_DGL}	Deglitch time for charge termination			24		ms
t_{RECHG_DGL}	Deglitch time for recharge			250		ms
$t_{BATOVLD_DGL}$	Battery over-current deglitch time to turn off Q4			100		μs
t_{BATOVP}	Battery over-voltage deglitch time to disable charge			1		μs
t_{SAFETY}	Typical Charge Safety Timer Range	CHG_TIMER = 1	8	10	12	hr
t_{TOP_OFF}	Typical Top-Off Timer Range	TOP_OFF_TIMER[1:0] = 10 (30 min)	24	30	36	min

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DIGITAL CLOCK AND WATCHDOG TIMER						
t_{WDT}	REG05[4]=1	REGN LDO disabled		40		s
f_{LPDIG}	Digital Low Power Clock	REGN LDO disabled		30		kHz
f_{DIG}	Digital Clock	REGN LDO enabled		500		kHz
f_{SCL}	SCL clock frequency				400	kHz

7.7 Typical Characteristics



Fsw=1.5MHz VBAT=3.8V

Figure 1. Charge Efficiency vs. Charge Current

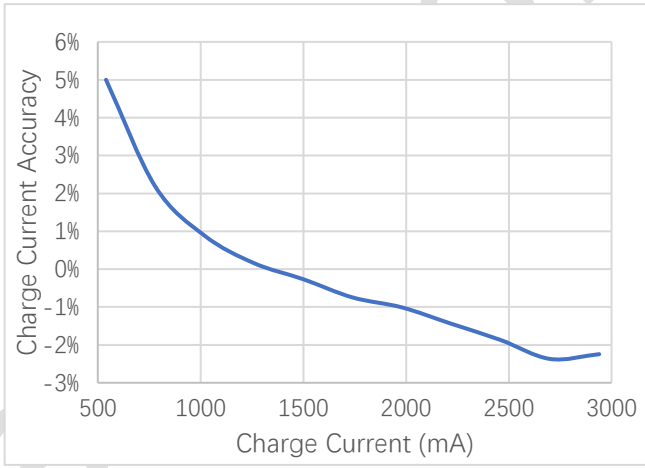


Figure 4. Charge Current Accuracy

8 Detailed Description

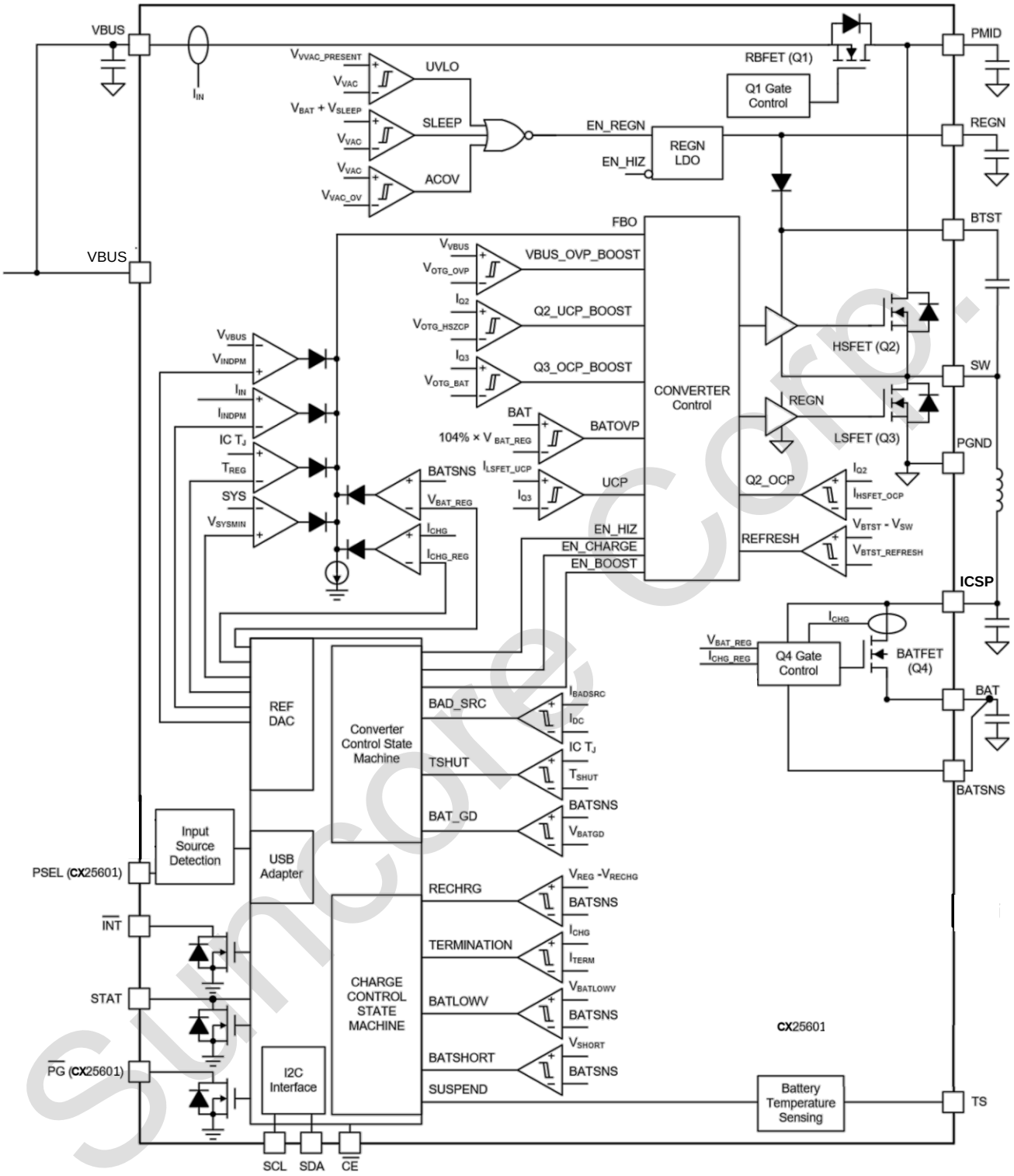
8.1 Overview

The CX25601 device is a highly integrated 3.0-A switch-mode battery charger for single cell Li-Ion and Li-polymer battery. It includes the input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4), and bootstrap diode for the high-side gate drive.

8.2 Functional Block Diagram

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8.3 Feature Description

8.3.1 Power-On-Reset (POR)

The device powers internal bias circuits from the higher voltage of VBUS and BAT. When VBUS rises above V_{VBUS_UVLOZ} or BAT rises above V_{BAT_UVLOZ}, the sleep comparator, battery depletion comparator and BATFET driver are active. I²C interface is ready for communication and all the registers are reset to default value. The host can access all the registers after POR.

8.3.2 Power Up from Input Source

When an input source is plugged in, the device checks the input source voltage to turn on REGN LDO and all the bias circuits. It detects and sets the input current limit before the buck converter is started. The power up sequence from input source is as listed:

1. Power Up REGN LDO
2. Poor Source Qualification
3. Input Source Type Detection is based on or PSEL to set default input current limit (IINDPM) register or input source type.
4. Input Voltage Limit Threshold Setting (VINDPM threshold)
5. Converter Power-up

8.3.2.1 Power Up REGN Regulation

The REGN LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive. The REGN also provides bias rail to TS external resistors. The pull-up rail of STAT can be connected to REGN as well. The REGN is enabled when all the below conditions are valid:

- V_{VBUS} above $V_{VAC_PRESENT}$
- V_{VBUS} above V_{BAT} + V_{SLEEPZ} in buck mode
- After 220-ms delay is completed

If any one of the above conditions is not valid, the device is in high impedance mode (HIZ) with REGN LDO off. The device draws less than I_{VBUS_HIZ} from VBUS during HIZ state.

8.3.2.2 Poor Source Qualification

After REGN LDO powers up, the device confirms the current capability of the input source. The input source must meet both of the following requirements in order to start the buck converter.

- VBUS voltage below V_{VAC_OV}
- VBUS voltage above $V_{VBUSMIN}$ when pulling I_{BADSRC} (typical 30 mA)

Once the input source passes all the conditions above, the status register bit VBUS_GD is set high and the $\overline{INT}$ pin is pulsed to signal to the host. If the device fails the poor source detection, it repeats poor source qualification every 2 seconds.

8.3.2.3 Input Source Type Detection

After the VBUS_GD bit is set and REGN LDO is powered, the device runs input source detection through the PSEL pin. The CX25601 sets input current limit through PSEL pins.

After input source type detection is completed, an INT pulse is asserted to the host. In addition, the following registers and pin are changed:

1. Input Current Limit (IINDPM) register is changed to set current limit
2. PG_STAT bit is set
3. VBUS_STAT bit is updated to indicate USB or other input source

The host can over-write IINDPM register to change the input current limit if needed. The charger input current is always limited by the IINDPM register.

8.3.2.3.1 PSEL Pins Sets Input Current Limit in CX25601

The CX25601 has PSEL pin for input current limit setting to interface with USB PHY. It directly takes the USB PHY device output to decide whether the input is USB host or charging port. When the device operates in host-

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control mode, the host needs to IINDET_EN bit to read the PSEL value and update the IINDPM register. When the device is in default mode, PSEL value updates IINDPM in real time.

Table 3. Input Current Limit Setting from PSEL

Input Detection	PSEL Pin	Input Current Limit (ILIM)	VBUS_STAT
USB SDP	High	500mA	001
Adapter	Low	2.4A	011

8.3.2.4 Input Voltage Limit Threshold Setting (VINDPM Threshold)

The device supports wide range of input voltage limit (3.9 V – 5.4V) for USB.

The device supports dynamic VINDPM settings which tracks the battery voltage. The actual input voltage limit will be VBAT + VDPM_BAT_TRACK offset.

8.3.2.5 Converter Power-Up

After the input current limit is set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, BATFET turns off. Otherwise, BATFET stays on to charge the battery.

As a battery charger, the device deploys a highly efficient 1.5 MHz step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

8.3.3 Host Mode and Standalone Power Management

8.3.3.1 Host Mode and Default Mode in CX25601

The CX25601 is a host-controlled charger, but it can operate in default mode without host management. in default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode. When the charger is in default mode, WATCHDOG_FAULT bit is HIGH. When the charger is in host mode, WATCHDOG_FAULT bit is LOW.

After power-on-reset, the device starts in default mode with watchdog timer expired, or default mode. All the registers are in the default settings. During default mode, any change on PSEL pin will make real time IINDPM register changes.

In default mode, the device keeps charging the battery with default 10-hour fast charging safety timer. At the end of the 10-hour, the charging is stopped.

Writing a 1 to the WD_RST bit transitions the charger from default mode to host mode. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires (WATCHDOG_FAULT bit is set), or disable watchdog timer by setting WATCHDOG bits = 00.

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When the watchdog timer expires (WATCHDOG_FAULT bit = 1), the device returns to default mode and all registers are reset to default values except IINDPM, BATFET_DLY, and BATFET_DIS bits.

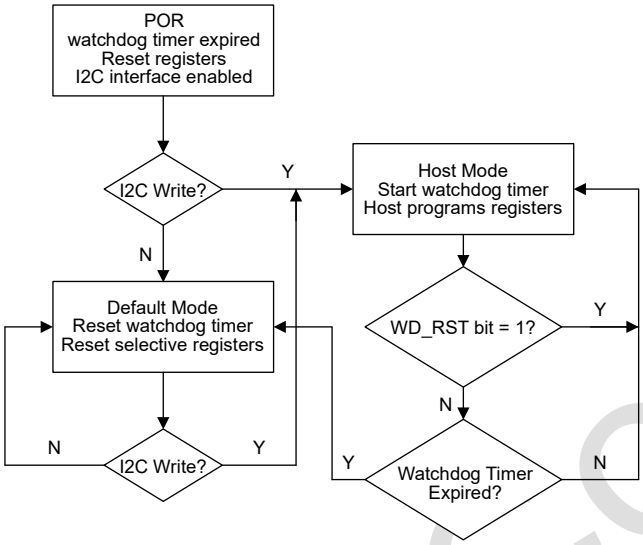


Figure 5. Watchdog Timer Flow Chart

8.3.4 Battery Charging Management

The device charges 1-cell Li-Ion battery with up to 3.0-A charge current for high-capacity tablet battery. The 19.5mΩ BATFET improves charging efficiency and minimize the voltage drop during discharging.

8.3.4.1 Autonomous Charging Cycle

With battery charging is enabled (CHG_CONFIG bit = 1 and CE pin is LOW), the device autonomously completes a charging cycle without host involvement. The device default charging parameters are listed in Table 2. The host can always control the charging operations and optimize the charging parameters by writing to the corresponding registers through I^2C.

Table 2. Charging Parameter Default Setting

Default Mode	CX25601
Charging Voltage	4.208V
Charging Current	2.048A
Pre-charge Current	180mA
Termination Current	180mA
Temperature Profile	JEITA
Safety Timer	10 hours

A new charge cycle starts when the following conditions are valid:

- Converter starts
- Battery charging is enabled (CHG_CONFIG bit = 1 and ICHG register is not 0 mA and $\overline{CE}$ is low)
- No thermistor fault on TS
- No safety timer fault
- BATFET is not forced to turn off (BATFET_DIS bit = 0)

The charger device automatically terminates the charging cycle when the charging current is below termination threshold, battery voltage is above recharge threshold, and device not is in DPM mode or thermal regulation. When a fully charged battery is discharged below recharge threshold (selectable through VRECHG bit), the

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device automatically starts a new charging cycle. After the charge is done, toggle $\overline{CE}$ pin or CHG_CONFIG bit can initiate a new charging cycle.

The STAT output indicates the charging status: charging (LOW), charging complete or charge disable (HIGH) or charging fault (Blinking). The STAT output can be disabled by setting EN_ICHG_MON bits = 11. in addition, the status register (CHRG_STAT) indicates the different charging phases: 00-charging disable, 01-precharge, 10-fast charge (constant current) and constant voltage mode, 11-charging done. Once a charging cycle is completed, an INT is asserted to notify the host.

8.3.4.2 Battery Charging Profile

The device charges the battery in five phases: battery short, preconditioning, constant current, constant voltage and top-off trickle charging (optional). At the beginning of a charging cycle, the device checks the battery voltage and regulates current and voltage accordingly.

Table 3. Charging Current Setting

V_{BAT}	Charging Current	Register Default Setting	CHRG_STAT
< 2.2V	I_{SHORT}	100mA	01
2.2V to 3V	I_{PRECHG}	180mA	01
> 3V	I_{CHG}	2.048A	10

If the charger device is in DPM regulation or thermal regulation during charging, the actual charging current will be less than the programmed value. in this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate.

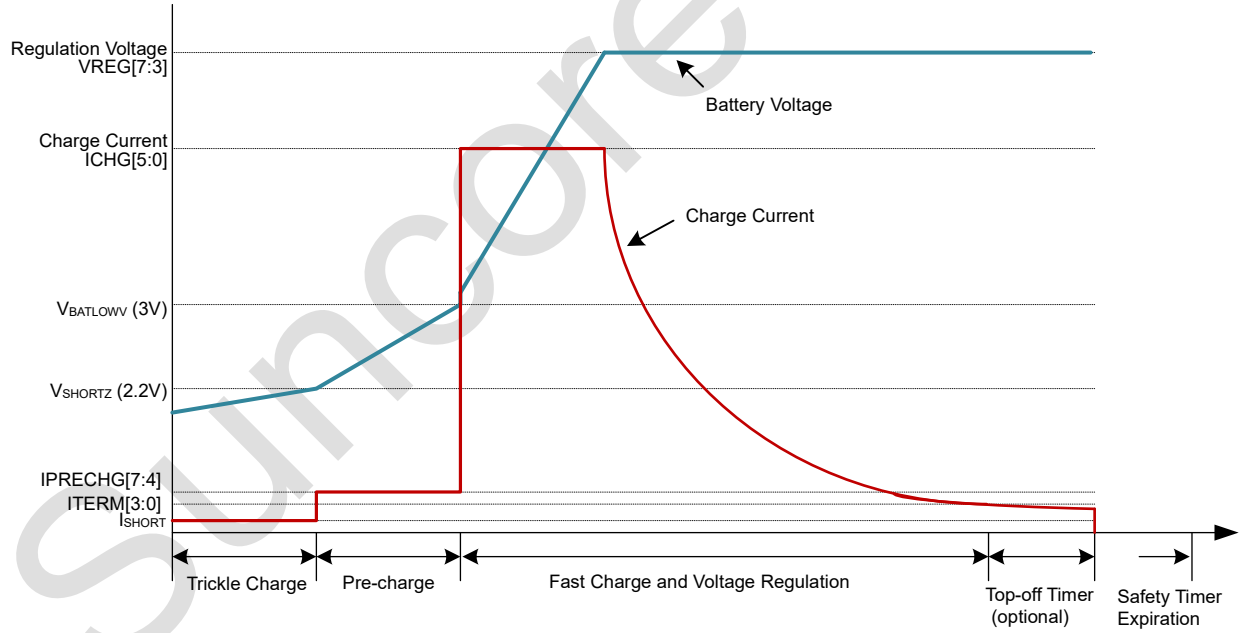


Figure 6. Battery Charging Profile

8.3.4.3 Charging Termination

The device terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below termination current. After the charging cycle is completed, the BATFET turns off.

When termination occurs, the status register CHRG_STAT is set to 11, and an INT pulse is asserted to the host. Termination is temporarily disabled when the charger device is in input current, voltage or thermal regulation. Termination can be disabled by writing 0 to EN_TERM bit prior to charge termination.

At low termination currents (25 mA-50 mA), due to the comparator offset, the actual termination current may be 10 mA-20 mA higher than the termination target.

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8.3.4.4 Thermistor Qualification

The charger device provides a single thermistor input for battery temperature monitor.

8.3.4.5 JEITA Guideline Compliance During Charging Mode

To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges.

To initiate a charge cycle, the voltage on TS pin must be within the VT1 to VT5 thresholds. If TS voltage exceeds the T1-T5 range, the controller suspends charging and waits until the battery temperature is within the T1 to T5 range.

At cool temperature (T1-T2), JEITA recommends the charge current to be reduced to half of the charge current or lower. At warm temperature (T3-T5), JEITA recommends charge voltage less than 4.1 V.

The charger provides flexible voltage/current settings beyond the JEITA requirement. The voltage setting at warm temperature (T3-T5) can be VREG or 4.1V (configured by JEITA_VSET). The current setting at cool temperature (T1-T2) can be further reduced to 20% of fast charge current (JEITA_ISET).

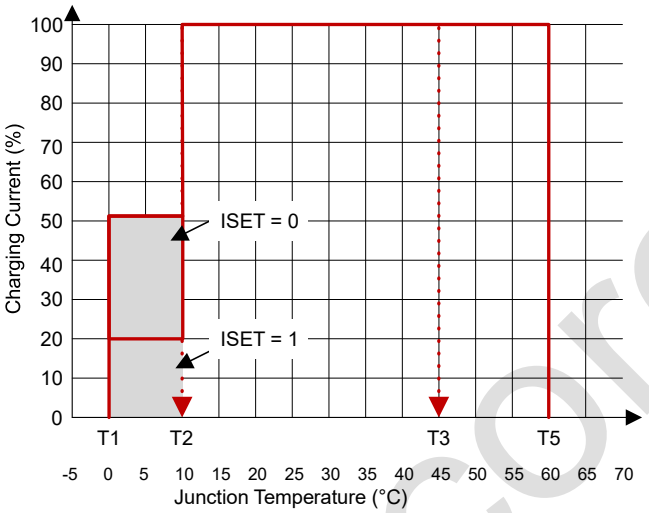


Figure 7. JEITA Profile: Charging Current

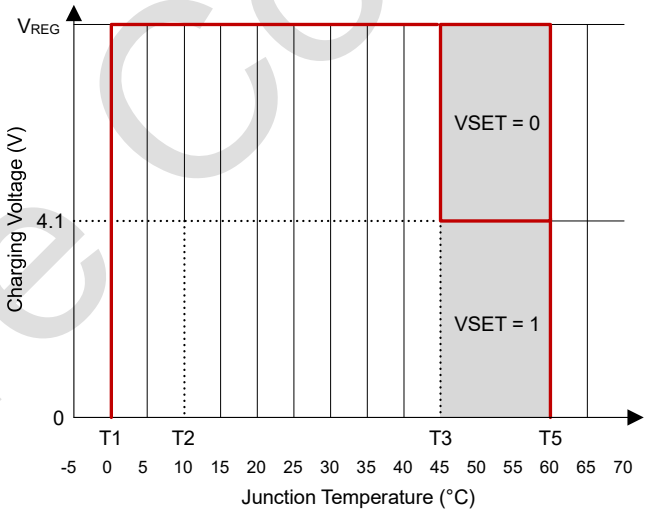


Figure 8. JEITA Profile: Charging Voltage

Equation 1 through Equation 2 describe updates to the resistor bias network.

$$RT2 = \frac{V_{REGN} \times RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{VT1} - \frac{1}{VT5}\right)}{RTH_{HOT} \times \left(\frac{V_{REGN}}{VT5} - 1\right) - RTH_{COLD} \times \left(\frac{V_{REGN}}{VT1} - 1\right)} \quad (1)$$

$$RT1 = \frac{\left(\left(\frac{V_{REGN}}{VT1}\right) - 1\right)}{\left(\frac{1}{RT2}\right) + \left(\frac{1}{RTH_{COLD}}\right)} \quad (2)$$

Select 0°C to 60°C range for Li-ion or Li-polymer battery:

- RTHCOLD = 27.28 KΩ
- RTHHOT = 3.02 KΩ
- RT1 = 5.23 KΩ
- RT2 = 30.9 KΩ

8.3.4.6 Charging Safety Timer

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The device has built-in safety timer to prevent extended charging cycle due to abnormal battery conditions. The safety timer is 2 hours when the battery is below $V_{BATLOWV}$ threshold and 10 hours when the battery is higher than VBATLOWV threshold.

The user can program fast charge safety timer through I^2C (CHG_TIMER bits). When safety timer expires, the fault register CHRG_FAULT bits are set to 11 and an INT is asserted to the host. The safety timer feature can be disabled through I^2C by setting EN_TIMER bit

During input voltage, current, JEITA cool or thermal regulation, the safety timer counts at half clock rate as the actual charge current is likely to be below the register setting. For example, if the charger is in input current regulation (IDPM_STAT = 1) throughout the whole charging cycle, and the safety time is set to 5 hours, the safety timer will expire in 10 hours. This half clock rate feature can be disabled by writing 0 to TMR2X_EN bit.

During the fault, timer is suspended. Once the fault goes away, fault resumes. If user stops the current charging cycle, and start again, timer gets reset (toggle CE pin or CHRG_CONFIG bit).

8.3.5 Shipping Mode

8.3.5.1 BATFET Disable Mode (Shipping Mode)

To extend battery life and minimize power when system is powered off during system idle, shipping, or storage, the device can turn off BATFET so that the ICSP voltage is zero to minimize the battery leakage current. When the host set BATFET_DIS bit, the charger can turn off BATFET immediately or delay by t_{SM_DLY} as configured by BATFET_DLY bit.

8.3.5.2 BATFET Enable (Exit Shipping Mode)

When the BATFET is disabled (in shipping mode) and indicated by setting BATFET_DIS, one of the following events can enable BATFET:

1. Plug in adapter
2. Clear BATFET_DIS bit
3. Set REG_RST bit to reset all registers including BATFET_DIS bit to default (0)

8.3.6 Status Outputs ($\overline{PG}$, STAT, $\overline{INT}$)

8.3.6.1 Power Good indicator ($\overline{PG}$ Pin and PG_STAT Bit)

The PG_STAT bit goes HIGH and $\overline{PG}$ pin goes LOW to indicate a good input source when:

- VBUS above V_{VBUS_UVLO}
- VBUS above battery (not in sleep)
- VBUS below V_{VAC_OV} threshold
- VBUS above $V_{VBUSMIN}$ (typical 3.8 V) when I_{BADSRC} (typical 30 mA) current is applied (not a poor source)
- Completed input Source Type Detection

8.3.6.2 Charging Status indicator (STAT)

The device indicates charging state on the open drain STAT pin. The STAT pin can drive LED. The STAT pin function can be disabled by setting the EN_ICHG_MON bits = 11.

Table 4. STAT Pin State

CHARGING STATE	STAT INDICATOR
Charging in progress (including recharge)	LOW
Charging complete	HIGH
Sleep mode, charge disable	HIGH

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Charge suspend (input overvoltage, TS fault, timer fault)	Blinking at 1 Hz

8.3.6.3 Interrupt to Host ($\overline{INT}$)

In some applications, the host does not always monitor the charger operation. The INT pulse notifies the system on the device operation. The following events will generate 256-μs INT pulse.

- USB/adapter source identified (through PSEL detection)
- Good input source detected
  - VBUS above battery (not in sleep)
  - VBUS below V_{VAC_OV} threshold
  - VBUS above $V_{VBUSMIN}$ (typical 3.8 V) when I_{BADSRC} (typical 30 mA) current is applied (not a poor source)
- input removed
- Charge Complete
- Any FAULT event in REG09

When a fault occurs, the charger device sends out INT and keeps the fault state in REG09 until the host reads the fault register. Before the host reads REG09 and all the faults are cleared, the charger device would not send any INT upon new faults. To read the current fault status, the host has to read REG09 two times consecutively. The first read reports the pre-existing fault register status and the second read reports the current fault register status.

8.3.7 Protections

8.3.7.1 Voltage and Current Monitoring in Converter Operation

The device closely monitors the input voltage, as well as internal FET currents for safe buck mode operation.

8.3.7.1.1 Voltage and Current Monitoring in Buck Mode

8.3.7.1.1.1 Input Overvoltage (ACOV)

If VBUS voltage exceeds V_{VAC_OV} (programmable via OVP[2:0] bits), the device stops switching immediately.

During input overvoltage event (ACOV), the fault register CHRG_FAULT bits are set to 01. An INT pulse is asserted to the host. The device will automatically resume normal operation once the input voltage drops back below the OVP threshold.

8.3.7.2 Thermal Regulation and Thermal Shutdown

8.3.7.2.1 Thermal Protection in Buck Mode

The CX25601 monitors the internal junction temperature T_J to avoid overheat the chip and limits the IC surface temperature in buck mode. When the internal junction temperature exceeds thermal regulation limit (110°C), the device lowers down the charge current. During thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, termination is disabled, the safety timer runs at half the clock rate, and the status register THERM_STAT bit goes high.

Additionally, the device has thermal shutdown to turn off the converter and BATFET when IC surface temperature exceeds T_{SHUT}(160ºC). The fault register CHRG_FAULT is set to 1 and an INT is asserted to the host. The BATFET and converter is enabled to recover when IC temperature is T_{SHUT_HYS} (30ºC) below T_{SHUT}(160ºC).

8.3.7.3 Battery Protection

8.3.7.3.1 Battery overvoltage Protection (BATOVP)

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The battery overvoltage limit is clamped at 4% above the battery regulation voltage. When battery over voltage occurs, the charger device immediately disables charging. The fault register BAT_FAULT bit goes high and an INT is asserted to the host.

8.3.7.3.2 Battery Over-Discharge Protection

When battery is discharged below $V_{BAT_DPL_FALL}$, the BATFET is turned off to protect battery from over discharge. To recover from over-discharge latch-off, an input source plug-in is required at VBUS. The battery is charged with I_{SHORT} (typically 100 mA) current when the $V_{BAT} < V_{SHORT}$, or precharge current as set in IPRECHG register when the battery voltage is between V_{SHORTZ} and V_{BAT_LOWV}.

8.3.7.3.3 Battery Over-Current Protection

When the ICSP pin is shorted or significantly overloaded ($I_{BAT} > I_{BATOP}$) and the current exceeds BATFET overcurrent limit, the BATFET latches off. Section BATFET Enable (Exit Shipping Mode) can reset the latch-off condition and turn on BATFET.

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8.3.8 Serial interface

The device uses I²C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I²C™ is a bi-directional 2-wire serial interface developed by Philips Semiconductor (now NXP Semiconductors). Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 6BH, receiving control inputs from the master device like micro controller or a digital signal processor through REG00-REG0B. Register read beyond REG0B (0x0B) returns 0xFF. The I²C interface supports both standard mode (up to 100 kbits), and fast mode (up to 400 kbits). connecting to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

8.3.8.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

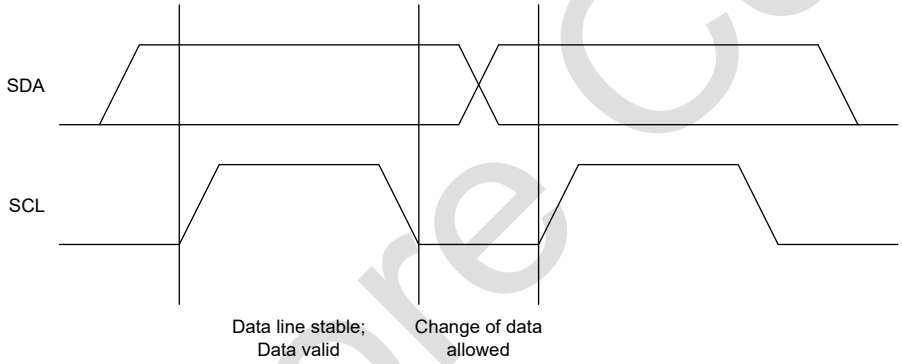


Figure 13. Bit Transfer on the I2C Bus

8.3.8.2 START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition. START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

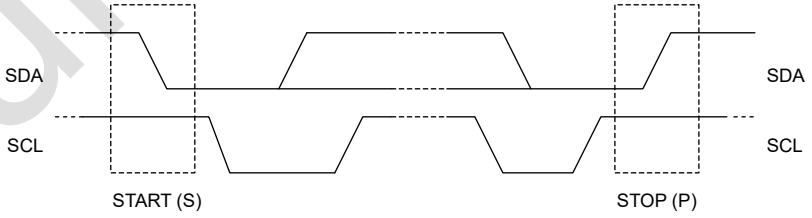


Figure 14. TS START and STOP conditions

8.3.8.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

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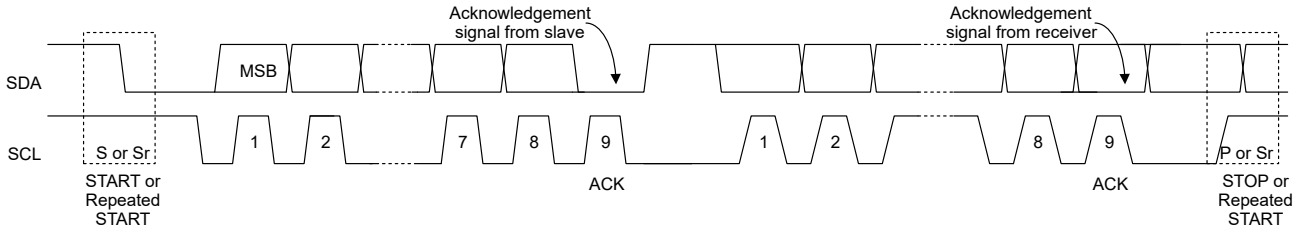


Figure 15. Data Transfer on the I2C Bus

8.3.8.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge ninth clock pulse, are generated by the master. The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the ninth clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

8.3.8.5 Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

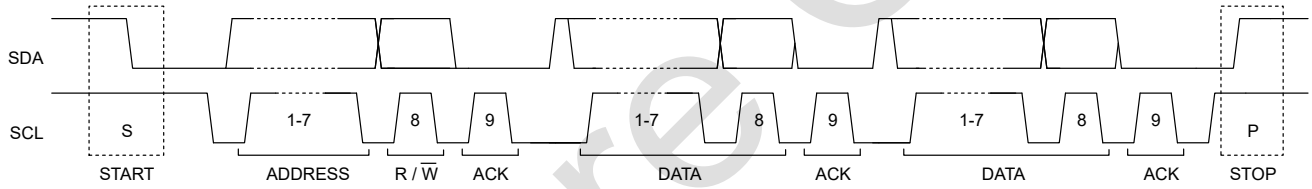


Figure 16. Complete Data Transfer

8.3.8.6 Single Read and Write

If the register address is not defined, the charger IC send back NACK and go back to the idle state.



Figure 17. Single Write

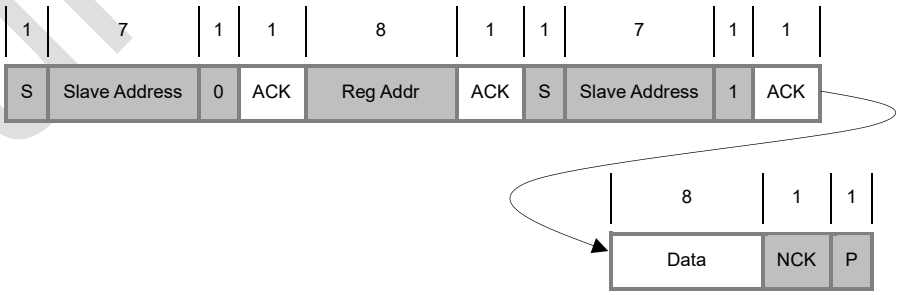


Figure 18. Single Read

8.3.8.7 Multi-Read and Multi-Write

The charger device supports multi-read and multi-write on REG00 through REG0B.

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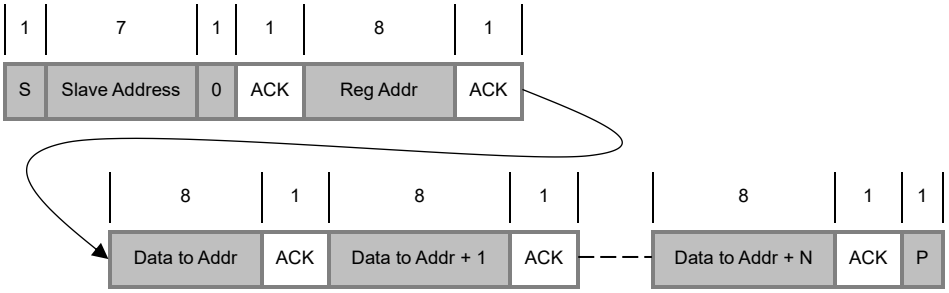


Figure 19. Multi-Write



Figure 20. Multi-Read

REG09 is a fault register. It keeps all the fault information from last read until the host issues a new read. For example, if Charge Safety Timer Expiration fault occurs but recovers later, the fault register REG09 reports the fault when it is read the first time, but returns to normal when it is read the second time. in order to get the fault information at present, the host has to read REG09 for the second time. The only exception is NTC_FAULT which always reports the actual condition on the TS pin. in addition, REG09 does not support multi-read and multi-write.

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8.4 Register Maps

I²C Slave Address: 6BH (1101011B + R/$\overline{W}$)

REG	Bit	Field	Type	Reset	Default	Description	
00	7	Reserved	R	N/A	0		
	6	EN_ICHG_MON[1]	R/W	by REG_RST	0	00 – Enable STAT pin function (default) 01 – Reserved 10 – Reserved 11 – Disable STAT pin function (float pin)	
	5	EN_ICHG_MON[0]	R/W	by REG_RST	0		
	4	IINDPM[4]	R/W	by REG_RST	1	1600mA	Input Current Limit Offset: 100mA Range: 100mA (00000) – 3.2A (11111) Default: 2400mA (10111), maximum input current limit, not typical. IINDPM bits are changed automatically after input source detection is completed CX25601: PSEL = Hi = 500mA PSEL = Lo = 2.4A
	3	IINDPM[3]	R/W	by REG_RST	0	800mA	
	2	IINDPM[2]	R/W	by REG_RST	1	400mA	
	1	IINDPM[1]	R/W	by REG_RST	1	200mA	
	0	IINDPM[0]	R/W	by REG_RST	1	100mA	
REG	**Bit**	**Field**	**Type**	**Reset**	**Default**	**Description**	
01	7	Reserved	R	N/A	0		
	6	WD_RST	R/W	N/A	0	I2C Watchdog Timer Reset 0 – Normal 1 – Reset (Back to 0 after timer reset)	
	5	Reserved	R	N/A	0		
	4	CHG_CONFIG	R/W	by REG_RST by Watchdog	1	Charge Enable Configuration 0 – Charge Disable 1 – Charge Enable (default)	
	3	Reserved	R	N/A	1		
	2	Reserved	R	N/A	0		
	1	Reserved	R	N/A	1		
	0	Reserved	R	N/A	0		
REG	**Bit**	**Field**	**Type**	**Reset**	**Default**	**Description**	
02	7	Reserved	R	N/A	1		
	6	Q1_FULLON	R/W	by REG_RST	0	0 – Use higher Q1 Rdson when programmed IINDPM<700mA (default, better accuracy) 1 – Use lower Q1 Rdson always (better efficiency)	
	5	ICHG[5]	R/W	by REG_RST by Watchdog	1	1920mA	Fast Charge Current Range: 0mA (000000) – 3000mA (110010) Default: 2040mA (100010) Note: ICHG = 0mA disables charge. ICHG > 3000mA (110010) clamped to register value 3000mA.
	4	ICHG[4]	R/W	by REG_RST by Watchdog	0	960mA	
	3	ICHG[3]	R/W	by REG_RST by Watchdog	0	480mA	
	2	ICHG[2]	R/W	by REG_RST by Watchdog	0	240mA	
	1	ICHG[1]	R/W	by REG_RST by Watchdog	1	120mA	
	0	ICHG[0]	R/W	by REG_RST by Watchdog	0	60mA	
REG	**Bit**	**Field**	**Type**	**Reset**	**Default**	**Description**	
03	7	IPRECHG[3]	R/W	by REG_RST by Watchdog	0	480mA	Precharge Current Offset: 60mA Default: 180mA (0010) Note: IPRECHG > 780mA clamped to 780mA (1100)
	6	IPRECHG[2]	R/W	by REG_RST by Watchdog	0	240mA	
	5	IPRECHG[1]	R/W	by REG_RST by Watchdog	1	120mA	
	4	IPRECHG[0]	R/W	by REG_RST by Watchdog	0	60mA	
	3	ITERM[3]	R/W	by REG_RST by Watchdog	0	480mA	Termination Current Offset: 60mA

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	2	ITERM[2]	R/W	by REG_RST by Watchdog	0	240mA	Default: 180mA (0010) Note: ITERM > 780mA clamped to 780mA (1100)
	1	ITERM[1]	R/W	by REG_RST by Watchdog	1	120mA	
	0	ITERM[0]	R/W	by REG_RST by Watchdog	0	60mA	
REG	**Bit**	**Field**	**Type**	**Reset**	**Default**	**Description**	
04	7	VREG[5]	R/W	by REG_RST by Watchdog	0	512mV	Charge Voltage Offset: 3.856V Range: 3.856V – 4.624V (11000) Default: 4.208V (01011) Note: Value above 11000 (4.624V) is clamped to register value 11000 (4.624V). REG04[7:3] is for compatibility, when write to REG04, VREG[0] will be automatically set 0. If need more VREG[5:0] settings, please use REG0E[7:2].
	6	VREG[4]	R/W	by REG_RST by Watchdog	1	256mV	
	5	VREG[3]	R/W	by REG_RST by Watchdog	0	128mV	
	4	VREG[2]	R/W	by REG_RST by Watchdog	1	64mV	
	3	VREG[1]	R/W	by REG_RST by Watchdog	1	32mV	
	2	Reserved	R	N/A	0		
	1	Reserved	R	N/A	0		
	0	VRECHG	R/W	by REG_RST by Watchdog	0	Battery Recharge Threshold (below VREG) 0 – 100mV (default) 1 – 200mV	
REG	**Bit**	**Field**	**Type**	**Reset**	**Default**	**Description**	
05	7	EN_TERM	R/W	by REG_RST by Watchdog	1	Enable Charge Termination 0 – Disable, 1 – Enable (default)	
	6	Reserved	R	N/A	0		
	5	WATCHDOG [1]	R/W	by REG_RST by Watchdog	0	I2C Watchdog Timer Setting 00 – Disable watchdog timer 01 – 40s (default) 10 – 80s 11 – 160s	
	4	WATCHDOG [0]	R/W	by REG_RST by Watchdog	1		
	3	EN_TIMER	R/W	by REG_RST by Watchdog	1	Charging Safety Timer Enable 0 – Disable 1 – Enable (default)	
	2	CHG_TIMER	R/W	by REG_RST by Watchdog	1	Fast Charge Timer Setting 0 – 5hrs 1 – 10hrs (default)	
	1	TREG[0]	R/W	by REG_RST by Watchdog	1	Thermal Regulation Threshold 0 - 100°C 1 - 120°C (default) Note: REG05[1] is for compatibility, when write to REG05, TREG[1] will be automatically set 1. If need more TREG[1:0] settings, please use REG0F[7:6].	
	0	JEITA_ISET (0℃-10℃)	R/W	by REG_RST by Watchdog	1	JEITA Low Temperature Charge Current Setting 0 – 50% of CC 1 – 20% of CC (default)	
REG	**Bit**	**Field**	**Type**	**Reset**	**Default**	**Description**	
06	7	OVP[1]	R/W	by REG_RST	0	ACOV threshold: 00 – 5.5V 01 – 6.5V (5V input, default) 10 – 10.5V (9V input) 11 – 14V (12V input)	
	6	OVP[0]	R/W	by REG_RST	1		
	5	Reserved	R	N/A	1		
	4	Reserved	R	N/A	0		
	3	VINDPM[3]	R/W	by REG_RST	0	Absolute VINDPM Threshold Offset: 3.9V Range: 4.8V (1001) – 5.4V (1111) Default: 4.5V (0110)	
	2	VINDPM[2]	R/W	by REG_RST	1		
	1	VINDPM[1]	R/W	by REG_RST	1		
	0	VINDPM[0]	R/W	by REG_RST	0		
REG	**Bit**	**Field**	**Type**	**Reset**	**Default**	**Description**	
07	7	IINDET_EN	R/W	by REG_RST by Watchdog	0	Input Current Limit Detection 0 – Not in PSEL detection 1 – Force PSEL detection (Back to 0 after ICL detection is complete)	
	6	TMR2X_EN	R/W	by REG_RST by Watchdog	1	Safety Timer Setting during DPM or Thermal Regulation 0 – Safety timer not slowed by 2X during input DPM or thermal regulation 1 – Safety timer slowed by 2X during input DPM or thermal regulation	

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	5	BATFET_DIS	R/W	by REG_RST	0	Force BATFET off to enable ship mode 0 – Allow BATFET turn on 1 – Force BATAFET off
	4	JEITA_VSET (45℃-60℃)	R/W	by REG_RST by Watchdog	0	JEITA High Temperature Charge Voltage Setting 0 – Set Charge Voltage to VREG-200mV during JEITA high temperature 1 – Set Charge Voltage to VREG during JEITA high temperature
	3	BATFET_DLY	R/W	by REG_RST	1	BATFET turn off delay control 0 – BATFET turn off immediately when BATET_DIS bit is set 1 – BATFET turn off delay by t_{SM_DLY} (typ. 10s) when BATFET_DIS bit is set
	2	Reserved	R	N/A	1	
	1	VDPM_TRACK[1]	R/W	by REG_RST	0	Sets VINDPM to track BAT voltage. Actual VINDPM is higher of register value and VBAT+VDPM_TRACK. 00 – Disable tracking function (VINDPM is set by register) 01 – VBAT + 200mV 10 – VBAT + 250mV 11 – VBAT + 300mV
	0	VDPM_TRACK[0]	R/W	by REG_RST	0	
REG	**Bit**	**Field**	**Type**	**Reset**	**Default**	**Description**
08	7	VBUS_STAT[2]	R	N/A	0	VBUS Status CX25601: 000 – No Input 001 – USB Host SDP (500mA) → PSEL HIGH 011 – Adapter 2.4A → PSEL LOW Software current limit is reported in IINDPM register
	6	VBUS_STAT[1]	R	N/A	0	
	5	VBUS_STAT[0]	R	N/A	0	
	4	CHRG_STAT[1]	R	N/A	0	Charging Status 00 – Not in Charging 01 – Pre-Charge (<$V_{BATLOWV}$) 10 – Fast Charge 11 – Charge Termination Done
	3	CHRG_STAT[0]	R	N/A	0	
	2	PG_STAT	R	N/A	0	Power Good Status 0 – Not Power Good 1 – Power Good
	1	THERM_STAT	R	N/A	0	Thermal Regulation Status 0 – Normal 1 – In Thermal Regulation
	0	Reserved	R	N/A	0	
REG	**Bit**	**Field**	**Type**	**Reset**	**Default**	**Description**
09	7	WATCHDOG_FAULT	R	N/A	1	I2C Watchdog Fault Status 0 – Normal 1 – Watchdog timer expiration
	6	Reserved	R	N/A	0	
	5	CHRG_FAULT[1]	R	N/A	0	Charger Fault Status 00 – Normal 01 – Input fault (VBUS>V_{ACOV} or VBAT<VBUS<V_{BUSMIN} (typical 3.8V)) 10 – Thermal shutdown 11 – Charger Safety Timer Expiration
	4	CHRG_FAULT[0]	R	N/A	0	
	3	BAT_FAULT	R	N/A	0	Battery Fault Status 0 – Normal 1 – BATOVP (VBAT>V_{BATOVP})
	2	NTC_FAULT[2]	R	N/A	0	NTC Fault Status Charge Mode: 000 – Normal 010 – TS Warm 011 – TS Cool 101 – TS Cold 110 – TS Hot
	1	NTC_FAULT[1]	R	N/A	0	
	0	NTC_FAULT[0]	R	N/A	0	
REG	**Bit**	**Field**	**Type**	**Reset**	**Default**	**Description**
0A	7	VBUS_GD	R	N/A	0	VBUS Good Status 0 – Not VBUS attached 1 – VBUS attached
	6	VINDPM_STAT	R	N/A	0	0 – Not in VINDPM 1 – in VINDPM
	5	IINDPM_STAT	R	N/A	0	0 – Not in IINDPM 1 – in IINDPM
	4	Reserved	R	N/A	0	
	3	Reserved	R	N/A	0	
	2	ACOV_STAT	R	N/A	0	0 – Device is NOT in ACOV 1 – Device is in ACOV
	1	Reserved	R	N/A	0	
	0	Reserved	R	N/A	0	
REG	**Bit**	**Field**	**Type**	**Reset**	**Default**	**Description**

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0B	7	REG_RST	R/W	N/A	0	Register reset 0 – Keep current register setting 1 – Reset to default register value and reset safety timer Note: Bit resets to 0 after register reset is completed
	6	PN[3]	R	N/A	X	CX25601 - 0010
	5	PN[2]	R	N/A	X	
	4	PN[1]	R	N/A	X	
	3	PN[0]	R	N/A	X	
	2	Reserved	R	N/A	X	
	1	DEV_REV[1]	R	N/A	X	
	0	DEV_REV[0]	R	N/A	X	
REG	**Bit**	**Field**	**Type**	**Reset**	**Default**	**Description**
0C	7	Reserved	R	N/A	0	
	6	Reserved	R	N/A	1	
	5	Reserved	R	N/A	1	
	4	Reserved	R	N/A	0	
	3	Reserved	R	N/A	0	
	2	Reserved	R	N/A	0	
	1	Reserved	R	N/A	1	
	0	ICO_EN	R/W	by REG_RST	0	Enable Input Current Limit Optimization (ICO) 0 – Disable Optimization 1 – Enable Optimization
REG	**Bit**	**Field**	**Type**	**Reset**	**Default**	**Description**
0D	7	FORCE_ICO	R/W	by REG_RST	0	Force Start Input Current Limit Optimization (ICO) 0 – Do not force ICO 1 – Force ICO (can be set only and will back to 0 after ICO starts)
	6	ICO_OPTIMIZED	R	N/A	0	Input Current Limit Optimization (ICO) Status 0 – Optimization is in progress 1 – Maximum Input Current Detected
	5	IDPM_LIM[5]	R	N/A	0	1600mA Input Current Limit in effect while Input Current Optimizer (ICO) is enabled Offset: 100mA Range: 100mA (000000) – 3.25A (111111)
	4	IDPM_LIM[4]	R	N/A	0	800mA
	3	IDPM_LIM[3]	R	N/A	0	400mA
	2	IDPM_LIM[2]	R	N/A	0	200mA
	1	IDPM_LIM[1]	R	N/A	0	100mA
	0	IDPM_LIM[0]	R	N/A	0	50mA
REG	**Bit**	**Field**	**Type**	**Reset**	**Default**	**Description**
0E	7	VREG[5]	R/W	by REG_RST by Watchdog	0	512mV Charge Voltage Offset: 3.856V Range: 3.856V – 4.624V (110000) Default: 4.208V (010110) Note: Value above 110000 (4.624V) is clamped to register value 110000 (4.624V)
	6	VREG[4]	R/W	by REG_RST by Watchdog	1	256mV
	5	VREG[3]	R/W	by REG_RST by Watchdog	0	128mV
	4	VREG[2]	R/W	by REG_RST by Watchdog	1	64mV
	3	VREG[1]	R/W	by REG_RST by Watchdog	1	32mV
	2	VREG[0]	R/W	by REG_RST by Watchdog	0	16mV
	1	Reserved	R	N/A	0	
	0	Reserved	R	N/A	0	
REG	**Bit**	**Field**	**Type**	**Reset**	**Default**	**Description**
0F	7	TREG[1]	R/W	by REG_RST by Watchdog	1	Thermal Regulation Threshold 00 - 60°C 01 - 80°C 10 - 100°C 11 - 120°C (default)
	6	TREG[0]	R/W	by REG_RST by Watchdog	1	
	5	BAT_COMP[2]	R/W	by REG_RST by Watchdog	0	80mΩ IR Compensation Resistor Setting Range: 0 – 140mΩ

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	4	BAT_COMP[1]	R/W	by REG_RST by Watchdog	0	40mΩ	Default: 0mΩ (000) (i.e. Disable IR Comp)
	3	BAT_COMP[0]	R/W	by REG_RST by Watchdog	0	20mΩ	
	2	VCLAMP[2]	R/W	by REG_RST by Watchdog	0	128mV	IR Compensation Resistor Setting Offset: 0mV Range: 0 – 224mV Default: 0mV (000)
	1	VCLAMP[1]	R/W	by REG_RST by Watchdog	0	64mV	
	0	VCLAMP[0]	R/W	by REG_RST by Watchdog	0	32mV	
REG	**Bit**	**Field**	**Type**	**Reset**	**Default**	**Description**	

9 Application and Implementation

9.1 Application information

A typical application consists of the device configured as an I²C controlled device and a single cell battery charger for Li-Ion and Li-polymer batteries used in a wide range of smart phones and other portable devices. It integrates an input reverse-block FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET Q4) between the ICSP and battery. The device also integrates a bootstrap diode for the high-side gate drive.

9.2 Typical Application Diagram

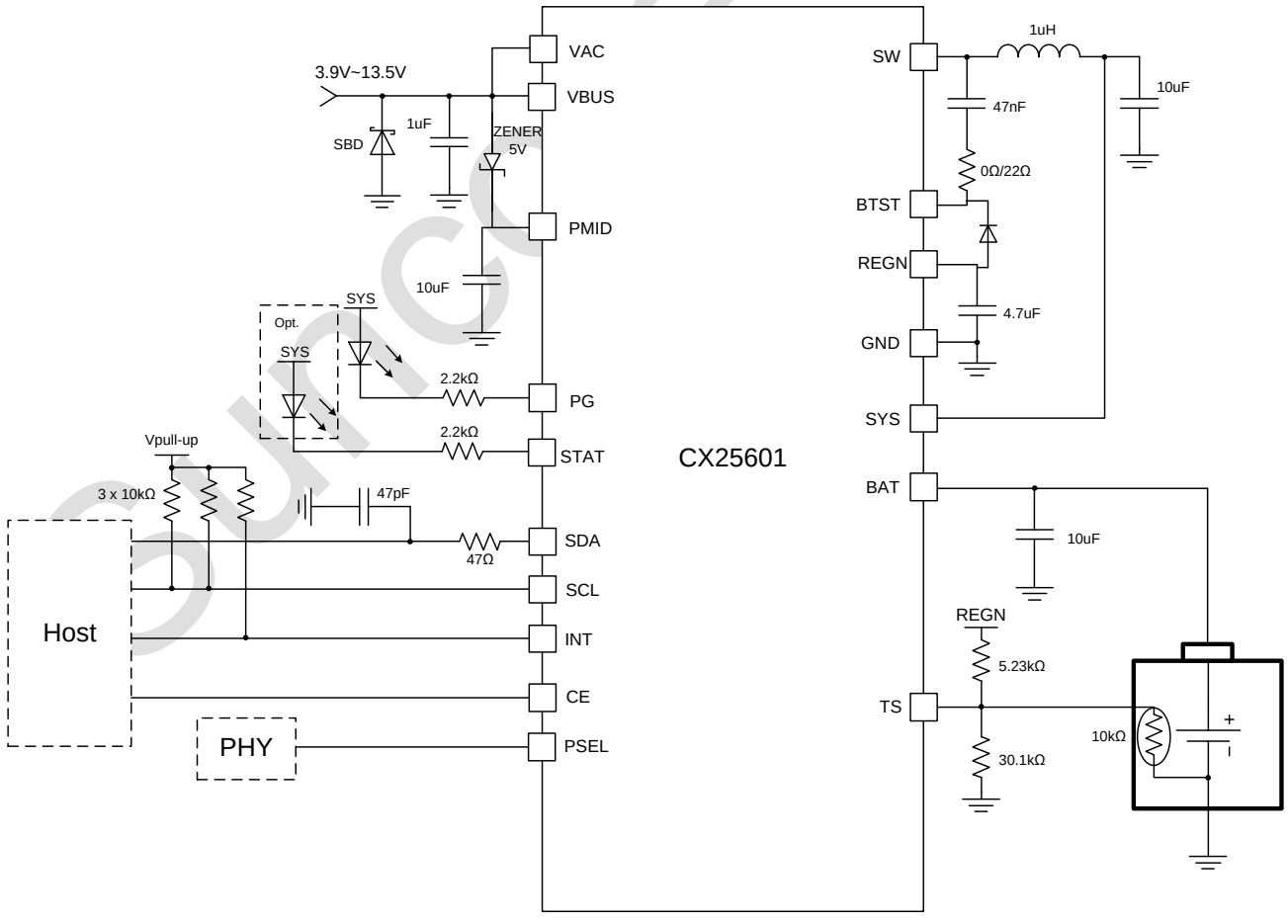


Figure 21. CX25601 Applications Diagram

9.2.1 Detailed Design Procedure

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9.2.1.1 inductor Selection

The 1.5-MHz switching frequency allows the use of small inductor and capacitor values to maintain an inductor saturation current higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2)\ I_{RIPPLE} \quad (3)$$

The inductor ripple current depends on the input voltage (V_{VBUS}), the duty cycle ($D = V_{BAT}/V_{VBUS}$), the switching frequency (f_S) and the inductance (L).

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1-D)}{fs \times L} \quad (4)$$

The maximum inductor ripple current occurs when the duty cycle (D) is 0.5 or approximately 0.5. Usually inductor ripple is designed in the range between 20% and 40% maximum charging current as a trade-off between inductor size and efficiency for a practical design.

9.2.1.2 input Capacitor

Design input capacitance to provide enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current I_{Cin} occurs where the duty cycle is closest to 50% and can be estimated using Equation 5.

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1-D)} \quad (5)$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high-side MOSFET and source of the low-side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. A rating of 25-V or higher capacitor is preferred for 15 V input voltage. Capacitance of 22-μF is suggested for typical of 3A charging current.

9.2.1.3 Output Capacitor

Ensure that the output capacitance has enough ripple current rating to absorb the output switching ripple current. Equation 6 shows the output capacitor RMS current I_{COUT} calculation.

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (6)$$

The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_O = \frac{V_{OUT}}{8LCfs^2}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

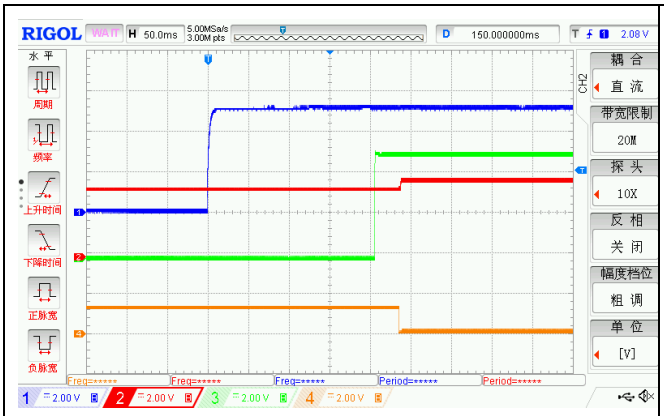
At certain input and output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

The charger device has internal loop compensation optimized for >20μF ceramic output capacitance. The preferred ceramic capacitor is 10V rating, X7R or X5R.

9.3 Application Curves

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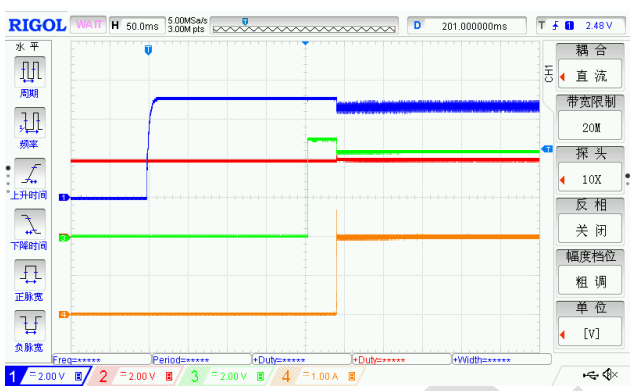
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CH1 VBUS CH2 VICSP CH3 REGN CH4 PG

VBUS = 5 V VBAT = 3.2 V

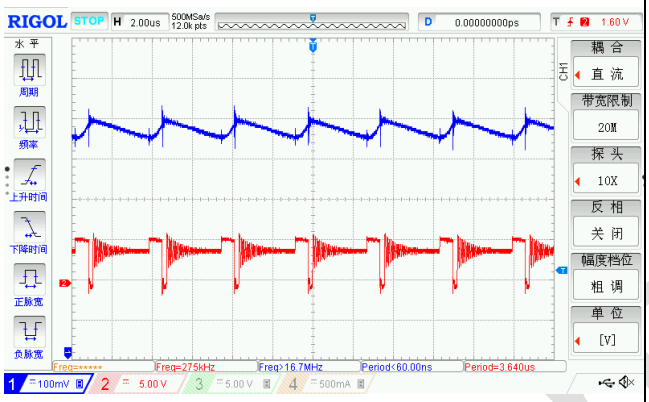
Figure 22. Power-Up with Charge Disabled



CH1 VBUS CH2 VICSP CH3 REGN CH4 IBAT

VBUS = 5 V VBAT = 3.2 V ICHG = 2 A

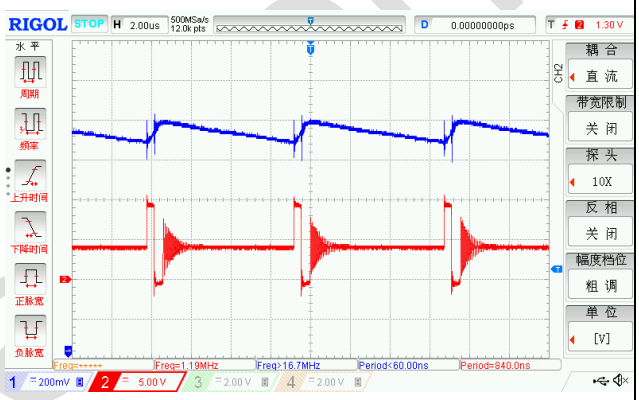
Figure 23. Power-Up with Charge Enabled



CH1 VICSP CH2 SW

VBUS=5V IICSP=0.1A charge disabled no bat

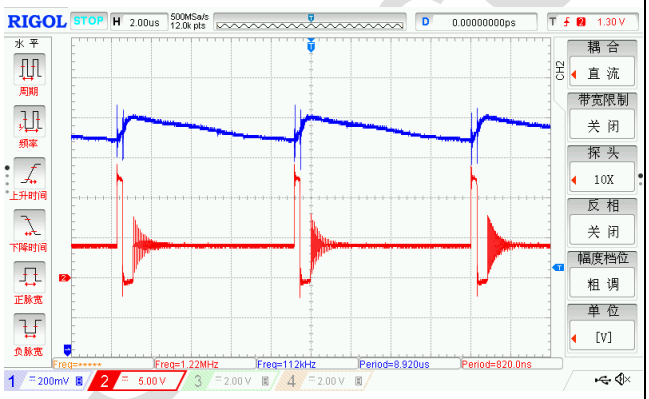
Figure 24. PFM Switching in Buck Mode



CH1 VICSP CH2 SW

VBUS=9V IICSP=0.1A charge disabled no bat

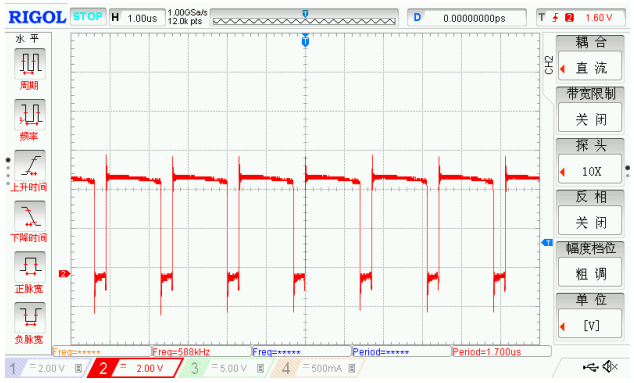
Figure 25. PFM Switching in Buck Mode



CH1 VICSP CH2 SW

VBUS=12V IICSP=0.1A charge disabled no bat

Figure 26. PFM Switching in Buck Mode



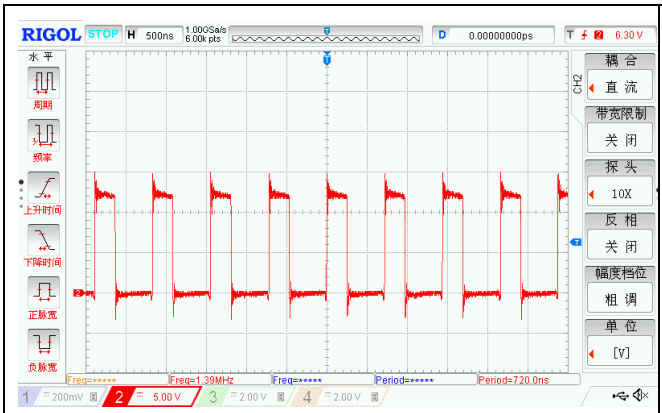
CH2 SW

VBUS=5V VBAT=3.8V ICHG=2A

Figure 27. PWM Switching in Buck Mode

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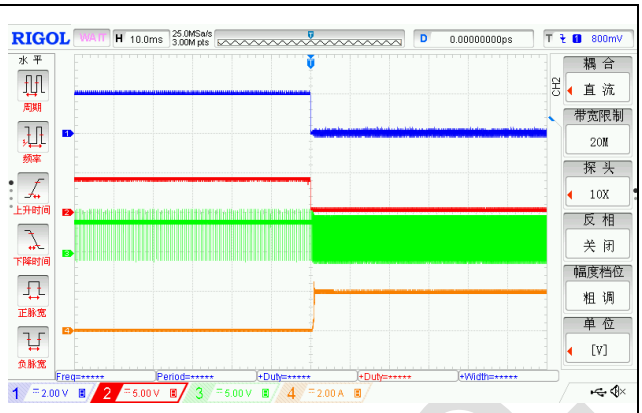
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CH2 SW

VBUS=12V VBAT=3.8V ICHG=2A

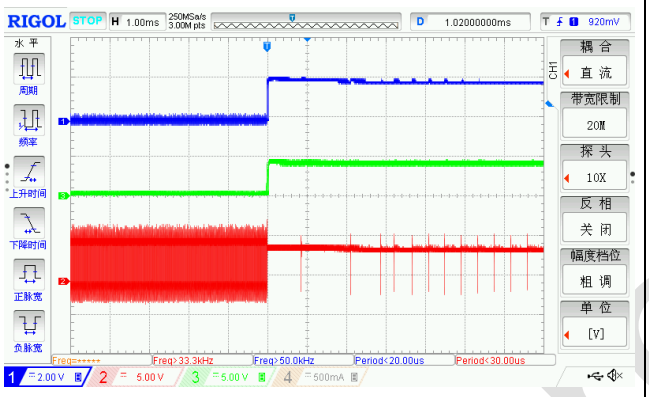
Figure 28. PWM Switching in Buck Mode



CH1 STAT CH2 CE CH3 SW CH4 IBAT

VBUS=5V VBAT=3.8V ICHG=2A

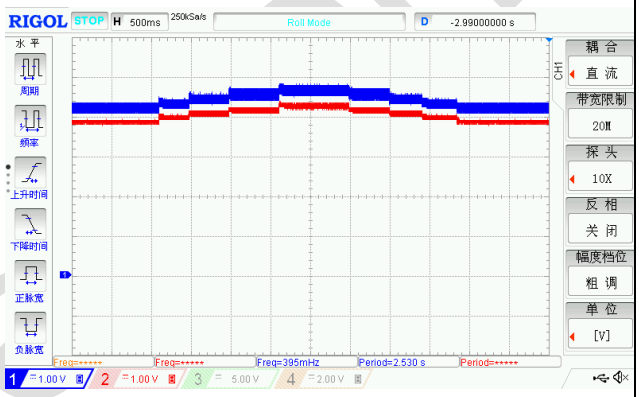
Figure 29. Charge Enable



CH1 STAT CH2 SW CH3 CE

VBUS=5V VBAT=3.8V ICHG=2A

Figure 30. Charge Disable



CH1 VBUS CH2 VBAT

VBAT=3.7V~4.1V Adaptor ILIM = 1 A

Figure 37. VINDPM Tracking Battery Voltage

10 Power Supply Recommendations

In order to provide an output voltage on ICSP, the CX25601 device requires a power supply between 3.9 V and 14.2 V input with at least 100-mA current rating connected to VBUS and a single-cell Li-Ion battery with voltage > $V_{BATUVLO}$ connected to BAT. The source current rating needs to be at least 3A in order for the buck converter of the charger to provide maximum output power to ICSP.

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11 Layout

11.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see Figure 38) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

1. Place input capacitor as close as possible to PMID pin and GND pin connections and use shortest copper trace connection or GND plane.
2. Place inductor input pin to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
3. Put output capacitor near to the inductor and the device. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
4. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using thermal pad as the single ground connection point. Or using a 0-Ω resistor to tie analog ground to power ground.
5. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the device. Use ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.
6. Place decoupling capacitors next to the IC pins and make trace connection as short as possible.
7. It is critical that the exposed thermal pad on the backside of the device package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
8. Ensure that the number and sizes of vias allow enough copper for a given current path.

11.2 Layout Example

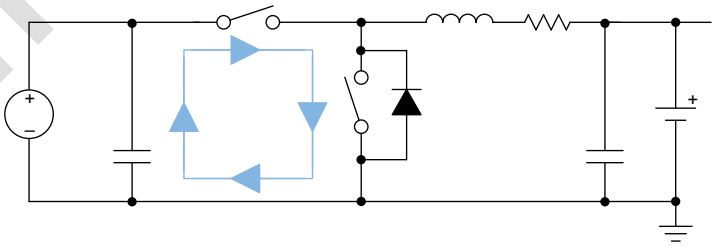


Figure 38. High Frequency Current Path

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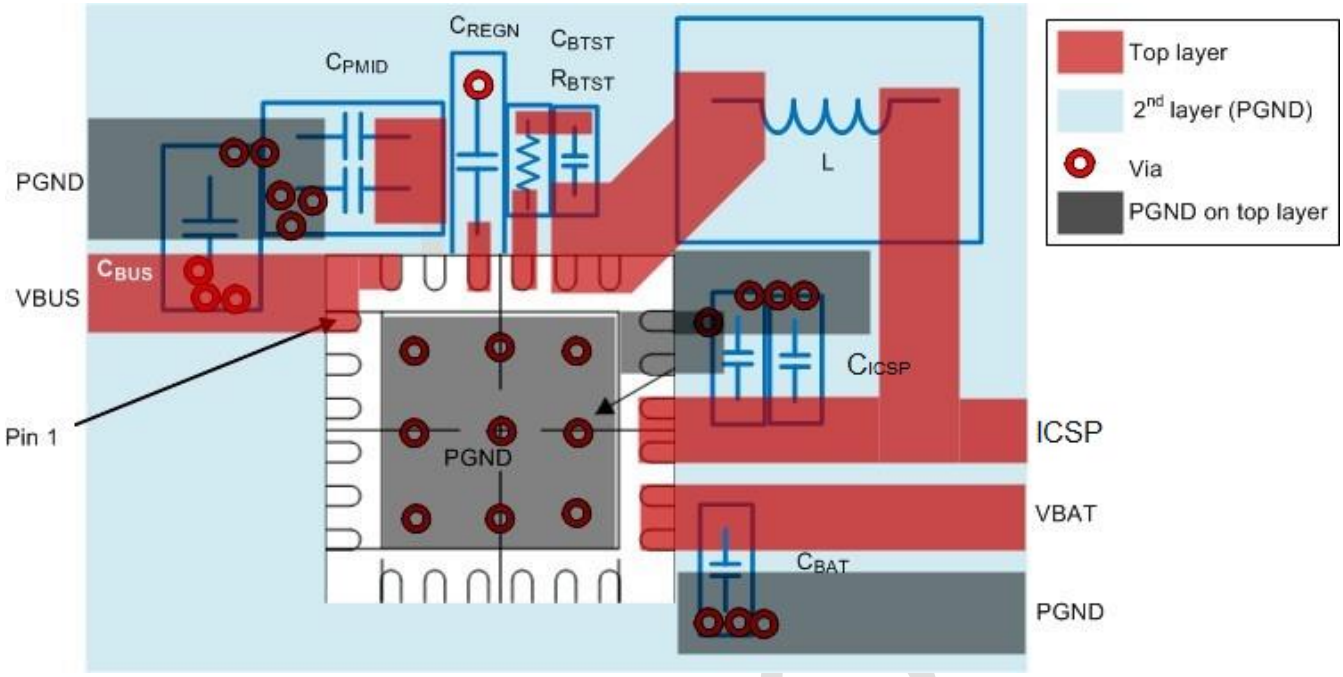
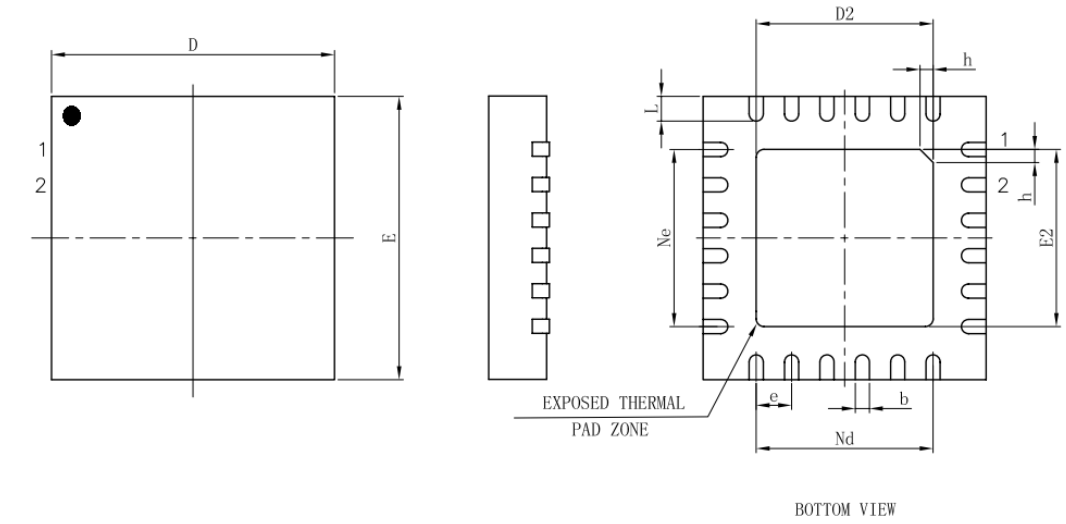


Figure 39. Layout Example

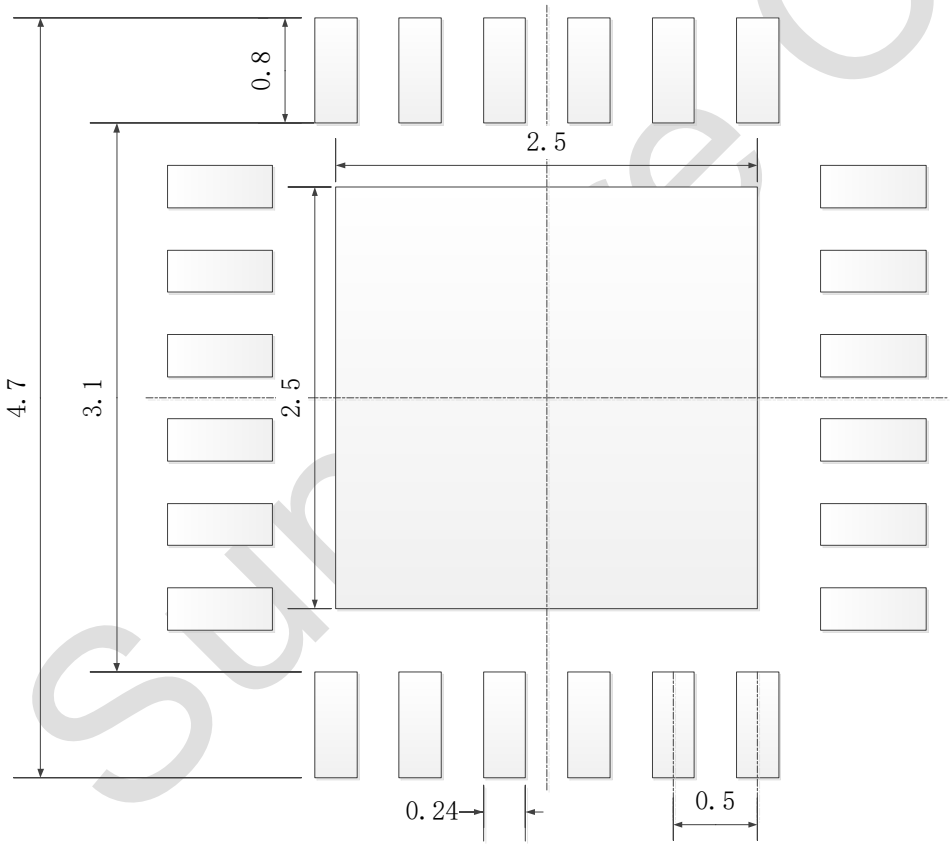
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12 Packaging



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.40	2.50	2.60
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.40	2.50	2.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F载体尺寸	110x110		



RECOMMENDED LAND PATTERN (Unit: mm)

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