da230

MEMS digital output motion sensor

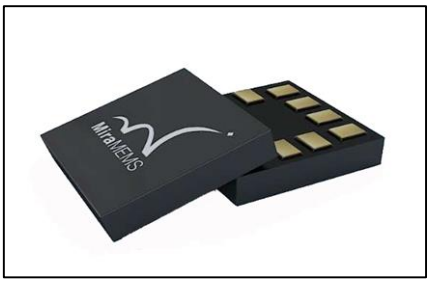
Ultra-low-power high performance 3-axes “DSC-XYZ” accelerometer

Key Features

- Supply voltage, 1.62V to 3.6V
- For 2x2x0.9 mm LGA-12 package
- User selectable range, ±2g, ±4g, ±8g, ±16g
- User selectable data output rate
- Digital I^2C/SPI output interface
- 14 bit resolution
- Ultra-low power consumption to 12.8uA@125Hz
- Embedded 32-level FIFO
- Internal step counter
- 2 Programmable interrupt generators with independent function for tap interrupt detection
- Factory programmable offset and sensitivity
- RoHS compliant

Applications

- Active monitoring
- Double/single Click recognition
- Step counter
- Gesture recognition
- Bluetooth Earphone



Product Overview

The da230 sensor is a special accelerometer sensor for bluetooth earphone application. Its ultra-low power consumption and ultra-small package can completely meet the needs of the bluetooth earphone market.

The device features user selectable full scale of ±2g/ ±4g/ ±8g/ ±16g measurement range with data output rate from 1Hz to 1000Hz with signal condition, step counter and step detection embedded.

The da230 has an integrated 32-level first-in, first-out (FIFO) buffer allowing the user to store data in order to limit intervention by the host processor.

Two independent and flexible interrupts provided greatly simplify the algorithm for bluetooth earphone tap gestures detection. Standard I^2C and SPI interfaces are used to communicate with the chip.

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1. Block diagram and pin description

1.1. Block diagram

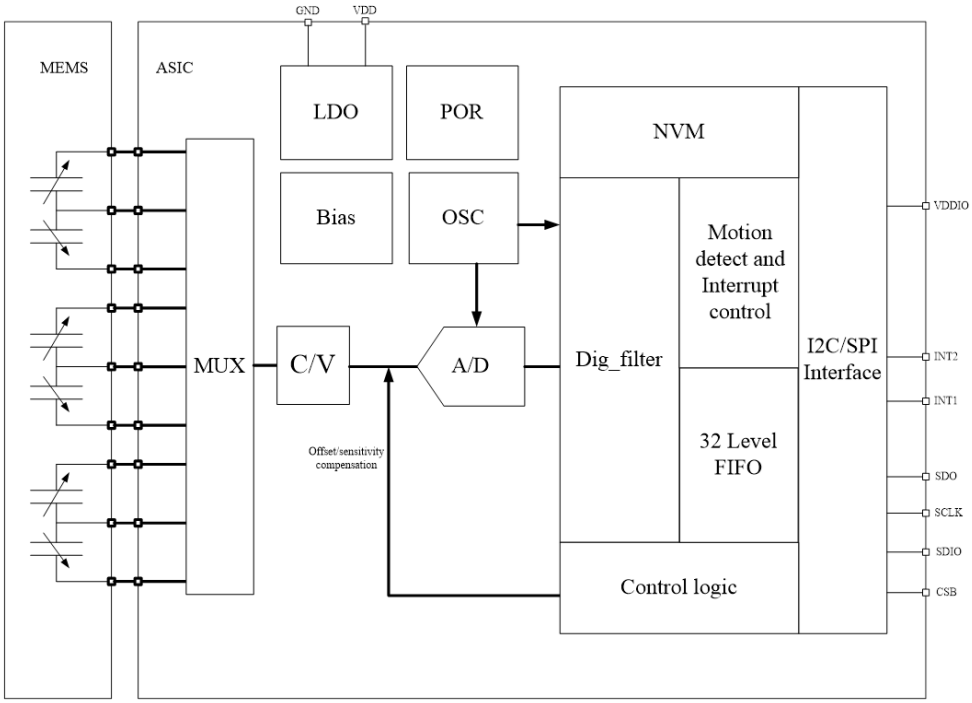


Figure 1 Block Diagram

1.2. Pin description

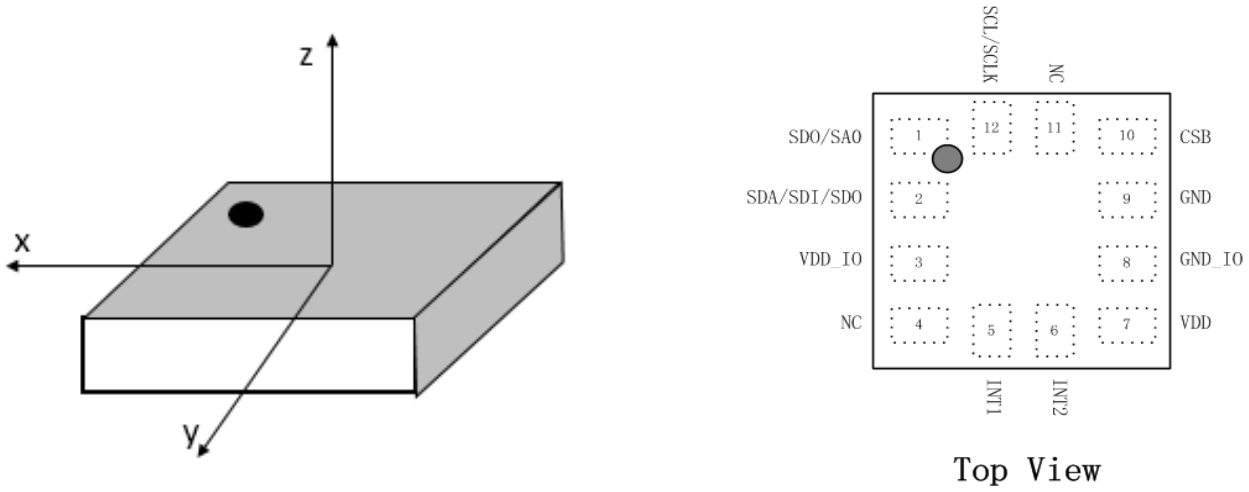


Figure 2 Pin description

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Table 1.Pin description

Pin#	Name	I/O Type	Function
1	SDO SA0	Digital out Digital in	SPI(4-wire mode) serial data output (SDO) I2C less significant bit of the device address (SA0) When using the I2C communication: SA0 must be connected to VDDIO or keep floating
2	SDA SDI SDO	Digital in/out	I2C serial data input/output(SDA) SPI(4-wire mode) serial data input (SDI) 3-wire interface serial data input/output (SDO)
3	VDD_IO	Supply	Power supply for I/O pins
4	NC	--	NO internal connection
5	INT1	Digital out	Interrupt pin1 (recommend used for tap interrupt)
6	INT2	Digital out	Interrupt pin2
7	VDD	Supply	Power supply
8	GND_IO	Ground	Ground supply for I/O pins
9	GND	Ground	Ground supply
10	CSB	Digital in	Chip select for SPI When using the I2C communication: CSB pin must be connected to VDDIO or keep floating
11	NC	--	NO internal connection
12	SCL SCLK	Digital in	I2C serial clock (SCL) SPI serial clock (SCLK)

NOTE: NC- NO internal connection

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2. Mechanical and electrical specifications

2.1. Mechanical characteristics

VDD = 2.5 V, T = 25 ℃ unless otherwise noted.

Table 2.Mechanical characteristic

Symbol	Parameter	Test conditions	Min	Type	Max	Unit
FS	Measurement range	FS bit set to 00		±2		g
		FS bit set to 01		±4		g
		FS bit set to 10		±8		g
		FS bit set to 11		±16		g
So	Sensitivity	FS bit set to 00		4096		LSB/g
		FS bit set to 01		2048		LSB/g
		FS bit set to 10		1024		LSB/g
		FS bit set to 11		512		LSB/g
TCSo	Sensitivity change vs. temperature	FS bit set to 00		±0.01		%/℃
Tyoff	Typical zero-g level offset accuracy			±70		mg
Tcoff	Zero-g level change vs. temperature	Max delta from 25℃		±0.6		mg/℃
Noise	XYZ RMS noise	FS bit set to 00, normal mode，BW = 100Hz		1		mg
Top	Operation temperature range		-40		85	℃

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2.2. Electrical characteristics

Vdd = 2.5 V, T = 25 ℃ unless otherwise noted

Table 3.Electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
VDD	Supply voltage		1.62	2.5	3.6	V
VDD_IO	I/O Pins supply voltage		1.62		VDD	V
IDD	current consumption in normal mode	Top=25℃, ODR=125Hz,		12.8		uA
IDD_SM	current consumption in suspend mode	Top=25℃		1		uA
TVDD	VDD&VDDIO power up time				100	ms
VIH	Digital high level input voltage	SPI&I2C	0.7*Vdd_IO			V
VIL	Digital low level input voltage	SPI&I2C			0.3*Vdd_IO	V
VOH	high level output voltage		0.9*Vdd_IO			V
VOL	Low level output voltage				0.1*Vdd_IO	V
BW	System bandwidth		100		500	Hz
ODR	Output data rate		1		1000	Hz
TWU	Wake-up time	From stand-by		1		ms
TSU	Start-up time	From power off		3		ms
PSRR	Power Supply Rejection Rate	Top=25℃			20	mg/V

2.3. Absolute maximum ratings

Stresses below those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 4.Absolute maximum ratings

Parameter	Test conditions	Min	Max	Unit
Storage Temperature		-45	125	℃
Supply Voltage VDD	Supply pins	-0.3	4.25	V
Supply Voltage VDD_IO	Logic pins	-0.3	Vdd_IO+0.3	V
ESD Rating	HMB,R=1.5k,C=100pF		±2	kV
Mechanical Shock	Duration<200us		10,000	g

Note: *Supply voltage on any pin should never exceed 4.25V*

This is a mechanical shock sensitive device, improper handling can cause permanent damages to the part.

This is an ESD sensitive device, improper handling can cause permanent damages to the part.

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3. Functionality

3.1. Functionality

3.1.1. Power mode

The da230 has two different power modes: normal and suspend mode.

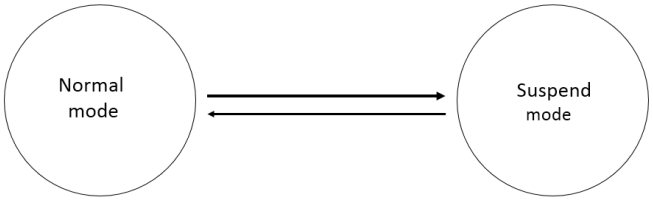


Figure 3 power mode

In the normal mode, the device is periodically switching between a sleep phase and a wake-up phase. During the wake-up phase, if an enabled interrupt is detected, the device stays in the wake-up phase as long as the interrupt condition endures (non-latched interrupt), or until the latch time expires (temporary latched interrupt), or until the interrupt is reset (latched interrupt). If no interrupt detected, the device enters the sleep phase.

Suspend mode: power-down mode, which is only support I2C and SPI interface.

3.1.2. Sensor data

The width of acceleration data is 14bits given in two's complement representation. The 14bits for each axis are split into an MSB part (one byte containing bits 13 to 6) and an LSB lower part (one byte containing bits 5 to 0).

3.1.3. Factory calibration

The IC is factory calibrated for sensitivity (So) and Zero-*g* level (TyOff). The trimming values are stored inside the chip's nonvolatile memory. The trimming parameters are loaded to registers while da230 reset (POR or software reset). This allows using the device without further calibration.

3.2. Interrupt controller

Interrupt engines are integrated in the da230. Each interrupt can be independently enabled and configured. If the condition of an enabled interrupt is fulfilled, the corresponding status bit is set to 1 and the selected interrupt pin is activated. There are two interrupt pins, INT1 and INT2; interrupts can be freely mapped to any of these two pins. The pin state is a logic 'or' combination of all mapped interrupts.

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3.2.1.Active detection

Active detection uses the slope between successive acceleration signals to detect changes in motion. An interrupt is generated when the slope (absolute value of acceleration difference) exceeds a preset threshold. The threshold can be configured by register.

3.2.2.Tap detection

Tap detection has a functional similarity with a common laptop touch-pad or clicking keys of a computer mouse. A tap event is detected if a pre-defined pattern of the acceleration slope is fulfilled at least for one axis. Two different tap events are distinguished: A single tap is a single event within a certain time, followed by a certain quiet time. A double tap consist a first such event followed by a second event within a defined time.

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4. Digital blocks

4.1. FIFO

The da230 embeds 32-level of 12-bit data FIFO for each of the three output channels, X, Y and Z of the acceleration module that can be used to minimize host processor burden. This buffer has four modes: bypass, FIFO, stream, and trigger.

4.1.1. Bypass Mode

In bypass mode, FIFO is not operational and, therefore, remains empty.

4.1.2. FIFO Mode

In FIFO mode, acceleration data of the x, y, and z-axes are stored in FIFO. When the number of samples in FIFO equals the level specified in the watermark sample register, the watermark interrupt is set. FIFO continues accumulating samples until it is full and then stops collecting data. After FIFO stops collecting data, the device continues to operate; therefore, features such as tap detection can be used after FIFO is full. The watermark interrupt continues to occur until the number of samples in FIFO is less than the value stored in the watermark sample register.

4.1.3. Stream Mode

In stream mode, acceleration data of the x, y, and z-axes are stored in FIFO. FIFO continues accumulating samples and holds the latest 32 samples from measurements of the x, y, and z-axes, discarding older data as new data arrives. The watermark interrupt continues occurring until the number of samples in FIFO is less than the value stored in the watermark sample register.

4.1.4. Trigger Mode

In trigger mode, FIFO accumulates samples, holding the latest 32 samples from measurements of the x, y, and z-axes. After an enable interrupt event occurs, FIFO keeps the last n samples and then operates in FIFO mode, collecting new samples only when FIFO is not full. Additional trigger events cannot be recognized until the trigger mode is reset. To reset the trigger mode, set the device to bypass mode and then set the device back to trigger mode. Note that the FIFO data should be read first because placing the device into bypass mode clears FIFO.

4.2. Embedded functions

The da230 embeds internal logic able to implement the following function:

- Step counter
- Step detector

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4.2.1.Step counter

When step counter is enable, the step counter counts the number of the steps, and recognize out the current status of walk or run.

4.2.2.Step detector

When step counter is enable and step detector interrupt is enable ,the step detector function generates an interrupt when a step is recognized.

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5. Application hints

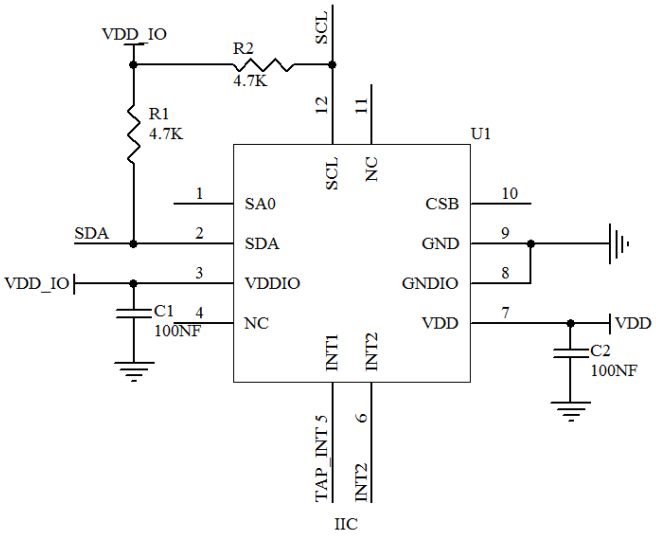


Figure 4 da230 I2C electrical connect

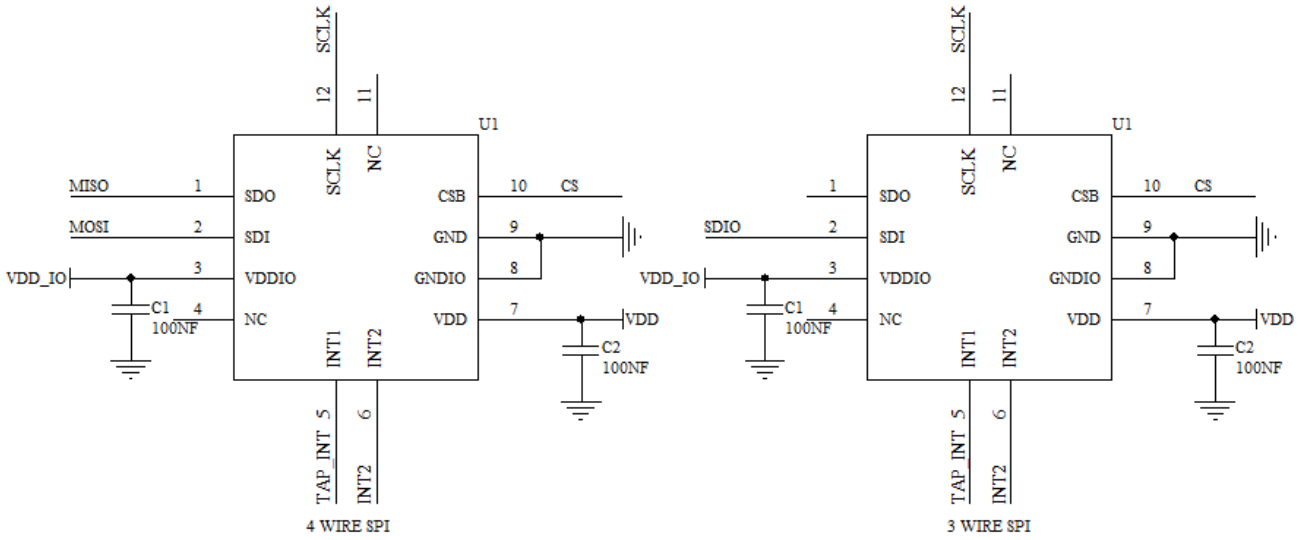


Figure 5 da230 SPI electrical connect

The device core is supplied through VDD line while the I/O pads are supplied through VDD_IO line. Power supply decoupling capacitors (100 nF ceramic) should be placed as near as possible to the pin 7 and pin 3 of the device (common design practice).

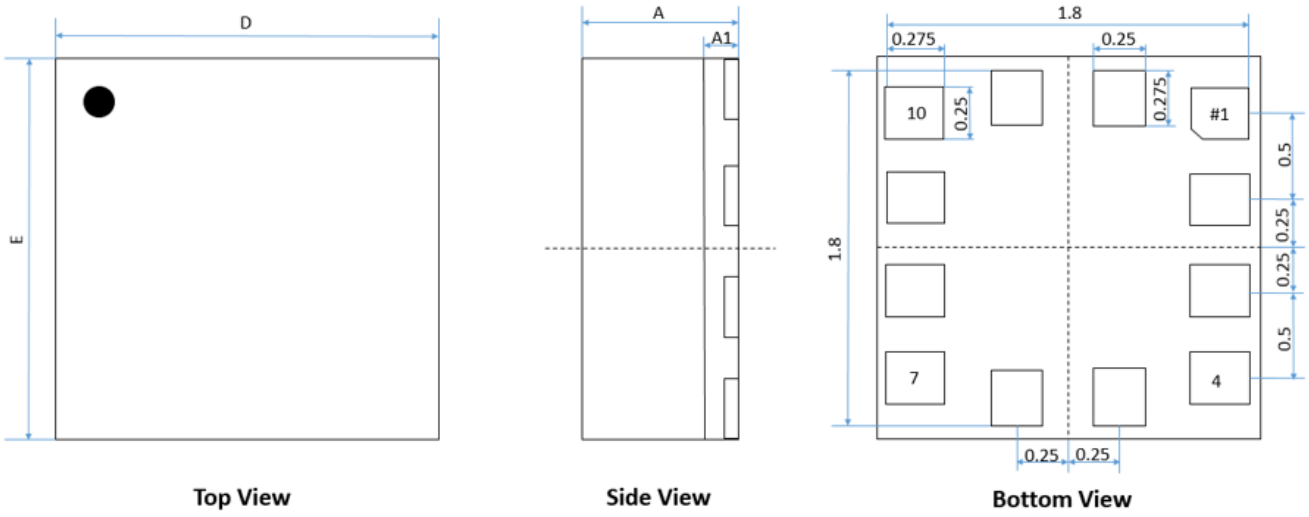
The functionality of the device and the measured acceleration data is selectable and accessible through the I2C or SPI interfaces. When using the I2C, CS must be tied high or keep floating. The functions, the threshold and the timing of the two interrupt pins (INT1 and INT2) can be completely programmed by the user through the I2C/SPI interface.

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6. Package information

6.1. Outline dimensions

The sensor housing is a standard LGA package. Its dimensions are the following.



COMMON DIMENSIONS(MM)			
PKG.	W:VERYVERY THIN		
REF.	MIN.	NOM.	MAX
A	0.82	0.9	0.98
A1(SUBSTRATE)	200 REF.		
D	1.9	2	2.1
E	1.9	2	2.1

Figure 6 12Pin LGA Mechanical data and package dimensions

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6.2. Landing pattern recommendation

For the design of the landing patterns, we recommend the following dimensioning:

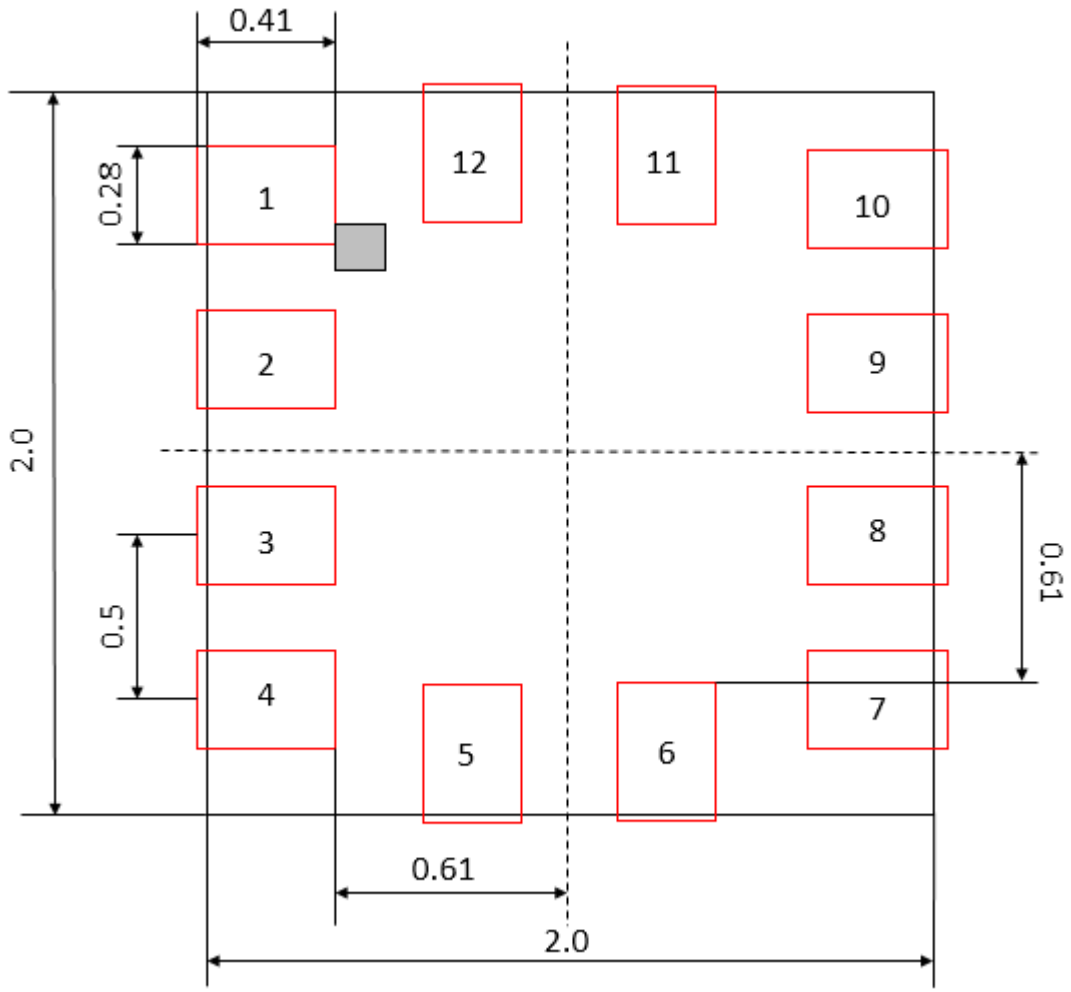


Figure 7 landing patterns; dimensions in mm

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6.3. Tape and reel specification

The da230 is shipped in a standard pizza box

The box dimension for 1 reel is: L x W x H = 35cm x 35cm x 5cm

The da230 quantity: 5000pcs per reel, please handle with care.

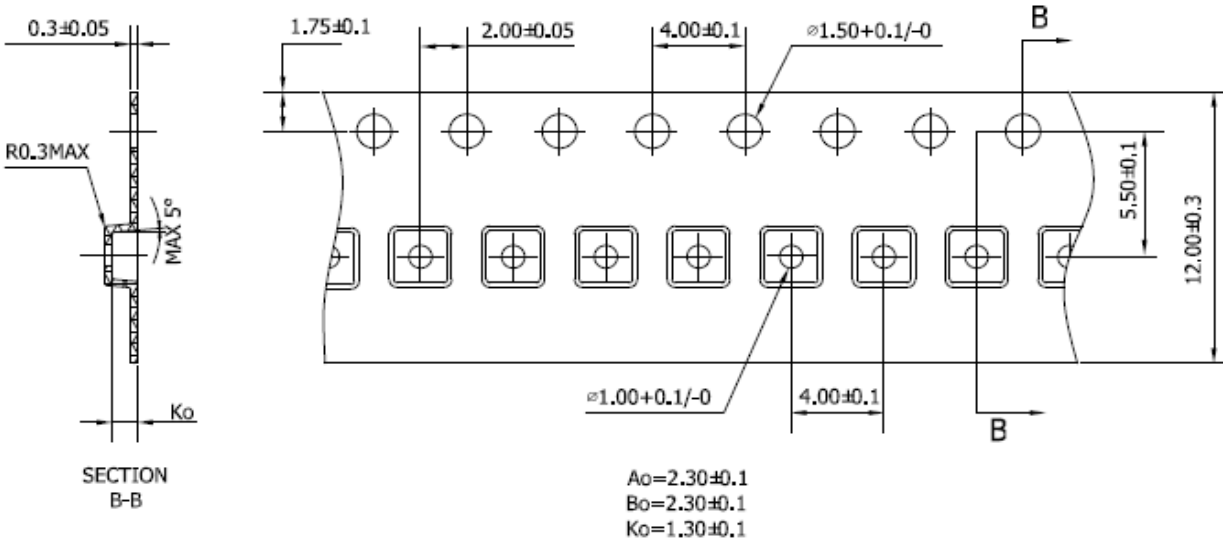


Figure 8 Tape and reel dimension in mm

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7. Reliability

The qualification condition of MiraMEMS's products is based on the stress test qualification for integrated circuits, JEDEC JESD47H.01 Standard. The test summary is listed below.

Table 5.Accelerated Life Tests

Test	Condition	Qty/lot	Lot	Acc/Rej	Result
High Temperature Storage (HTS)*	150C, 1000hrs JEDEC JESD22-A103D Condition A	77	3	0/1	PASS
High Temperature Operating Life Test (HTOL)*	125C, 1000hrs, 3.63V biased JEDEC JESD22-A108D	77	3	0/1	PASS
Highly Accelerated Stress Test (uHAST)*	130C/85%, 96hrs JEDEC JESD22-A118A Condition A	77	3	0/1	PASS

*Tests are preceded by MSL3 preconditioning in accordance with JEDEC JESD22-A113F

Table 6.Component Level Tests

Test	Condition	Qty/lot	Lot	Acc/Rej	Result
Preconditioning(MSL3)	24hrs HTSL (125C) ->192Hrs WHTSL (30C/60%RH) + 3x PbFree Reflow, 260C max JEDEC JESD22-A113F	77	3	0/1	PASS
Temperature Cycle*	-40C~85C (air to air) 500 cycles JEDEC JESD22-A104D Condition N	77	3	0/1	PASS
Shock Test	10000G/0.2ms, X/Y/Z 5 time/ direction JEDEC JESD22-B104C	10	3	0/1	PASS
Vibration Test	sweep 20-2000Hz, 4 times/direction JEDEC JESD22-B103B Condition 1 60Hz_32h/direction	10	2	0/1	PASS
ESD Susceptibility	2000V (HBM) JEDEC JS-001-2012	6	1	0/1	PASS
	200V (MM) JEDEC JESD22-A115C	6	1	0/1	PASS
	500V (CDM) JEDEC JESD22-C101E	6	1	0/1	PASS
Latch-up	>+/-2Vcc, max >+/-2Icc, max JEDEC JESD-78D	6	1	0/1	PASS

*Tests are preceded by MSL3 preconditioning in accordance with JEDEC JESD22-A113F

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8. Revision history

Table 7.Document revision history

Date	Revision	Changes
13-Apr.-2018	0.1	Initial release

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