IST8310

3D Magnetometer

Datasheet

本规格书由 铄泓科技 SH-MEMS 提供 · 联系人:李生 13632956297 · shop.sh-mems.com

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1 General Description

iSentek IST8310 is a 3-axis digital magnetometer with 3.0x3.0x1.0mm^3, 16-pin LGA package. It is an integrated chip with 3-axis magnetic sensors, digital control logic, built-in temperature compensation circuit and self-test function. IST8310 provides an I^{2}C digital output with fast mode up to 400kHz. The high output data rate, ultra-low hysteresis, excellent temperature drift and low noise performance feathers make it a perfect candidate for high accuracy applications.

Features

- Single chip 3-axis magnetic sensor
- 3.0x3.0x1.0mm^3, 16-pin LGA package
- I^{2}C slave, Fast Mode up to 400kHz
- 14 bits data output
- Wide dynamic range of ±1600uT (x, y-axis) and ±2500uT (z-axis)
- High output data rate of maximum 200Hz
- Ultra-low hysteresis (<0.1%FS)
- Ultra-low sensitivity temperature drift (±0.016 %/ ^{o}K)
- Ultra-low offset temperature drift (0.024uT/ ^{o}K)
- Wide operating temperature range
- High precision temperature compensation
- Built-in self-test function
- Software and algorithm support available (For tilt compensation, cross-axis compensation and noise suppression)

Applications

Quadcopter/Drone Applications
Augmented Reality Applications
Virtual Reality Applications
Location Based Services
Navigation Applications
Industrial Applications
Magnetometry
IOT devices
Heading
Gaming

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2 Block Diagram, Package Dimension and Application Circuit

2.1 Block diagram

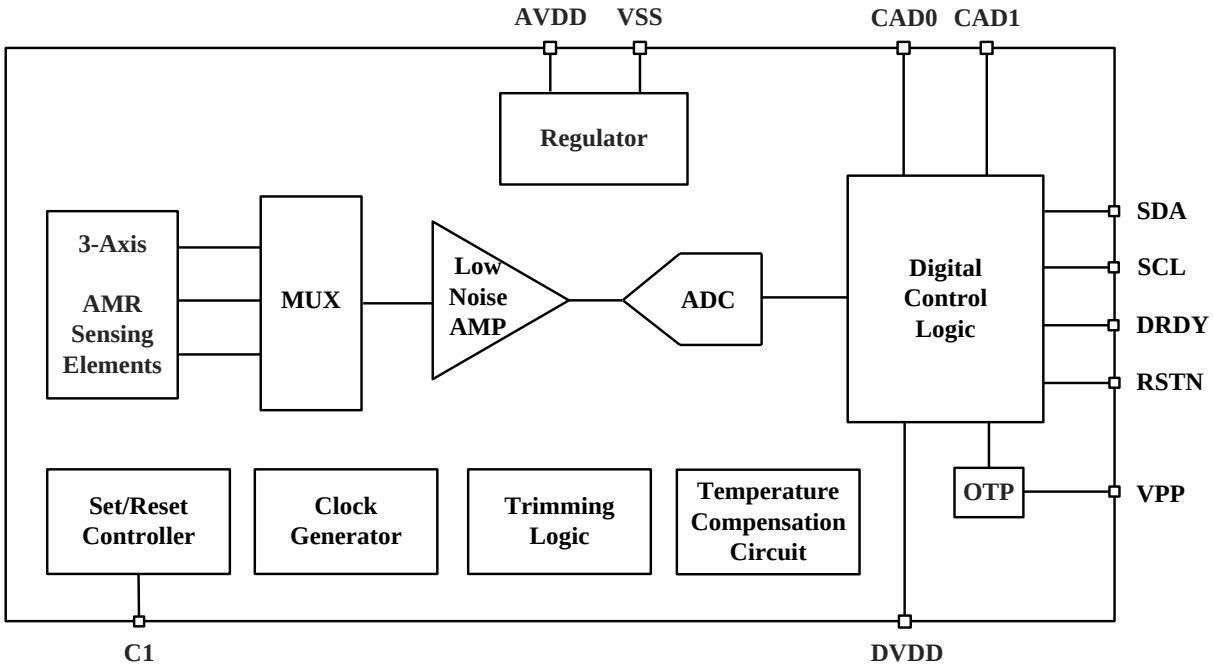
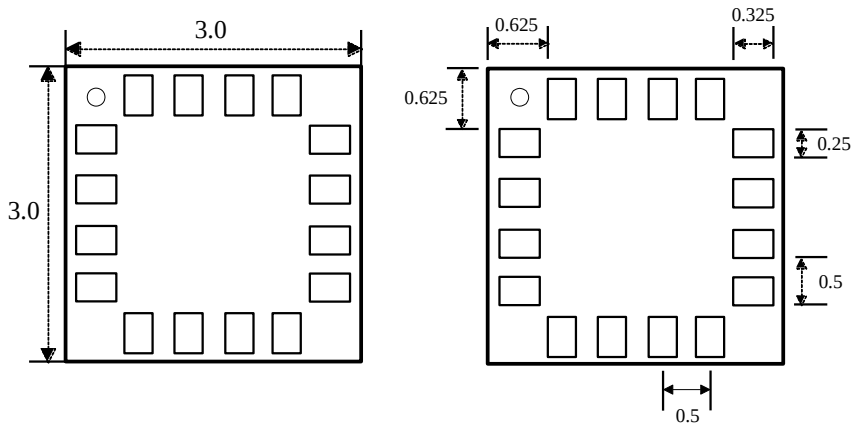


Figure 1. Block Diagram

2.2 Package Dimensions and Pin Description

IST8310 LGA Top View (Looking Through)



Unit: mm

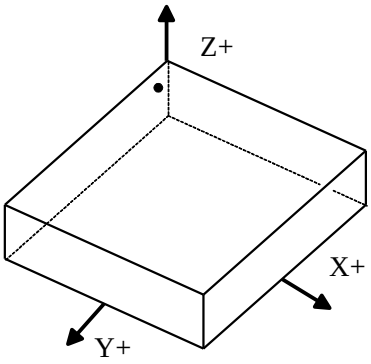
Tolerance: ±0.1mm

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IST8310 LGA Side View



IST8310 3D Top View



Unit: mm

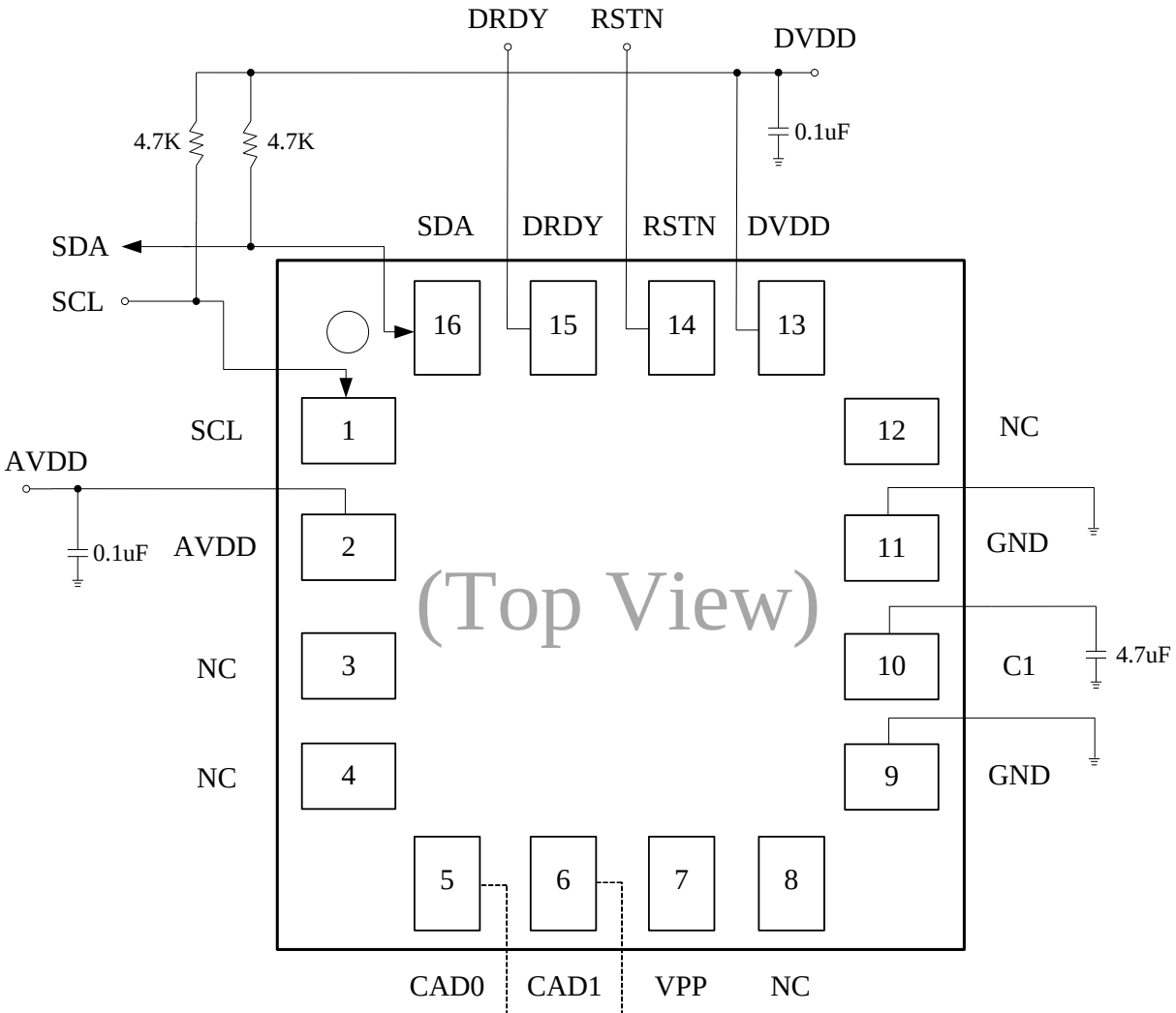
Tolerance: ±0.1mm

Pin	Name	Function
1	SCL	I^2C serial clock
2	AVDD	Analog supply voltage, 1.72~3.6V
3	NC	Not use
4	NC	Not use
5	CAD0	I^2C slave address
6	CAD1	I^2C slave address
7	VPP	Test pin, floating connection is suggested
8	NC	Not use
9	VSS	GND
10	C1	Set/Reset function, 4.7uF
11	VSS	GND
12	NC	Not use
13	DVDD	Digital supply voltage, 1.72~3.6V
14	RSTN	Reset pin, resets registers by setting it to “Low”. Internally pulled to “High” for floating connection. MCU connection is suggested (but not necessary).
15	DRDY	Data ready indication, output pin only
16	SDA	I^2C serial data

*please refer to Figure 2.

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2.3 Application Circuit



Slave Address Select

CAD1	CAD0	Address (7-bit)	Address (8-bit)
VSS	VSS	0CH	18H
VSS	VDD	0DH	1AH
VDD	VSS	0EH	1CH
VDD	VDD	0FH	1EH

*if CAD1 and CAD0 are floating, I^2C address will be 0EH/1CH.

Figure 2. Application Circuit

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3 Operational Modes and Functional Descriptions

3.1 Operation modes

IST8310 has following operation modes:
(1) Stand-By Mode
(2) Single Measurement Mode
(3) Self-Test Mode

3.1.1 Stand-By Mode

The initial mode (after power on) of IST8310 is Stand-By Mode. In Stand-By Mode, all internal circuits are off (except oscillator and regulator). All registers can be accessed in Stand-By Mode. Data stored in Read/Write registers remains as last state. Registers can be reset by soft reset or hard reset (through RSTN pin).

As initial setting, please set Pulse Duration Control Register, PDCTNL(0x42) = 11000000b (C0H) for performance optimization. For low noise performance, please set Average Control Register, AVGCNTL(0x41) = 00100100b (24H) for more internal average times. The minimum waiting time between two measurements under low noise performance setup is 6ms (166Hz).

3.1.2 Single Measurement Mode

In Single Measurement Mode, the measured data is stored in data registers then IST8310 transits to Stand-By Mode automatically. On transition to Stand-By Mode, Control register 1(CNTL1[3:0]) turns to “0000”. At the same time, DRDY bit in STAT1 register turns to “1”. This is called “data ready”. When any of the measurement data registers or STAT2 register is read, DRDY bit turns to “0”. For the next measurement, user needs to set Control register 1(CNTL1[3:0]) to “0001” again. The minimum waiting time between two measurements in default setup is 5ms (200Hz).

Please noted in IST8310, ultra-low noise performance is obtained through soft-averaging in driver. Please contact iSentek for technical details.

3.1.3 Self-Test Mode

Self-Test mode is used to check if the 3-axis outputs read in Single Measurement Mode are correct. It is activated by setting Self-Test Register (0x0C) to 40h; then all 3-axis outputs will change their polarity. User can check the 3-axis output values before and after activating Self-Test Mode; if the absolute values are the same, then the IC is working correctly. It can be turned off by setting Self-Test Register (0x0C) to 00h.

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3.2 Interrupt Function

Interrupt function is used when there is a huge external magnetic field in the surrounding. When the absolute sum of measured 3-axis output value exceeds 1600 uT, the INT flag is activated. The INT flag can be found in STAT2 register.

3.3 DRDY Function

DRDY function is used when the output data is updated. The DRDY pin is used to monitor the data ready output. DRDY is changed to low after reading data from the output register.

3.4 IST8310 Read Process

(1) Read STAT1 register:

- Polling STAT1 register bit 0
- DRDY: shows if the data is ready or not

  0: no data ready

  1: data ready
- DOR: shows if any data has been skipped before the current data

  0: no skipped data

  1: data skipped.

(2) Read Measurement Data:

Read Register 0x03h~0x08h for X, Y and Z axis data. When data reading starts, DRDY bit and DOR bit turn to “0”.

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4 Electrical Specifications

4.1 Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
Storage Temperature	TSTG	-40 to +125	°C
Operating Temperature	TA	-40 to +85	°C
Analog Supply Voltage	AVDD	-0.5 to +3.6	V
Digital Supply Voltage	DVDD	-0.5 to +3.6	V
Digital Input Voltage	VIN	-0.3 to DVDD+0.3	V
Electrostatic Discharge Voltage*[1]	VESD_HBM	-4000 to 4000	V
Electrostatic Discharge Voltage*[2]	VESD_MM	-350 to 350	V
Reflow Classification	JESD22-A113 with 260 °C Peak Temperature		

1. Human Body Model (HBM)
2. Machine Model (MM)

4.2 Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Temperature	TA	-40		+85	°C
Analog Supply Voltage	AVDD	1.72	2.8	3.6	V
Digital Supply Voltage	DVDD	1.72	1.8	3.6	V

4.3 Electrical Specifications

(Operating conditions: TA=+25℃; AVDD=2.8V; DVDD=1.8V; 0.1μF ceramic capacitors **tied closely** to AVDD/DVDD and GND respectively.)

Parameter	Symbol	Conditions	Min.	Typ.	Max	Unit
Operating Current	IDD3A	Full operation, at				uA
		1 sps		20		
		8 sps		72		
		10 sps		80		
		20 sps		140		
		50 sps		320		
		100 sps		600		
		200 sps		1200		
Standby Current	ISTB			10		uA

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Output Data Rate (ODR)	ODR		1		200	Hz
Input Low Voltage	VIL		0		DVDD *30%	V
Input High Voltage	VIH		DVDD *70%		DVDD	V
Output Low Voltage	VOL	IOL= +4 mA	0		DVDD *20%	V
Output High Voltage	VOH	IOH= -100 uA (Except SCL and SDA)	DVDD *80%		DVDD	V

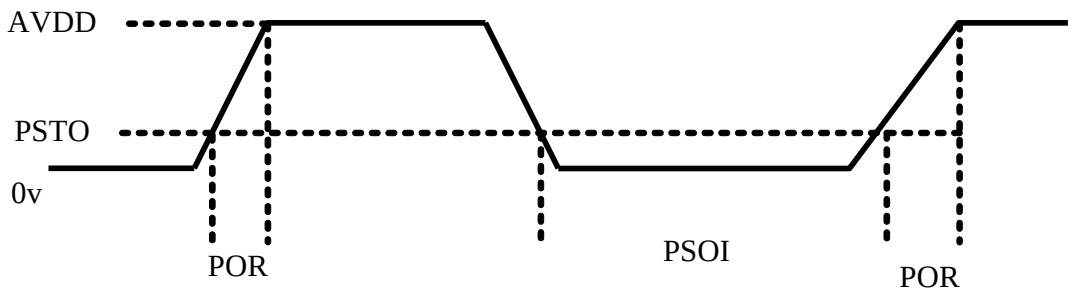
4.4 Magnetic Sensor Specifications

(Operating conditions: Ta=+25℃; AVDD=2.8V; DVDD=1.8V; 4.7μF ceramic capacitors **tied closely** to C1 and GND respectively.)

Parameter	Symbol	Condition	Min.	Typ.	Max	Unit
Dynamic Range	MDR_XY	TA=25 °C		±1600		uT
	MDR_Z	TA=25 °C		±2500		
Linearity	LIN	X-axis		1	1.5	%FS
		Y, Z-axis		0.1	0.5	
Resolution	RESO			0.3		uT/LSB
Sensitivity	SEN			3.3		LSB/uT
Zero Gauss Offset	ZGD	RMS value		±0.3		uT
Hysteresis	HS			0.1		%FS
Sensitivity Temperature Drift	TD_S	-40 ~ 85 °C		±0.016		%/ °K
Zero-B Offset Temperature Drift	TD_O	-40 ~ 85 °C		0.024		uT/ °K

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4.5 Power On Reset (POR) Specifications



PSTO: Power Supply Turn Off voltage	PSTO: max=0.1volt
PSOI: Power Supply Turn Off Interval	PSOI: min=10ms
POR: Power On Reset	POR: max:50ms

When POR circuit detects the rise of AVDD voltage, it resets all internal circuits and initializes all registers. After reset, IST8310 transits to Stand-By mode.

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5 Technology Overview

5.1 AMR Technology

IST8310, an iSentek patented magnetometer is designed based on Anisotropy Magneto-Resistance (AMR) technology. The output is generated from the resistance change of the AMR resistors while external magnetic field changes. The sensitivity is about 50 to 200 times larger than traditional Hall element. The high sensitivity allows higher output data rate (ODR), lower noise and lower power consumption.

5.2 High Reliability Planarized Structure Design

IST8310 consists of three full Whetstone Bridge of AMR resistors. The three bridges detecting magnetic component in three directions orthogonal to each other are located on one chip, wire-bonded to a control ASIC. This planarized structure design enables outstanding stability to thermal shock, making our device highly reliable, immune from thermal reflow-induced failure. While other known AMR magnetometers placing z-axis sensor vertical to the substrate using 90-degree flip-chip packaging suffers from reliability issues

5.3 Ultra-low Hysteresis Design

iSentek has developed a specialized high permeability (μ) material for magnetic field detection. This high-μ material has ultra-low residual magnetization below 0.1 %FS in the field range as large as +/- 500 G. The ultra-low hysteresis design prevents the magnetometer from dynamic offset after encountering a strong external magnetic field impact; that is, the angular accuracy restores automatically without calibration after the removal of interference field. This feature fulfills the requirements for applications when real time calibration is not available. No calibration is required in general conditions.

5.4 Magnetic Setting Mechanism

AMR sensing resistors consist of Permalloy thin film and metallization. Permalloy is soft magnetic, irreversible magnetic rotation may occur after the strength of external magnetic field exceeds half of the anisotropy field of the sensing resistor, resulting in angular error induced by offset. To solve this issue, a magnetic setting mechanism is introduced in IST8310. A magnetic field is generated within IST8310 to align the magnetization of AMR sensing resistors before every measurement. This auto-zeroing mechanism ensures the stability of angular accuracy of IST8310 during whole operation.

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6 Digital Interface and Registers

6.1 I²C Interface

The interface of IST8310 follows the standard I²C definition guidelines with some additional protocol definitions. IST8310 supports standard speed (100kHz) and fast speed (400kHz). Pull-up resistors of 4.7kohm for both SDA and SCL lines should be used.

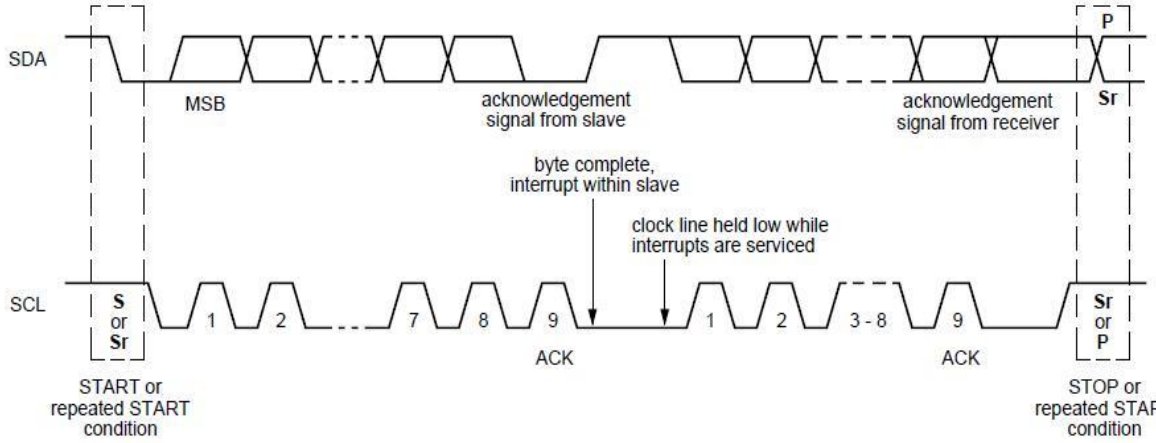


Figure 3. I²C Operation

6.1.1 Slave Address

MSB LSB

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	1	1	selectable	selectable	R/W

IST8310 has 4 different I²C slave addresses, which can be chosen through Pin 5 (CAD0) and Pin 6 (CAD1), the corresponding 7-bit and 8-bit defined I²C slave addresses are listed below:

CAD1	CAD0	I²C Slave Address (7-bit)	I²C Slave Address (8-bit)
VSS	VSS	0CH	18H
VSS	VDD	0DH	1AH
VDD	VSS	0EH	1CH
VDD	VDD	0FH	1EH
Floating (default)	Floating (default)	0EH	1CH

6.2 I²C Read Operation

Single Byte Read:

SA	Slave Address+ RW	ACK	Reg Address	ACK	SP	Slave Address+RW	ACK	DATA	NA	ST

Figure 4. I²C Single Byte Read Operation

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ACK: Acknowledge, NA: Not Acknowledge, SA: START Condition, SP: Repeat Start Condition, ST: STOP Condition

■: Slave to Master □: Master to Slave

Multiple Byte Read:

SA	Slave Address+ RW	ACK	Reg Address	ACK	SP	Slave Address+RW	ACK	DATA	ACK	DATA	NA	ST

Figure 5. I²C Multiple Byte Read Operation

ACK: Acknowledge, NA: Not Acknowledge, SA: START Condition, SP: Repeat Start Condition, ST: STOP Condition

■: Slave to Master □: Master to Slave

6.3 I²C Write Operation

Single Byte Write:

SA	Slave Address +RW	ACK	Reg Address	ACK	DATA	ACK	ST

Figure 6. I²C Single Byte Write Operation

ACK: Acknowledge, NA: Not Acknowledge, SA: START Condition, SP: Repeat Start Condition, ST: STOP Condition

■: Slave to Master □: Master to Slave

Multiple Byte Write:

SA	Slave Address +RW	ACK	Reg Adderss	ACK	DATA	ACK	DATA	NA	ST

Figure 7. I²C Multiple Byte Write Operation

ACK: Acknowledge, NA: Not Acknowledge, SA: START Condition, SP: Repeat Start Condition, ST: STOP Condition

■: Slave to Master □: Master to Slave

6.4 Registers

6.4.1 Customer Defined Registers

Register name	**Typ**	**I²C Addr**	**Size (bit)**	**Info**
Who am I	R	00h	8	Device ID
Status Register 1	R	02h	8	Data Status
Output Value X_L	R	03h	8	Low byte for X-axis data
Output Value X_H	R	04h	8	High byte for X-axis data
Output Value Y_L	R	05h	8	Low byte for Y-axis data
Output Value Y_H	R	06h	8	High byte for Y-axis data
Output Value Z_L	R	07h	8	Low byte for Z-axis data

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Output Value Z_H	R	08h	8	High byte for Z-axis data
Status Register 2	R	09h	8	Data Status
Control Register 1	R/W	0Ah	8	Chip Control setting 1
Control Register 2	R/W	0Bh	8	Chip Control setting 2
Output Value T_L	R	1Ch	8	Low byte for Temperature data
Output Value T_H	R	1Dh	8	High byte for Temperature data

6.4.2 Who Am I Register

This Register provides device ID information

WAI (0x00)			
Bit	Description	Attr	Default
7:0	Device ID	R	10

6.4.3 Status Register 1

This Register provides status information of IST8310

STAT1 (0x02)			
Bit	Description	Attr	Default
7:2	Reserved		
1	DOR: Turns to 1 when data has been skipped. Bit is released after any output data register read 0: no data overrun 1: data overrun	R	0
0	DRDY: Data ready pin 0: data not ready 1: data ready This status bit follows physical signal appearance, expect the polarity control (refer to DRP bit in CNTL2 register) If data ready function enable bit is not set (refer to DREN bit in CNTL2 register), this bit is zero	R	0

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6.4.4 Output Data Registers

The Output Registers (from 0x03h~0x08h) contain X, Y and Z axis measurement data. Measurement data are stored in 2's complement format.

DATAXL(0x03)			
Bit	Description	Attr	Default
7:0	Low Byte of X-axis data	R	0

DATAXH(0x04)			
Bit	Description	Attr	Default
7:0	High Byte of X-axis data	R	0

DATAYL(0x05)			
Bit	Description	Attr	Default
7:0	Low Byte of Y-axis data	R	0

DATAYH(0x06)			
Bit	Description	Attr	Default
7:0	High Byte of Y-axis data	R	0

DATAZL(0x07)			
Bit	Description	Attr	Default
7:0	Low Byte of Z-axis data	R	0

DATAZH(0x08)			
Bit	Description	Attr	Default
7:0	High Byte of Z-axis data	R	0

6.4.5 Status Register 2

In this register, there is an INT flag for customer use.

STAT2(0x09)			
Bit	Description	Attr	Default

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7:4	Reserved		
3	INT : Interrupt bit. When interrupt event occurs, this bit will be set to 1	R	0
2:0	Reserved		

6.4.6 Control Setting Register 1

This Register controls and adjusts the main parameters.

CNTL1(0x0A)			
Bit	Description	Attr	Default
7:4	Reserved		
3:0	Mode: Operating mode setting 0000: Stand-By mode 0001: Single Measurement Mode Others: Reserved	R/W	0

6.4.7 Control Setting Register 2

This Register controls and adjusts the main parameters.

CNTL2(0x0B)			
Bit	Description	Attr	Default
7:4	Reserved		
3	DREN : Data ready enable control: 0: disable 1: enable Master switch for DRDY output pin	R/W	1
2	DRP: DRDY pin polarity control 0: active low 1: active high	R/W	1
1	Reserved		
0	SRST: Soft reset, perform Power On Reset (POR) routine 0: no action 1: start immediately POR routine This bit will be set to zero after POR routine	R/W	0

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6.4.8 Self-Test Register

STR(0x0C)			
Bit	Description	Attr	Default
7	Reserved		
6	SELF_TEST : When this bit set to 1, chip enters self-test mode	R/W	0
5:0	Reserved		

6.4.9 Temperature Sensor Output Registers

The Output Data Registers use 2's complement format.

TEMPL(0x1C)			
Bit	Description	Attr	Default
7:0	Low Byte of Temperature data	R	0

TEMPH(0x1D)			
Bit	Description	Attr	Default
7:0	High Byte of Temperature data	R	0

6.4.10 Average Control Register

This register controls the times of average done in the circuit to lower the noise. Higher average times leads to lower noise.

AVGCNTL(0x41)			
Bit	Description	Attr	Default
7:6	Reserved.	R/W	0
5:3	Average times for y sensor data. Times of average will be done before switch to next channel 3'b000 no average 3'b001 average by 2 times 3'b010 average by 4 times (Default) 3'b011 average by 8 times 3'b100 average by 16 times	R/W	0

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	Others: no average		
2:0	Average times for x & z sensor data. Times of average will be done before switch to next channel 3'b000 no average 3'b001 average by 2 times 3'b010 average by 4 times (Default) 3'b011 average by 8 times 3'b100 average by 16 times Others: no average	R/W	0

6.4.11 Pulse Duration Control Register

This register controls the pulse duration for set/reset function of AMR sensors.

PDCNTL(0x42)			
Bit	Description	Attr	Default
7:6	Pulse duration: 2'b01 Long 2'b11 Normal (please use this setting) Others: only for extreme cases	R/W	0
5:0	Reserved.	R/W	0

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7 Ordering Information

Order Number	Package Type	Packaging	Marking Information
IST8310	LGA – 16 pin	Tape and Reel: 5k pieces per reel	$X_1X_2X_3$0 010● X_1: Last number of the year X_2X_3: Week number 010: Product code of IST8310

For more information on iSentek's Magnetic Sensors, please contact us by phone at +86-132-6706-8686 (China), +86-755-3337-0168 (China) or +886-2-2698-3306 ext:110 (Taiwan); via e-mail: sales@isentek.com or visit us online at www.isentek.com.

The application circuits herein constitute typical usage and interface of iSentek's product. iSentek does not warranty or assume liability of customer-designed circuits derived from this description or depiction.

iSentek reserves the right to make changes to improve reliability, function or design. iSentek does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights nor the rights of others.

US Patent 9,297,863, Taiwanese Patents I437249, I420128 and I463160 apply to our magnetic sensor technology described.

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