UX3361 Datasheet

10Gbps Burst mode Transceiver for XGPON Applications

General Description

UX3361 is a combined 10Gbps low power limiting amplifier, 2.5Gbps burst mode laser driver and a low-cost APD DC-DC booster for 10Gbps PON applications. The limiting amplifier can be operated in 10Gbps. The laser driver can be operated in 2.5Gbps burst mode and continuous mode. It can be set by IIC from external EEPROM or MCU. The UX3361 has DDM functions without external MCU. It can read and calibrate VCC, temperature, Ibias, transmitter power, receiver power.

Features

General

3.3V supply

Built-in DDMI function

Digital control through I2C interface

Integrated ADC/DAC and temperature sensor

4mm*4mm 32-pin QFN package

Laser driver

2.5Gbps Burst mode Transmitter

Bias current (I_{bias})up to 120 mA;

Modulation current (I_{mod})up to 120 mA;

Burst on/off time < 12.8 ns ;

TX SD delay time < 100ns;

Digital APC automatic control function;

Open loop with temperature look up table for Ibias and Imod;

Rogue ONU, long light emitting detection function;

LDD has low power mode (sleep mode);

Output pin LDOP/LDON of LDD has a built-in programmable filter circuit.

Limiting Amplifier

10 mV input sensitivity at 10Gbps;

Programmable input equalization

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Programmable output amplitude

Programmable output pre-emphasis

Polarity invert and output mute

Programmable LOS with adjustable threshold and hysteresis

Alarm delay latch function;

LA has low power mode (sleep mode).

Digital interface

Programmable IIC interface;

Build in Digital Diagnostic Monitor processor;

Device settings stored in external EEPROM;

PWM waveform output for DC-DC booster/DA output for APD control

Applications

10G XGPON ONU/ONT BoB designs;

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Pin Configuration

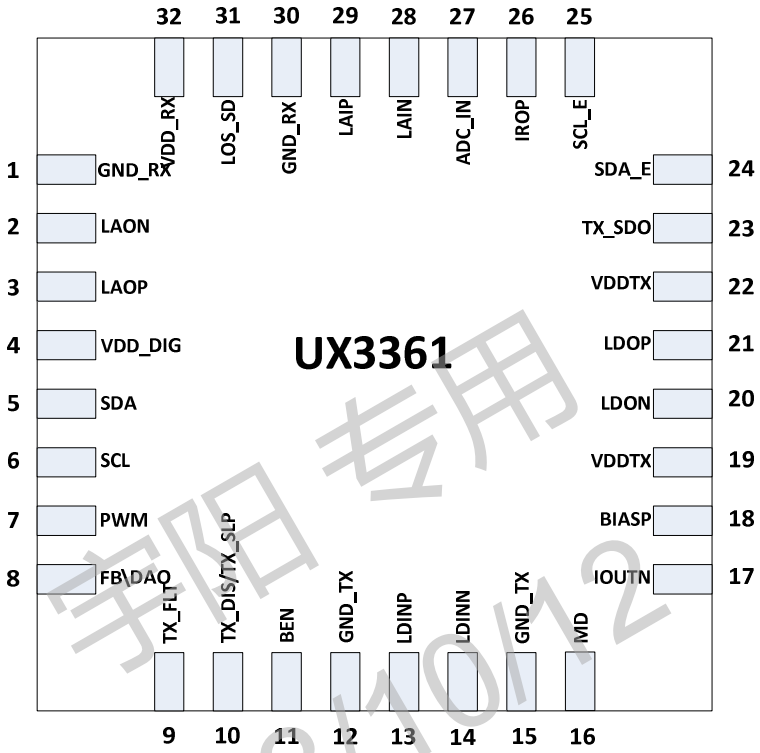


Figure 1-1. Pin Configuration QFN32

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1 Ordering Information

UX3361, QFN32, 4mm×4mm

2 Pin Description

Table 2-1: Pin Descriptions

PIN NO.	NAME	DESCRIPTION
1	GND_RX	Limiting Amplifier ground
2	LAON	Inverted Limiting Amplifier signal output
3	LAOP	Limiting Amplifier signal output
4	VDD_DIG	Digital power supply
5	SDA	IIC slave mode data interface

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6	SCL	IIC slave mode clock interface
7	PWM	Internal DC-DC convertor PWM control output. Connect to an external FET switch.
8	FB\DAO	Internal DC-DC convertor voltage feedback output. Can be used for iDAC;
9	TX_FLT	Transmitter fault alarm, external 4.7K~10K ohm pull-up
10	TX_DIS/TX_SLP	Transmitter disable, inner 20K ohm pull-up. Also used to enable sleep modes control input.
11	BEN	Burst enable control input.
12	GND_TX	Transmitter power ground
13	LDINP	Transmitter signal input
14	LDINN	Inverted transmitter signal input
15	GND_TX	Transmitter power ground
16	MD	Monitor photodiode input
17	IOUTN	Transmitter bias output in ben off. Connect a dummy load resistor to VDD_TX ;
18	BIASP	Transmitter bias output
19	VDD_TX	Transmit path output power supply
20	LDON	Inverted Transmitter signal output;Connect to Laser anode.
21	LDOP	Transmitter signal output;Connect to Laser cathode;
22	VDD_TX	Transmit path output power supply
23	TX_SDO	Transmit power output signal detect;
24	SDA_E	IIC master mode data interface
25	SCL_E	IIC master mode clock interface
26	IROP	ROSA input optical power monitor current input
27	ADC_IN	ADC inpuit, can be used to monitor APD voltage
28	LAIN	Inverted Limiting Amplifier signal input
29	LAIP	Limiting Amplifier signal input
30	GND_RX	Limiting Amplifier ground
31	LOS_SD	Limiting Amplifier signal lost alarm, external 4.7K~10K ohm pull-up
32	VDD_RX	Limiting Amplifier power supply

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3 Key Specifications

3.1 Absolute Maximum Ratings

Table 3-1: Absolute Maximum Ratings

Symbol	Parameter	Min.	Typical	Max.	Units.
VCC	Supply voltage	-0.5		4.5	V
T_{STO}	Storage temperature			150	℃
$T_{JUN\ MAX}$	Max junction temperature			150	℃
Tsolder	Soldering temperature		260		℃
ESD	HBM model	2			KV
ESD	CDM model	500			V

Device not guaranteed to meet specifications, permanent damage may be incurred by operating beyond these limits.

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3.2 Continuous Ratings

Table 3-2: Continuous Ratings

Symbol	Parameter	Min.	Typical	Max.	Units.
VCC	Supply voltage	2.97	3.3	3.63	V
ICC	Current consumption *		110		mA
T_{OPE}	Operating temperature	-40	25	95	℃
T_{JUN}	Junction temperature	-40		125	℃
Rja	junction to ambience thermal resistance		44.1		℃/W
Rjc	junction to case thermal resistance		21.58		℃/W
Rjb	junction to board thermal resistance		10.69		℃/W

*:AMPCTRL<2:0>=011, RX equalizer and pre-emphasis disabled, excluding 20mA bias and 20mA modulation current.

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3.3 Electrical Characteristics

Typical data rate= 10.3125Gbps;

Input pattern: PRBS31;

Typical values are for VDD_TX, VDD_RX=3.3V;

Temperature: 27℃

3.3.1 Limiting Amplifier

Table 3-3: Limiting Amplifier

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Data rate	DR			10		Gbps
Input sensitivity*	Vins	Differential	5	7	10	mVpp
Input impedance	Rin	Differential	90	100	110	Ohm
Output impedance	Rout	Differential	90	100	110	Ohm
Differential Output swing**	Vswing		350	600	1000	mVpp
Edge time*	Tr/Tf	20%~80%			35	ps
SD assert voltage range	Vth	Differential	6		100	mVpp
SD hysteresis	HYS		0.5	2	4	dB
SD de/assert time	SDt		12		100	us
Random jitter*	Rj				1.8	ps
Deterministic jitter*	Dj				12	ps

*: AMPCTRL<2:0>=011.

**: Measured using a 11110000 square wave pattern.

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3.3.2 Laser Diode Driver

Transmitter Inputs: LDIN/LDIP, BENN/BENP

Symbol	Parameter	Min.	Typ.	Max.	Units.
V_{ID}	Differential input swing	200		2400	mV
$V_{CM_IN/IP}$	common-mode voltage of input data	1200	0.6VDD	2700	mV
V_{CM_BEN}	common-mode voltage of BEN input		1.4		V
V_{BEN_H}	High voltage of BEN	2*			V
V_{BEN_L}	Low voltage of BEN			0.8*	V

*: If V_{CM_BEN} is changed by Chip external bias, for BEN logic high, V_{BEN_H} - V_{BEN_L} should ≥1.2V.

Table 3-4: Laser Diode Driver

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input amplitude range	VIN	Differential	100		1000	mVpp
DC voltage of input	VCM			1.2		V
Input terminal	RIN	Differential On chip	90	100	110	Ohm
Photodiode input sink current	IMD		0.025		1.5	mA
Maximum bias current	IBIASMAX		120			mA
Bias shutdown current	IBIASOFF				100	uA
Maximum modulation current	IMODMAX		120			mA
Modulation shutdown current	IMODOFF				100	uA
Equalization gain boost	EQBOOST		0		9	dB

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Crossing point adjustment	CPA		40		60	%
Total output Jitter	Tj			0.16		UIpp

3.3.3 Interface Signals

Table 3-5: Interface Signals

Symbol	Parameter	Min.	Typ.	Max.	Units.
V_{HIGH}	TX_Disable input high	2			V
V_{LOW}	TX_Disable input low			0.8	V
V_{FAULT_HIGH}	TX_Fault output high voltage	2			V
V_{FAULT_LOW}	TX_Fault output low voltage			0.8	V

3.3.4 Burst Mode Timings

Table 3-6: Burst Mode Timings

Symbol	Parameter	Min.	Typ.	Max.	Units.
$T_{BENONDELAY}$/ $T_{BENOFFDELAY}$	Burst enable/disable delay time, assertion of BEN to 90% of desired Ibias + Imod, de-assertion of BEN to 10% of settled Ibias + Imod			12.8	ns
T_{BENON}	Burst on time	200			ns
T_{BENOFF}	Burst off time	96			ns
T_{ON}	Time from power up to get target optical power, and fast start disabled, Apcfsst, table 80h, 83(7)h=0	24ns		50 ms	

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	Time from power up to get target optical power, and fast start enabled, Apcfsst, table 80h, 83(7)h =1		1.6		us
T_{TX_SDON}	Time from BEN on to TX_SDO high		80	100	ns
T_{TX_SDOFF}	Time from BEN off to TX_SDO low		80	100	ns

3.4 Safe Logic Timings

Table 3-7: Safe Logic Timings

Symbol	Parameter	Min.	Typ.	Max.	Units.
T_{INIT}	Time to initialize from power on or negation of TX_Fault using TX_Disable			100	ms
T_{ON}	Time from falling edge of TX_Disable to when the modulation optical output rises above 90% of nominal			1	ms
T_{OFF}	Time from rising edge of TX_Disable to when the optical output falls below 10% of nominal			10	us
T_{FAULT}	Time from fault to TX_Fault			10	us
T_{RESET}	Time TX_Disable must be held high to reset TX_Fault	10			us

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3.5 2-Wire Serial Interface

Table 3-8: 2-Wire Serial Interface

PARAMETER	SYMBOL	CONDITION	Min	Typ	Max	Unit
SCL clock frequency	F_{SCL}				400	KHz

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Low period of the SCL clock	T_{LOW}		1300			ns
High period of the SCL clock	T_{HIGH}		600			ns
Set-up time for start	$T_{SU:STA}$		600			ns
Hold time	$T_{HD:STA}$		600			ns
Data set-up time	$T_{SU:DAT}$		100			
Data hold time	$T_{HD:DAT}$	1	0			
Edge time	T_R/T_F				300	ns
Set-up time for stop	$T_{SU:STO}$		600			ns
Bus free time	T_{BUF}	Stop~start	1300			ns

NOTE:

1. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.

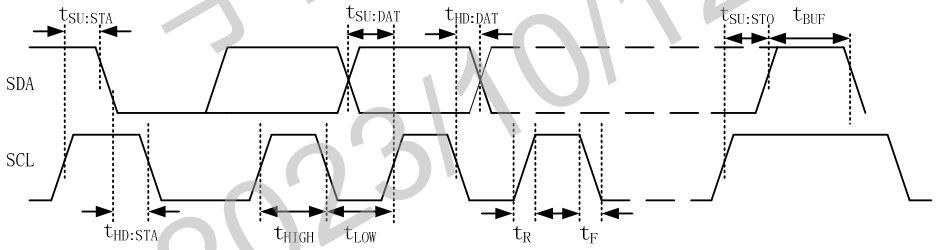


Figure 3-1. SDA and SCL Bus Timing

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4 Functional description

4.1 Overview

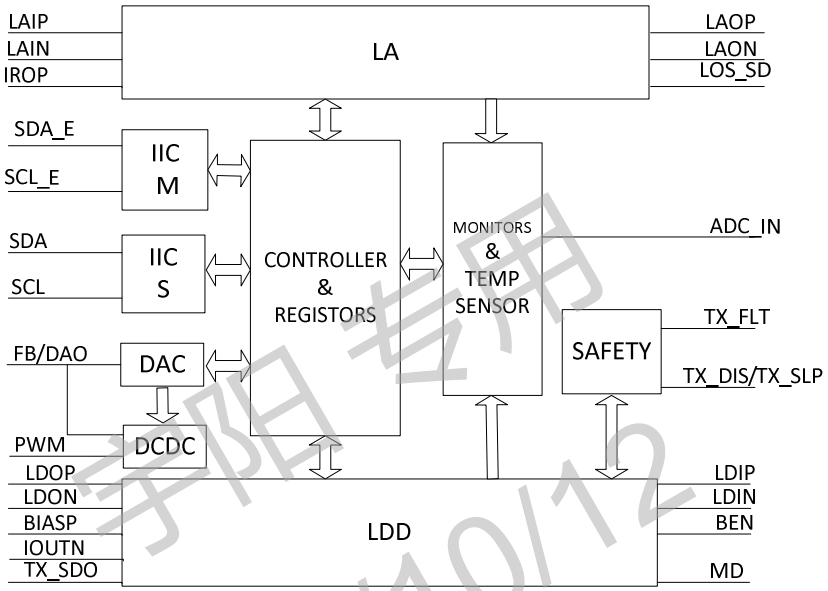


Figure 4-1. UX3361 function overview

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4.2 Limiting Amplifier

4.2.1 Architecture

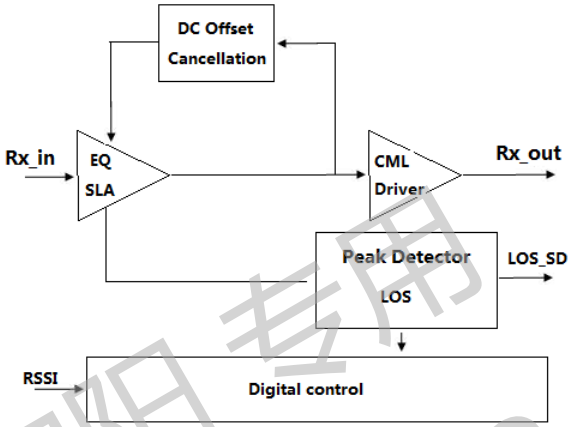


Figure 4-2. Limiting Amplifier Function Overview

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4.2.2 Limiting Amplifier features

The limiting amplifier of UX3361 consists of six blocks, which are equalizer; post amplifier; output CML driver; DC offset cancellation block; peak detector and LOS indicator and digital control block.

To compensate the high frequency loss of the input signal, an equalizer is implemented in the receive path of UX3361. The equalizer implements 0dB to 8dB of gain boost at 5.5GHz in fifteen steps through the RX_CTRL3 register RX_EQSETC, table 80h, AB(6:3)h; the equalization will be enabled by setting the RX_CTRL3 register RX_EQ_EN, table 80h, AB(7)h to '1'.

The polarity of the output data can be same or reverse to the input by setting the he RX_CTRL2 register DPOLCTRL, table 80h, AA(7)h to '0' or '1'.

The CML output buffer provides a high speed standard CML logic output interface with 50ohm output impedance. The output amplitude of the CML buffer can be changed from 300mV Vppd to 1100mV Vppd in 8 steps. The output amplitude setting can be set through the RX_CTRL1 register AMPCTRL, table 80h, A9(7:5)h. A selectable squelch function is implemented in the output driver of the LA, by setting the RX_CTRL3 register SQU_DIS, table 80h, AB(0)h to '0', the output high speed signal will be muted when the input

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amplitude is lower than the pre-programmed loss of signal threshold.

To compensate the high frequency loss in the output PCB trace, a pre-emphasis function is implemented at the output CML buffer. The post tap amplitude can be varied from 0 to 300mV Vppd in 16 steps through register Pectrl, A2h, 73(3:0)h. The pre-emphasis can be disabled by setting Pectrl, A2h, 73(3:0)h to 0000. The pulse width of the pre-emphasis can be tuned in 8 steps though the RX_CTRL5 register TPEDLY, table 80h, AE(2:0)h.

UX3361 indicates the loss of signal by detecting the OMA (optical modulation amplitude). The loss of signal threshold can be modified by the register LOSCTRLC, table 80h, AD(7:0)h. The LOS threshold can be set into two different ranges through the RX_CTRL4 register LOSRANGE(1:0), table 80h, AC(5:4)h. When setting the RX_CTRL4 register LOSRANGE(1:0), table 80h, AC(5:4)h to '00', the LOS threshold will be set in a lower input range (10-25mV Vppd). The LOS threshold will be set in a higher input range (20-60mV Vppd) by setting the RX_CTRL4 register LOSRANGE(1:0), table 80h, AC(5:4)h to '01'. The LOS threshold will reach the maximum input range (40-120mV Vppd) by setting the RX_CTRL4 register LOSRANGE(1:0), table 80h, AC(5:4)h to '10'. The hysteresis ratio of the LOS detection can be varied from 0.5dB to 4dB in 8 steps through the RX_CTRL4 register HYSCTRL, table 80h, AC(2:0)h. The loss output polarity is controlled by the RX_CTRL4 register LOSPOLCTRL, table 80h, AC(4)h. If the RX_CTRL4 register LOSPOLCTRL, table 80h, AC(4)h is set to '0', the LOS_SD pin indicates a digital stat high when the input amplitude is lower than the LOS threshold and vice versa.

To compensate the LOS threshold drift causing by temperature, the LOSCTRLC can be set through a temperature lookup table by setting register Loslut_en, table 80h, AC(7)h to '1'.

Figure 4-3 is a diagram indicates the LOS assert threshold versus LOSCTRLC.

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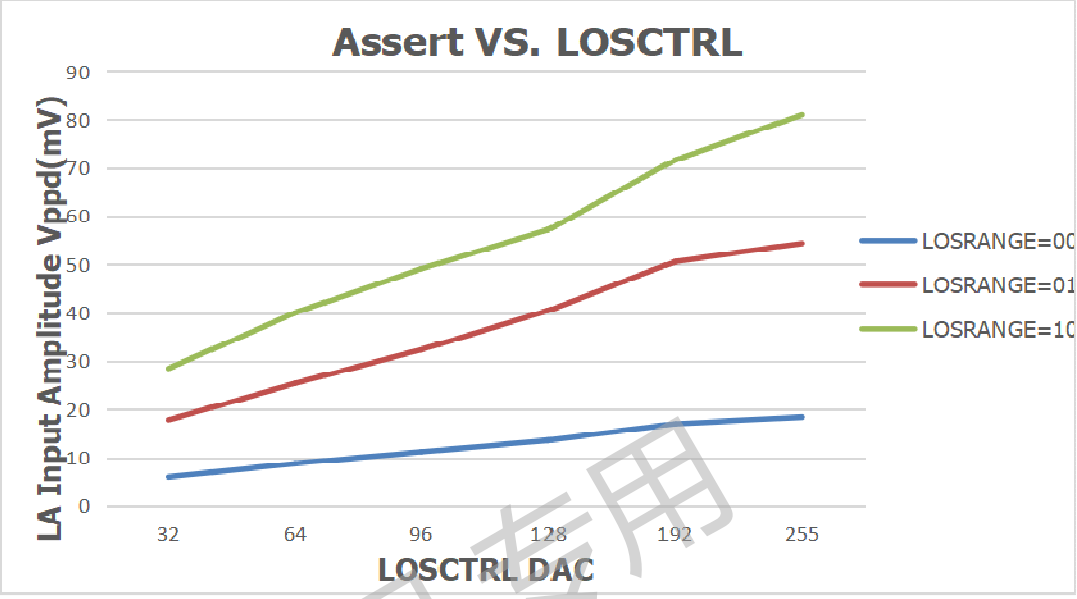


Figure 4-3. LOS Assert Threshold VS. LOSCTRLC(Sim value @LOSRANGE=10)

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The los register can be in-phase or reverse to the digital state of pin LOS_SD by setting the RX_CTRL4 register LSTAT_C, table 80h, AC(3)h to '0' or '1'. When LSTAT_C is '0', the los register will be in-phase to the digital state of pin LOS_SD and vice versa.

The state of the LOS can be latched by a LOS latch in order to filter a potential bouncing caused by the TIA. When LOS state changes from assert to de-assert, the LOS latch can hold the state for a programmable period of time controlled by register Los_latch, table 80h, AA(4:0)h; When LOS state changes from de-assert to assert, the LOS latch can hold the state for a programmable period of time controlled by register Los_delatch, table 80h, A9(4:0)h. Setting Los_latch, table 80h, AA(4:0)h or Los_delatch, table 80h, A9(4:0)h to 0000 to disable the LOS latching feature, respectively.

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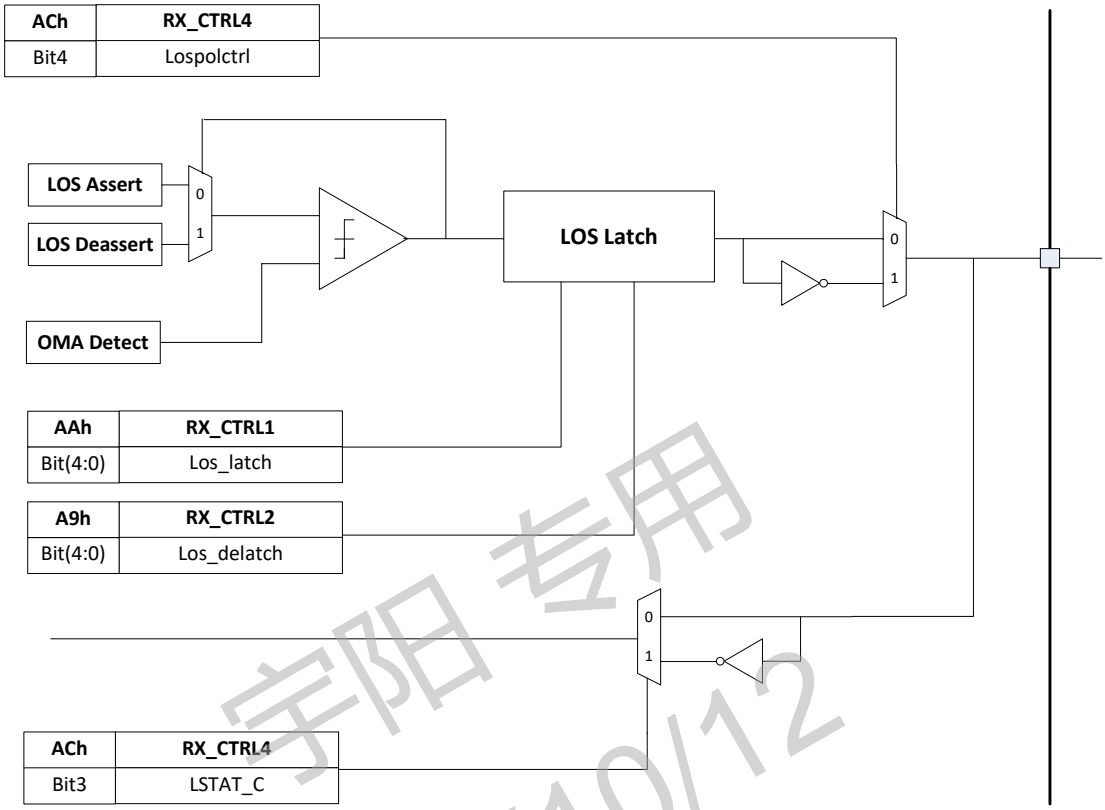


Figure 4-4. Block Diagram of the Los Detection

The high speed path of the LA can be power off by setting register PWROFF_EN, table 80h, AB(7)h to '1'. When the LA is on OMA LOS detection scheme, the LOS detection function will be disabled when LA is power off, the LOS_SD pin will be at LOS assert stat.

4.3 Laser Driver Features

The laser driver input buffer provides the necessary drive to the laser driver output stage. It includes an internal high impedance bias network and is designed to be DC or AC-coupled. For high frequency applications an external termination network must be implemented.

The laser driver output is designed to drive lasers in common anode configuration using DC or AC-coupling. In burst mode operation DC-coupling must be used.

The data polarity of the laser driver could be changed by setting **Inpolsw, table 80h, 83(3)h**. The burst enable polarity of the laser driver could be changed by setting BEN_pch, table 80h, 8A(1)h. The DCD of the output eye diagram could be adjusted by setting **Vdcdc,**

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table 84h, EAh.

4.3.1 Modulation Current Control

The modulation current can be either set by a constant register value or controlled by a temperature indexed look-up Table (TLUT).

If **ModLutEn, table 80h, 83(6)h** is set to 0, then Imod is set as a constant **Imodc, table 80h, 88h-89h**. If **ModLutEn, table 80h, 83(6)h** is set to 1, then Imod is set by **MOD TLUT, table 82h, 80-E8h**. The TLUT is indexed by the temperature ADC. When the Imod is changed from one value to another, the UX3361 has a gradient function of the current , that is, UX3361 builds in a clock with the frequency about 300K, the value of the Imod changes one LSB in a clock cycle. The temperature ADC could be saw in **TEMP_DATA, table 80h, F7-F8h**, and the search of the table lookup algorithm, please see Section 5.3.3 description.

In every index there is 10 bits Imod DAC.

The values of TLUT reside in EEPROM, and are transferred at start up to on-chip registers.

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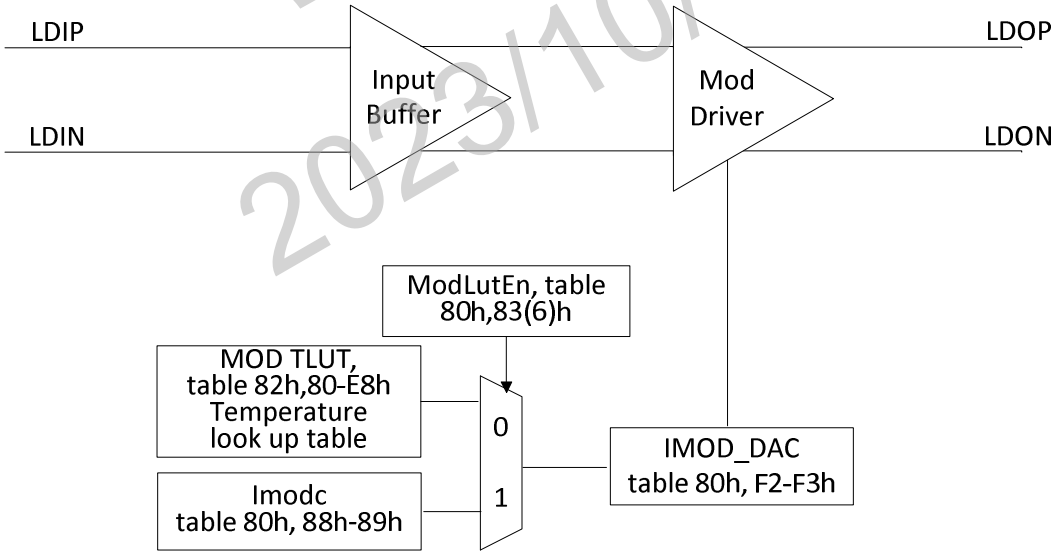


Figure 4-5. I_{mod} generation

The active setting of I_{mod} current DAC can be read at **IMOD_DAC, table 80h, F2-F3h**.

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Table 4-1: Imod Current DAC Characteristics

Parameter	Comments	Typical Step Size	DAC Range	Operational Range
I_{mod_dac}	I_{mod} current DAC (10 bits)	0.13mA	0 to 130mA	0 to 120 mA

Register **PA_SET(9:0), table 80h, 8D-8Eh**, set the PA optical power, The average optical power and extinction ratio can be determined by I_{bias} and I_{mod} current.

The value of I_{mod} could be read by **IMOD_DAC, table 80h, F2-F3h** register.

4.3.2 Bias Current Control

The bias current can be set in open loop or closed loop. In either mode the Ibias can be monitored and be read by AMUX output. The bias current is controlled by an 10 bits DAC, and the setting of this DAC can be read by **BIASCT_R, table 80h, F0-F1h**.

Table 4-2: Ibias Current DAC Characteristics

Parameter	Comments	Typical Step Size	DAC Range	Operational Range
Ibias_dac	Ibias current DAC (10 bits)	0.13mA	0 to 128mA	0 to 120 mA

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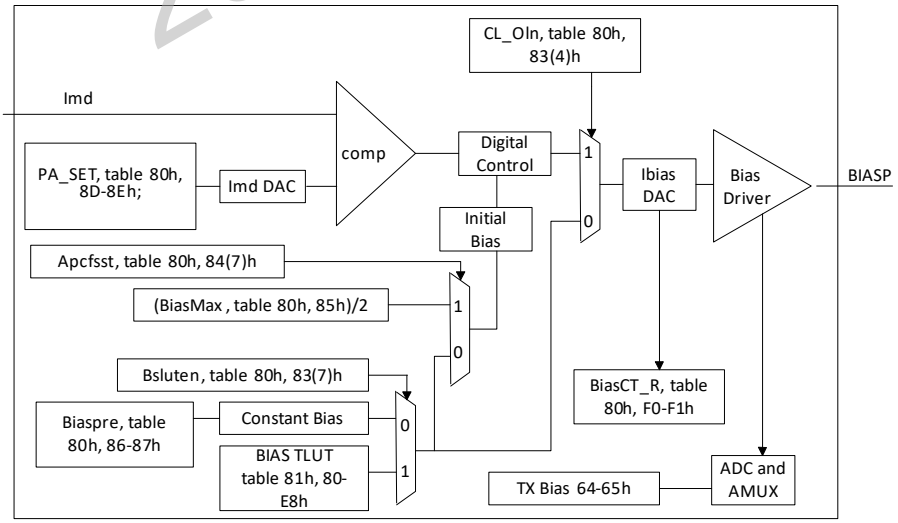


Figure 4-6. Ibias generation

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4.3.2.1 Open Loop

When **CL_OLn, table 80h, 83(4)h** is set to 0, the bias current is set in open loop mode. The bias current can be either set by a constant register value biaspre, table 80h, 85h-86h while **Bsluten, table 80h, 83(7)h** is set to 0, or set by a temperature indexed lookup Table (TLUT) while **Bsluten, table 80h, 83(7)h** is set to 1.

The **BIAS TLUT, Table 81h, 80-E8h** is indexed by the temperature ADC. When the I_{bias} current is changed from one value to another, the UX3361 has a gradient function of the current , that is, UX3361 builds in a clock with the frequency about 300K, the value of the I_{mod} changes one LSB in a clock cycle. The search of the table lookup algorithm, please see Section 5.3.3 description.

The active setting of I_{bias} DAC can be read at **BIAS TLUT, Table 81h, 80-E8h**.

4.3.2.2 Single Closed Loop

If **CL_OLn, table 80h, 83 (4)h** is set to 1, I_{bias} is set in closed loop mode. The average output optical power of the laser is controlled by a digital power control loop. The feedback of the control loop is connected to MD pin by a monitor photodiode.

When Ibias works in single closed loop mode, the current from the monitor photodiode I_{md} is scale-up or scale-down to I_{mdm} and then compares with a reference current I_{apcset} , I_{apcset} is generated by the **PA_SET(9:0), table 80h, 8D-8Eh**, used for setting the average optical power (i.e., the average current of photodiode).

The comparator in digital APC is a hysteresis comparator, and its hysteresis range I_{range} can be set by **Apcrange, table 80h, 8B(6:5)h**. The hysteresis range is 1%~5% of I_{apcset}.

Table 4-3: PA_SET_{dac} Current DAC Characteristics

Parameter	Comments	Typical Step Size	DAC Range	Operational Range
PA_SET_{dac}	I_{p1} current DAC (10 bits)	1.76uA	0 to 1800uA	0 to 1500uA

Table 4-3: Irange Settins in Single Closed Loop

Apcrange(1:0)	00	01	10	11
I_{range}	1%	2%	3%	5%

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In typical situation, I_{range} should be set as small as possible for good accuracy of I_{md} setting. But if the I_{range} is set too small, it would add some jitter to output eye diagram. So the Irange should be chosen properly.

The closed loop digital APC has a bulit-in clock (typical frequency is 20KHZ).

APC of UX3361 has the function of scaling down the optical power and maintaining the extinction ratio. When this function is used, the PA_SET current will be scaled up or down in a certain proportion, PA_SET current is set by **PA_SET(9:0), table 80h, 8D-8Eh**. when single closed loop is used, the I_{mod} current will be scaled up or down in a certain proportion. This function is set by **APCSCALE (1:0), table 80h,6F(1:0)h** in A2h.

Table 4-4: APCSCALE Settings in Single Closed Loop

APCSCALE(2:0)	PA_SET and I_{mod} in the single closed loop
00	×1
01	×0.5

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4.3.2.3 Start-up initialization

There are two types of APC start-up initialization in closed loop. If **Apcfsst, table 80h, 84(7)h** is set to 1, fast start-up is enabled. If **Apcfsst, table 80h, 84(7)h** is set to 0, then normal start-up is enabled.

If **Apcfsst, table 80h, 84(7)h** is set to 0, then it is initialed with normal start-up. The initial I_{bias} could load a constant from **biaspre, table 80h, 86h-87h**, when **Bsluten, table 80h, 83(7)h**=0 or from a BIAS temperature look up Table when **Bsluten, table 80h, 83(7)h**=1.

In fast start-up mode, Apcfsst is set to 1. After power up, **Starten, table 80h, 9D(1)h** is set to 1, TX_Disable is set to enable and while BEN is enabled, then the APC started. In the first 7 clocks the APC uses a fast clock which is set by **FAPC_CLK（1:0）, table 84h, E4(1:0)h**. When Fstclk1_2 is set to 11 then 5MHz clock is chosen. And when **FAPC_CLK（1:0）, table 84h, E4(1:0)h** is set to 00 then 11MHZ clock is chosen. When BEN is disabled, it turns off the bias and modulation currents, these 7 clocks are paused.

At the first 7 clocks, the APC uses halving binary search sequence to get the target optical power. During this period, the data path is disabled and modulation outputs balanced, then $I_{mod}/2$ flows into both LDOP and LDON. The original bias current output is determined by **BiasMax, table 80h, 85h**, which is an 8 bits binary code to set the safe maximum bias

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current. And the orginal I_{bias} by DAC is set to BiasMax/2. In the following 7 clocks the APC will find out the target optical power. After that, the data path will be enabled, and the APC clock will change to normal clock. The timing diagram is showed as follows, in which TX_Disable is enabled when it is set to low, BEN is enabled when it is set to high.

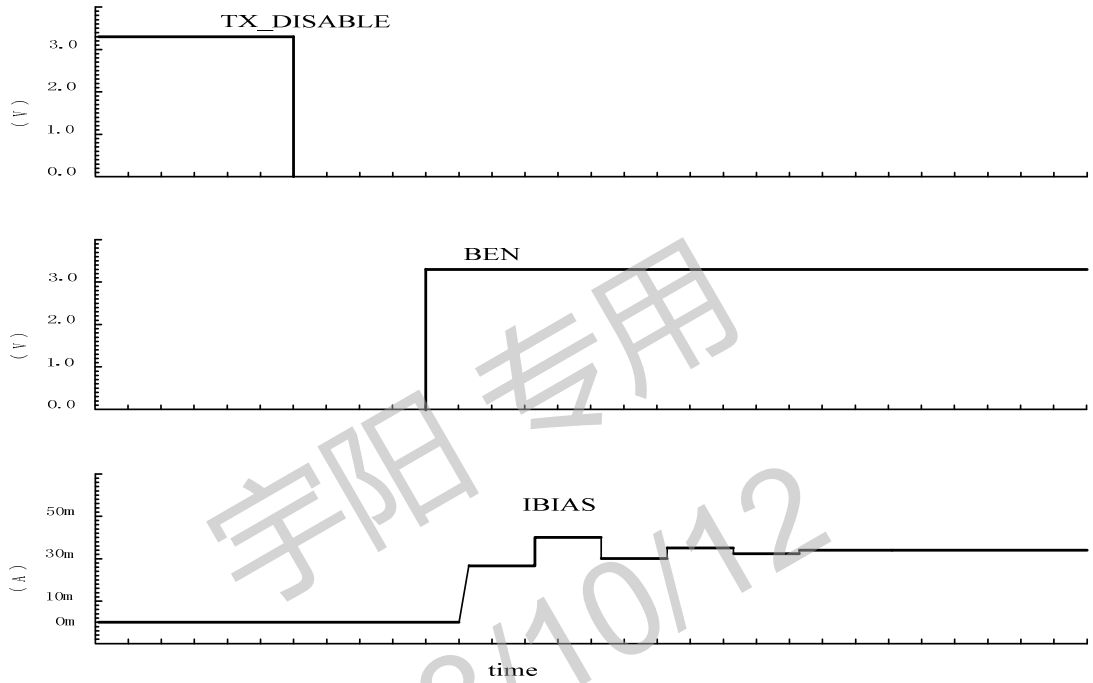


Figure 4-7. APC Fast Start-Up in Burst Mode

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4.3.2.4 Burst Mode

In burst mode, the register **Burst0_cm1, table 80h, 8B(7)h** should be set to 0, in continuous mode, it is set to 1. BENP/BENN input can be floating in continuous mode operation.

In burst mode, when burst polarity is set to not reverse polarity. **BEN_pch, table 80h, 8B (2) h**=0, BENP/BENN is set to low/high individually, the modulation and bias currents are turned off. When BENP/BENN is set to high/low, the modulation and bias currents are turned on. The burst on/off timing sequences are described in detail in 3.4.3.

In burst mode, pin20 TX_SDO can indicate the state of laser diode. The output level can be set to TTL or CMOS level. While **CMOS_SEL, table 80h, 8B(1)h**=1, the output is CMOS level. While **CMOS_SEL, table 80h, 8B(1)h**=0, the output is TTL level, and the pin20 should be pulled up a 4.7-10KΩ resistor to vdd for TX_SD function. When BENP/BENN is set to high/low, the laser diode is turned on, and there will be some current through the

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monitor current I_{md}, then TX_SDO will be set to high. Otherwise TX_SDO will be set to low.

There is a high speed comparator in UX3361.The monitored current I_{md} is calculated to I_{mdm}, and then compare with a reference current I_{mdsd}. I_{mdsd} could be set by **Txsdset, table 80h, 84(6:5)h** and Iapcset which set the average current of MD, So even in open loop, if we want the TX_SD function to work normally, we should set I_{apcset} equal to the PD monitor current I_{md}.

Table 4-5: TX sd Settings

Txsdset(1:0)	00	01	10	11
I_{mdsd}	1/8 of I_{apcset}	2/8 of I_{apcset}	3/8 of I_{apcset}	4/8 of I_{apcset}

The delay of TX_SD could be set by **SD_C(1:0), table 84h, E2(2:1)h**. In order to make the rise and fall delay is more symmetrical, it is recommended to choose 37.5% of Iapcset . And this is described in detail in 3.4.3.

When the burst is disabled, the I_{bias} and the I_{mod} can be set to be closed or not. when the register **Io_on0_off1, table 80h, 92 (1) h** is set to 0, then the burst is disabled, the I_{bias} and the I_{mod} are not closed, they are generated from the IOUTN; When the register **Io_on0_off1, table 80h, 92 (1)h** is set to 1, then the burst is disabled, the I_{bias} and the I_{mod} is completely shut down, the total power consumption of the chip will be significantly reduced.

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4.4 Laser Safety Features

The laser safety circuit monitors the device for potential faults. If a fault is detected then the pin20 TX_FAULT will be asserted, and it will be latched even if the fault condition goes away. The latched fault can be cleared by restart up, or the pin TX_DISABLE which is set to 1 and then to 0, or the register **Soft TX Disable, 6E(6)h** which is set to 1 and then to 0.

The register **LtchFt_R, 6E(2)h** reflects the status of the pin TX_FAULT.

The transmit fault can be caused by the following conditions:

1. After power on, the supply monitoring circuit detects that the power supply voltage is >4.3V, which can be regarded as a fault condition. **Faultset(0), table 80h, 8C(0)h**=1 should be set when choosing this as a fault condition, and this fault state is in **Fault(0), table 80h, EF(0)h**.

2. Whether internal current source work is normal or not. **Faultset(1), table 80h, 8C(1)h**=1 should be set when choosing this as a fault condition, and this fault state is in

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Fault(1), table 80h, EF(1)h.

3. The output voltage monitoring circuit detects whether the voltages of LDOP/LDON is smaller than 0.1V or not. **Faultset(2), table 80h, 8C(2)h**=1 should be set when choosing this as a fault condition, and this fault state is in **Fault(2), table 80h, EF(2)h**.

4. The output voltage monitoring circuit detects whether the voltages of BIASP is smaller than 0.1V or not. **Faultset(3), table 80h, 8C(3)h**=1 should be set when choosing this as a fault condition, and this fault state is in **Fault(3), table 80h, EF(3)h**.

5. Whether I_{bias} > or = BIASMAX or not. **Faultset(4), table 80h, 8C(4)h**=1 should be set when choosing this as a fault condition, and this fault state is in **Fault(4), table 80h, EF(4)h**.

6. Detecting whether the rogue ONU is found or not, that is, when the BEN is set to low and TX_SD is set to high. **Faultset(5), table 80h, 8C(5)h**=1 should be set when choosing this as a fault condition, and this fault state is in **Fault(5), table 80h, EF(5)h**.

7. Detecting whether the presence of long light or not. the time to high level of TX_SD over a programmable time can be regarded as a fault condition. The programmable time is set by the register COUNTER, table 80h, 81h, and a single count clock is 410us. **Faultset(6), table 80h, 8C(6)h**=1 should be set when choosing this as a fault condition, and this fault state is in **Fault(6), table 80h, EF(6)h**.

If **Ftshdnen, table 80h, 83(2)h** is set to 1, then the fault condition will cause to shut down the bias and modulation currents. If **Ftshdnen, table 80h, 83 (2)h** is set to 0, the fault condition will not shut down the bias and modulation currents.

If **Bsmaxprotect, table 80h, 8A(5)h** is set to 1, in close loop mode, while the Ibias DAC counts to the value of **BiasMax, table 80h, 85h**, then the counter will not increase again. It can only be held or reduced. If **Bsmaxprotect, table 80h, 8A(5)h** is set to 0, in this condition the Ibias DAC can either increase or reduce.

The LDD in UX3361 has some kinds of sleep modes. When **Lpow, table 80h, 83(5)h** is set to 0, the laser driver operates in normal state. But when **Lpow, table 80h, 83(5)h** is set to 1, the laser driver is disabled, and the current of the laser driver will be shut down.

4.5 Burst Enable and TX Input Connection Options

The UX3361 supports various modes of interfacing to the transmit data (LDIP/LDIN) and burst enable (BENP/BENN) inputs providing the signal voltage and common-mode voltage levels are within the valid range specified in 3.4.1. The input structure of laser driver in

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UX3361 is shown as below.

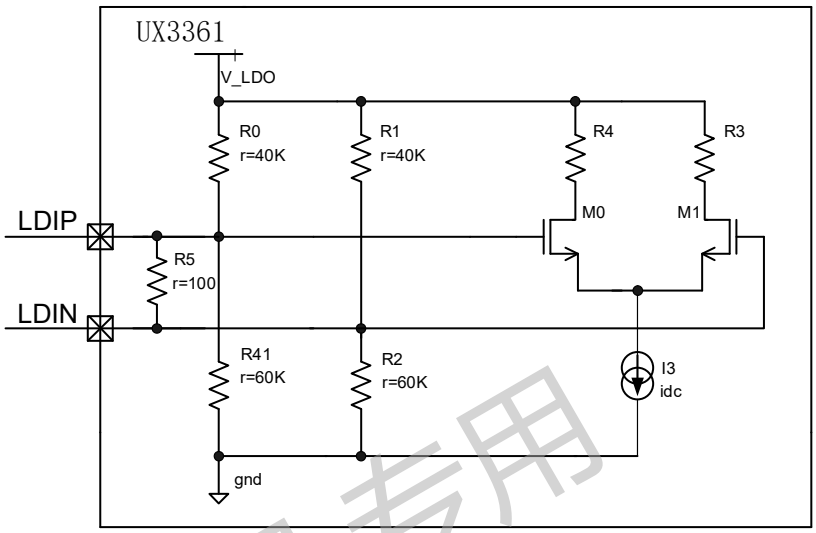


Figure 4-8. Laser Driver Input

4.6 Temperature Measurement

UX3361 uses an on-chip temperature monitor and a 9-bit ADC to perform a temperature measurement once per 10ms. When using on-chip temperature monitor, the measured ADC value can be read from the register.

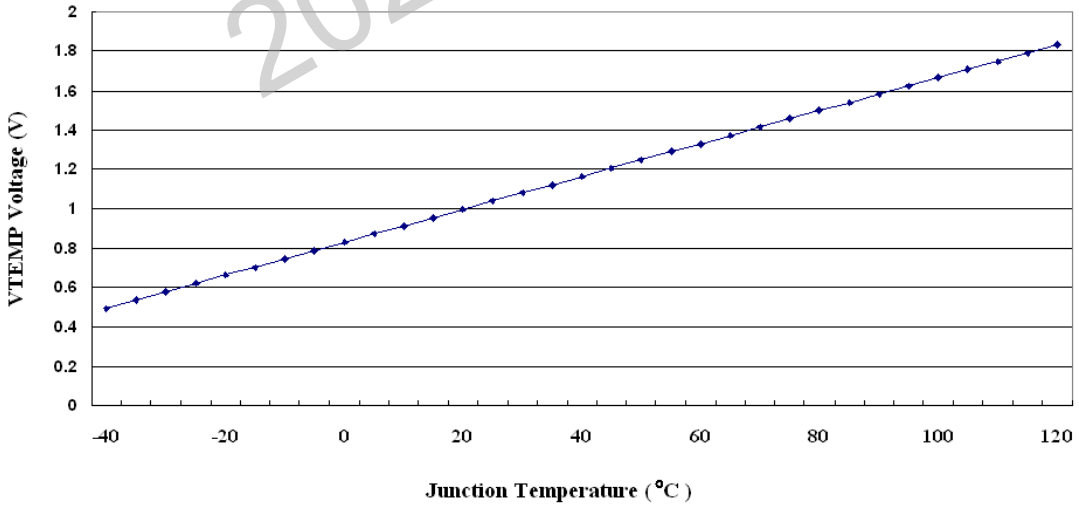


Figure 4-9. VTEMP voltage VS. Junction Temperature

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Table 4-6: The Relation of VTEMP Voltage in Temperature Sensor and Junction Temperature

Parameter	Symbol	Min.	Typical	Max.	Units.
Temperature	T	-40		120	℃
VTEMP Voltage	Vtemp	500		1850	mV
ADC Slope			0.4		℃/bit
Accuracy	Tacc		+/-2		℃

The temperature monitor is connected with a 9-bit ADC through an analog multiplexer (AMUX). The measured PTAT (proportional to absolute temperature) voltage is presented to the 9-bit ADC by setting the AMUX address **AMUX_ADDR(3:0), table 80h, E4(3:0)** to 0000.

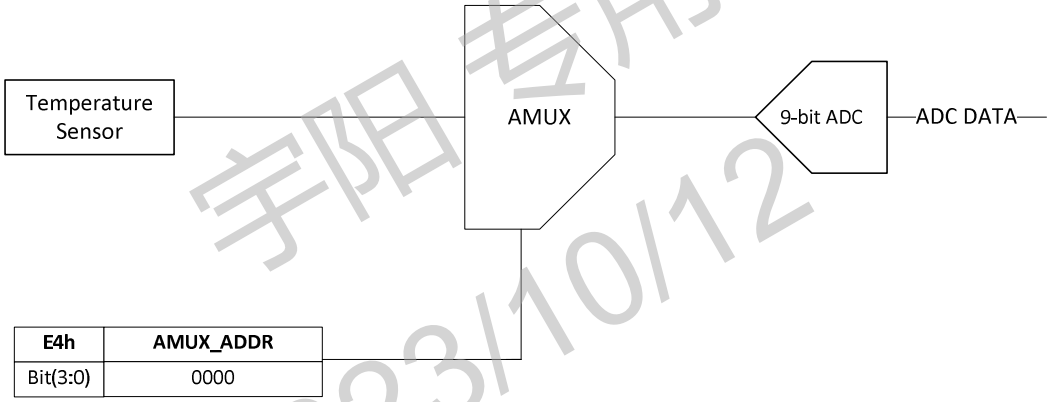


Figure 4-10. Temperature Calibration Functional Block Diagram

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4.7 DA Current output

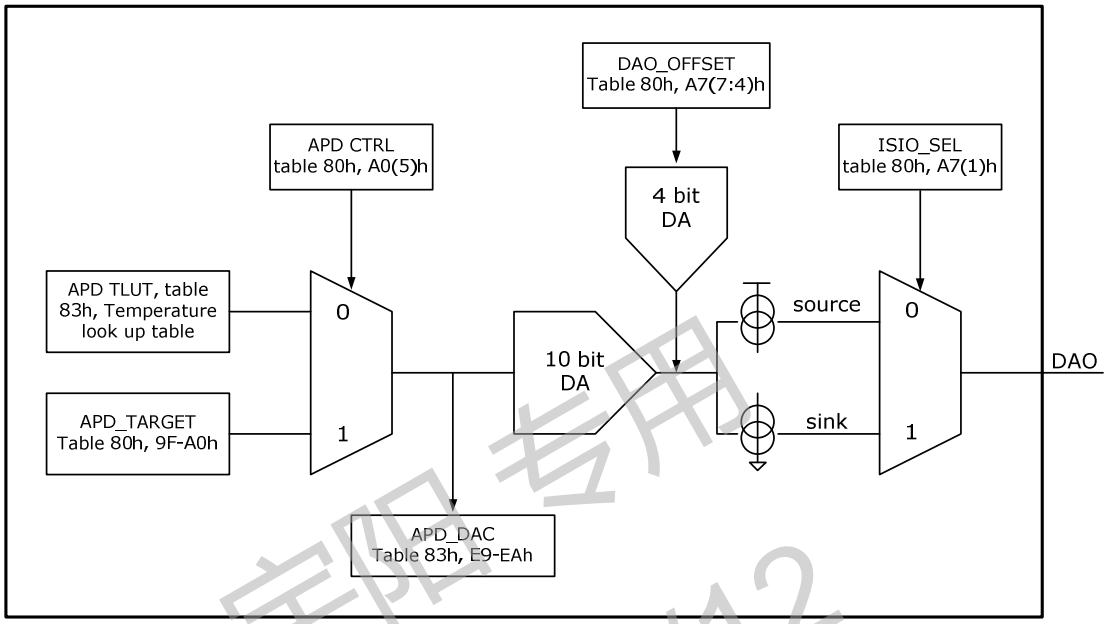


Figure 13. DA block diagram

The UX3361 has a 10 bits DA current output. The DA output current can be set as a constant by **APD_TARGET, table 80h, 9Fh-A0h**, or by a temperature look up Table **APD TLUT, table 83h, 80h-E8h**(10 bits DAC). If **APD_CTRL, table 80h, A0(5)h** =1, the DA current is set by APD_TARGET; if **APD_CRTL, table 80h, A0(5)h**=0, the DA current is set by APD TLUT.

The APD TLUT is indexed by the temperature sensor ADC. The temperature ADC could be seen in **TEMP_DATA, table 80h, F6h-F7h**. The search of the lookup table algorithm, please see the section 5.3.3.

According to customer's requirement, the output of 10 bit DA can add on an offset value by setting **DAO_OFFSET table 80h, A7(7:4)h**.

And the final DA output current can be set to Isource or Isink by setting **ISIO_SEL,table 80h,A7(1)h**, when it is set to 0, the Isink mode is selected, when it is set to 0, the Isource mode is selected. And the full range or half range can be set by **IOIS_HALF,table 80h,A7(2)h**, when it is set to 0, the full range is selected; when it is set to 1, the range is halved. The output current error of DAO is less than +/-10%.

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Parameter	Output current mode	Range mode	One LSB typical value	DAC Range
Idao	Isource@10 bit DA (VAPD_DAC<2V)	Full range	1.87uA	0 -- 1.912 mA
		Half range	0.94uA	0 -- 0.956 mA
	Isink@10 bit DA (VAPD_DAC>0.6V)	Full range	0.48uA	0 -- 488 uA
		Half range	0.24uA	0 -- 244 uA
	Isource@4 bit DA (VAPD_DAC<2V)	Full range	60.3uA	0 -- 905 uA
		Half range	30.1uA	0 -- 452 uA
	Isink@4 bit DA (VAPD_DAC>0.6V)	Full range	15.4uA	0 -- 231 uA
		Half range	7.7uA	0 -- 116 uA

The DA block has a sleep mode. DA works normally when **DA_LPOW, table 3, A7(0)h**=0 ; it is disabled when **DA_LPOW, table 3, A7(0)h**=1, and its output current is 0.

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4.8 Boost DC-DC controller

UX3361 integrates a boost DC-DC controller, which can be used to control the outside boost circuit to provide an avalanche voltage for APD.

When using the boost DC-DC controller, **DA0_PWM1, table 80h, A7(3)h** need be set to "1" in order to select voltage as the output item of DA module and select the "FB" function for PIN 8.

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4.8.1 Main Functions of boost DC-DC controller

4.8.1.1 Boost DC-DC controller application circuit

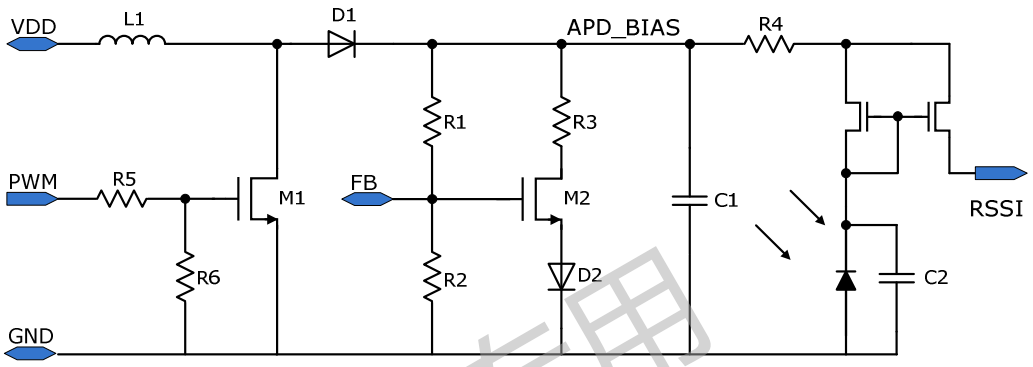


Figure 4-12. DC-DC Application Circuit

As shown in Figure 4-12, Signal "PWM" from UX3361, control the on/off state of PowerMos M1. By changing the pulse width of "PWM", the voltage "APD_BIAS" which sustained by the capacitance C1, can be changed. At the same time, "APD_BIAS" is divided by R1 and R2, then feedback to the "FB" PIN of UX3361, providing a stable bias for APD.

Figure 4-12 also shows a fast discharge function, which realized by PowerMos M2 and D2. When the controller detected an over current or over voltage warning, PIN "FB" will be pull up to VDD, M2 and D2 are turned on, then C1 can be fast discharged through M2 and D2, means "APD_BIAS" can be fast lower down, avoid the breakdown of APD.

4.8.1.2 Boost DC-DC control circuit

DC-DC Control circuit offers two working frequency, 250KHz and 500KHz, which decided by **FRQSEL, table 80h, A6(4)h**. When FRQSEL=0, working frequency is set to 250KHz. when FRQSEL=1, working frequency is set to 500KHz. **DUTYCODE(2:0), table 80h, A5(4:2)h** and **FIX_ADJ_SEL, table 80h, A6(0)h** are used to set the max duty-cycle of "PWM" signal. When FIX_ADJ_SEL=0, the max duty-cycle of PWM is set to 85%. When FIX_ADJ_SEL=1, the max duty-cycle of PWM can be set through DUTYCODE(2:0), setting range is 45%~80% and 5% for each step.

The way in which DC-DC control circuit use to adjust the APD_BIAS, is to adjust the internal reference voltage (Vref), as shown in Figure 4-13.

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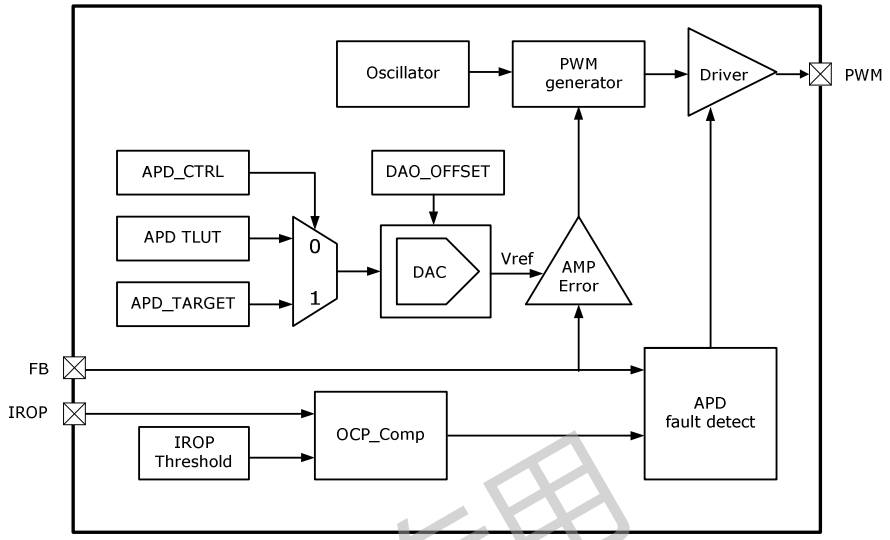


Figure 4-13. DC-DC control circuit

Just like DA current, Vref can be controlled by **APD_TARGET1, table 80h, 9Fh** and **APD_TARGET0, table 80h, A0(1:0)h,** or can be controlled by Table **APD TLUT, table 83h, 80-E8h**, decided by **APD_CTRL, table 80h, A0(5)h**. When APD_CTRL=1, Vref is controlled by APD_TARGET. When APD_CTRL=0, Vref is controlled by APD TLUT, and it becomes a temperature depended value. And an offset value also can be added on Vref by setting **DAO_OFFSET table 80h, A7(7:4)h**. Customer can use the below formula to get the desired APD_BIAS:

$$APD_BIAS = \left(\frac{D_{set} \times 1.24}{1023} + \frac{D_{offset} \times 0.58}{15}\right) \times \frac{R1 + R2}{R2}$$

D_{set} is the setting value in APD_TARGET or Table APD TLUT (in decimal format), D_{offset} is the setting value of DAO_OFFSET, R1, R2 is the voltage divider shown in Figure 4-12.

DC-DC control circuit also integrates the soft start function, in order to increase the power up time of APD_BIAS, avoiding big overshoot which might break APD. Soft start time can be adjusted by setting **Clk10k, table 80h, A6(6)**. When Clk10k=0, soft start time is about 10ms, When Clk10k=1, soft start time is about 20ms.

4.8.2 Safety logic and other functions of Boost DC-DC controller

Safety logic integrated in DC-DC controller includes over current protection (OCP) and over

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voltage protection (OVP). And each protection provides two process mode, one time protection mode and burp protection mode. After OCP or OVP being powered on, if RSSI current exceed the threshold setting by **CUR_THH(3:0), table 80h, 9E(7:4)h**, or FB voltage exceed the threshold setting by **OVPCODE(2:0), table 80h, A5(7:5)h**, "PWM" signal will be pulled down to GND (PD_PWM=1, shown in Figure 4-14). CUR_THH(3:0) is used to set OCP threshold, setting range is 500uA~2000uA and step is 100uA。 CUR_THH(3:0) should be used with **IRSSI_SEL, table 80h, A4(3:1)h**, in order to deal with the variation of outside current mirror ratio. Adaptive mirror ratio range is from 7:1 to 1:1. OVPCODE(2:0) is used to set OVP threshold, setting range is 1.05*Vref~1.25*Vref and step is 0.025*Vref.

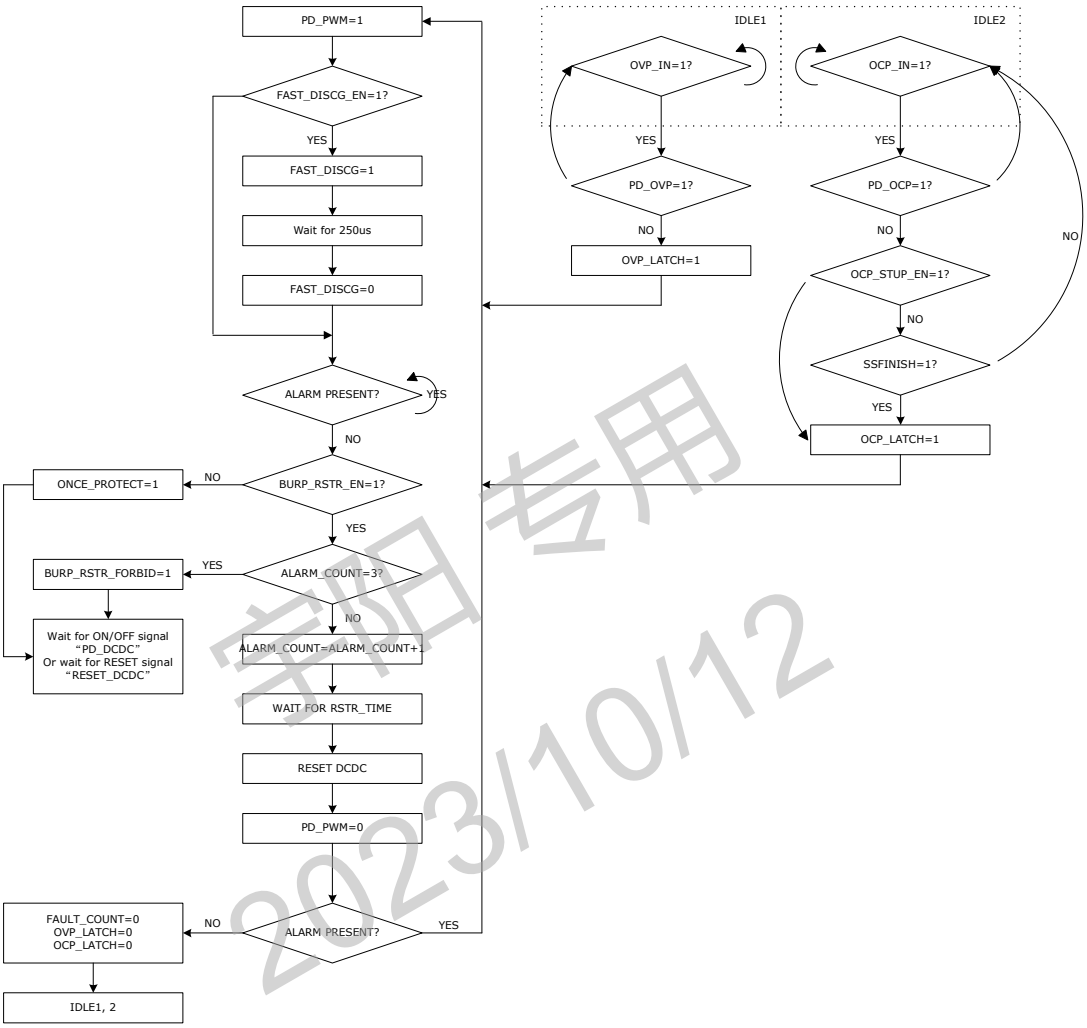
After "PWM" being pulled down to GND, customer can enable the "fast discharge" function by setting **Fast_discg_en, table 80h, A2(4)h** to "1", or can select one kind of warning processing mode by setting **BURP_RSTR_EN, table 80h, A3(7)h**. When BURP_RSTR_EN=0, one time protection mode is selected, PWM will be permanently pulled down to GND until restart or reset the controller. When BURP_RSTR_EN=1, burp protection mode is selected, the controller will be auto restarted after the OCP or OVP warning being clear. If consecutive auto restart exceed 3 times due to the same warning, PWM will be permanently pulled down to GND until restart or reset the controller. Customer can power down OCP or OVP function by setting **PD_OCP, table 80h, A5(0)h** or **PD_OVP, table 80h, A5(1)h**. When PD_OVP=1, over voltage protection is power down. When PD_OCP=1, over current protection is power down. During soft start period, over current protection can be disabled by setting **OCP_STUP_EN, table 80h, A4(7)h** to "0". Detail safety logic please refers to Figure 4-14.

For the whole DC-DC controller, it can be power down by setting **PD_DCDC, table 80h, A6(5)h** to "1". After power down, dc current of the controller will be less than 2uA. DC-DC controller provide a soft reset control bit, **RESET_DCDC, table 80h, A4(4)h**. When RESET_DCDC=1, all state registers relate to DC-DC controller will be reset. PD_DCDC also can be used to reset all DC-DC state registers.

In order to make the fault diagnose easier, DC-DC controller provide 9 state registers, indicating different kind of fault. **OVP_OUT, table 80h, F5(1)h**=1, stands for over voltage warning. **OVP_LATCH, table 80h, F4(5)h**=1, also stands for over voltage warning, but it is latched. **OCP_OUT, table 80h, F5(2)h**=1 stands for over current warning. **OCP_LATCH, table 80h, F4(6)h**=1, also stands for over current warning, but it is latched. VPWM_ABLE, table 80h, F5(3)h=0, means PWM is pulled down to GND. **SS_FINISH, table 80h, F5(0)h**=1, means soft start is finished. **FAST_DISCG, table 80h, F5(4)h**=1, means C1 is in fast discharging. **ONCE_PROTECT, table 80h, F4(4)h**=1, means the flow of one time protection mode is finished. **BURP_RSTR_FROBID, table 80h, F4(3)**=1 means the flow of burp protection mode is

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finished.



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Figure 4-11. Safety Logic

4.9 System control

4.9.1 Pin multiplexing selection control

UX3361 has three pins that are multiplexed. By setting TXD0_sleep1, table 80h, 92(4)h to 0, PIN10 can be set as the TX_DISABLE input, the SLEEP pin inside the chip is set to enable state; setting TXD0_sleep1, table 80h, 92(4)h to 1, PIN10 can be set as SLEEP input, the TX_DISABLE pin inside the chip is set to enable state.

By setting DA0_PWM1, table 80h, A7(3)h to 0, PIN8 can be set as DA current output.

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Setting DA0_PWM1, table 80h, A7(3)h to 1, PIN7 can be set as DCDC PWM output, and be connected to the gate of POWER-MOS, PIN8 be configured as feedback (FB) pin. In this case, A7(1)h must be set to 1.

By setting SD_ROGUE_C, table 80h, E5(4)h to 0, you can set the PIN24 as the TX_SD state output; set to 1 to set the PIN21 as light-emitting rogue ONU alarm output, for the light-emitting detection time see 7th point of Section 4.4.

4.9.2 Lower power control

The UX3361 analogs mainly include the LA limiter amplifier, the LDD laser driver, the DA current output and the DCDC PWM output, for each a low power control function is integrated. Each module has a low power control bit, for LA is PWROFF_EN, table 80h, AB(2)h,, LDD is LPOW, table 80h, 83(5)h, DA is DA_LPOW, table 80h, A7(0)h, and DCDC is PD_DCDC, table 80h, A6(5)h. When control bit is set to 0, corresponding circuit is working in normal mode, otherwise in sleep mode.

UX3361's A2 low bit also has low power control registers. RX_SOFT_SLEEP, table 80h, 6F(5)h, a low power control bit of the receiver, is enabled by setting to '1', and control the receiver after logic OR'd with PWROFF_EN, table 80h, AB(2)h. TX_SOFT_SLEEP, table 80h, 6F(3)h, a low power control bit of the transmitter, is enabled by setting to '1', and control the transmitter after logic OR'd with LPOW, table 80h, 83(5)h.

UX3361 also has a hardware low power control pin PIN10, TX_DIS/TX_SLP, and a software control bit TX_SOFT_SLEEP, table 80h, 6F(3)h. When the three control signals is low, logic OR'd with software control bit, the chip is in normal operation, otherwise it enters low power mode or sleep mode.

The low power consumption of the transmitter has the function of fast recovery to normal operation. Set the A2 low TX_FAST_SLEEP, table 80h, 6F(6)h =1, then when the transmitter wakes from sleep mode, the output modulation current and bias current will remain the value before sleep; set A2 low TX_FAST_SLEEP, table 80h, 6F(6)h=0, then when the transmit wakes from sleep mode, the output modulation current and bias current will be re-initialized.

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5 Control Interface

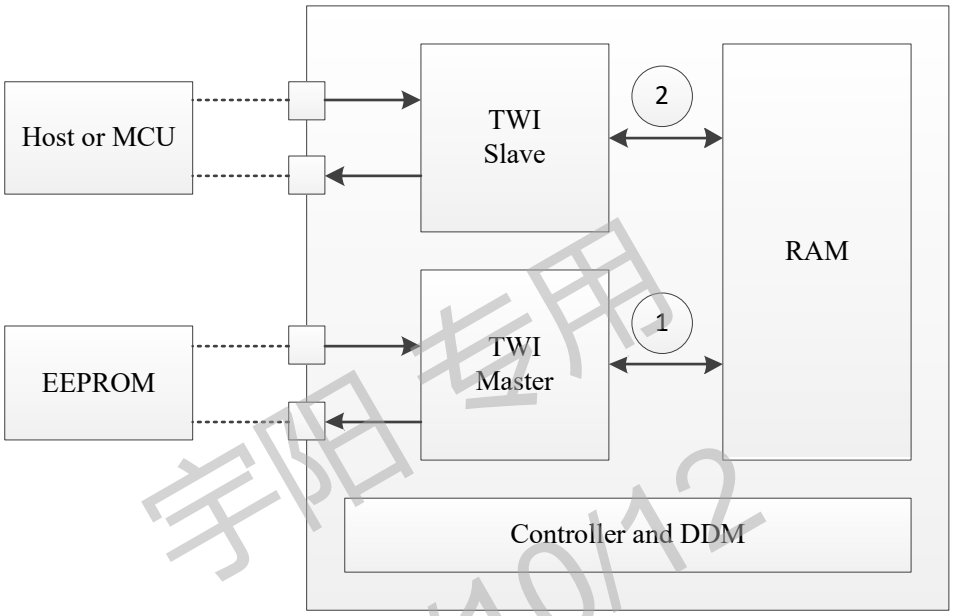


Figure 5-1. Serial Interfaces to RAM and the Controller

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The host communicates with the UX3361 via the slave Two Wire Interface(TWI) pins of the UX3361. When the data of the UX3361 is in need of storing to EEPROM, the UX3361 communicates with EEPROM via the master TWI pins of the UX3361.

5.1 Data Transfer Mechanisms

Two distinct data paths are identified in Figure 5-1.

When the UX3361 comes out of reset, the 2-wire serial slave interface is disabled. Only path 1 is active. The controller instructs the 2-wire serial master interface to attempt to transfer A0h and A2h register tables (A0 region, SFF-8472 diagnostics, user defined region, table 80h/81h/82h/83h/84h/85h/86h, and so on) from the external EEPROM to RAM. If this is successful then the start pulse will be set and the UX3361 will enter in the normal operation. If the transfer fails, then the status alarm bits in table 80h, FD-FEh) register will be set and the UX3361 will enter in the normal operation.

Regardless of the outcome, when the EEPROM read process is complete, the controller

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enables the 2-wire serial slave interface.

In the normal operation, the host or external MCU uses the 2-wire serial slave interface to write to or read from copies of A0 region, SFF-8472 diagnostics, user defined region, table 80h/81h/82h/83h/84h/85h/86h,and so on held in RAM(path 2).

The value of the 2-wire serial slave interface address can be changed to a value other than the default value of A0h and A2h(see datasheet register map in SLAVE_ADDRESS(table 80h, E4h)).To change The 2-wire serial slave interface address, write a new value to this register. The two least significant bits will be saved as zeros, the saved address is thus a new A0h address. A2h is always slaveaddress+2.

The UX3361 2-wire serial slave interface uses 8-bit addressing, which allows up to 256 bytes to be transferred during read process, while up to 16 bytes are allowed during write process. However, since the UX3361 contains more than 256 bytes, a table scheme is used. The lower 128 bytes of the default A2h region are independent of the currently selected table. Byte 7Fh is the Table select byte. This byte determines which memory table will be accessed by the 2-wire interface when address locations 80h to FFh in the default A2 region are accessed. Valid values for the Table Select byte are shown in Table 5-1.

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Table 5-1: Table Select Byte

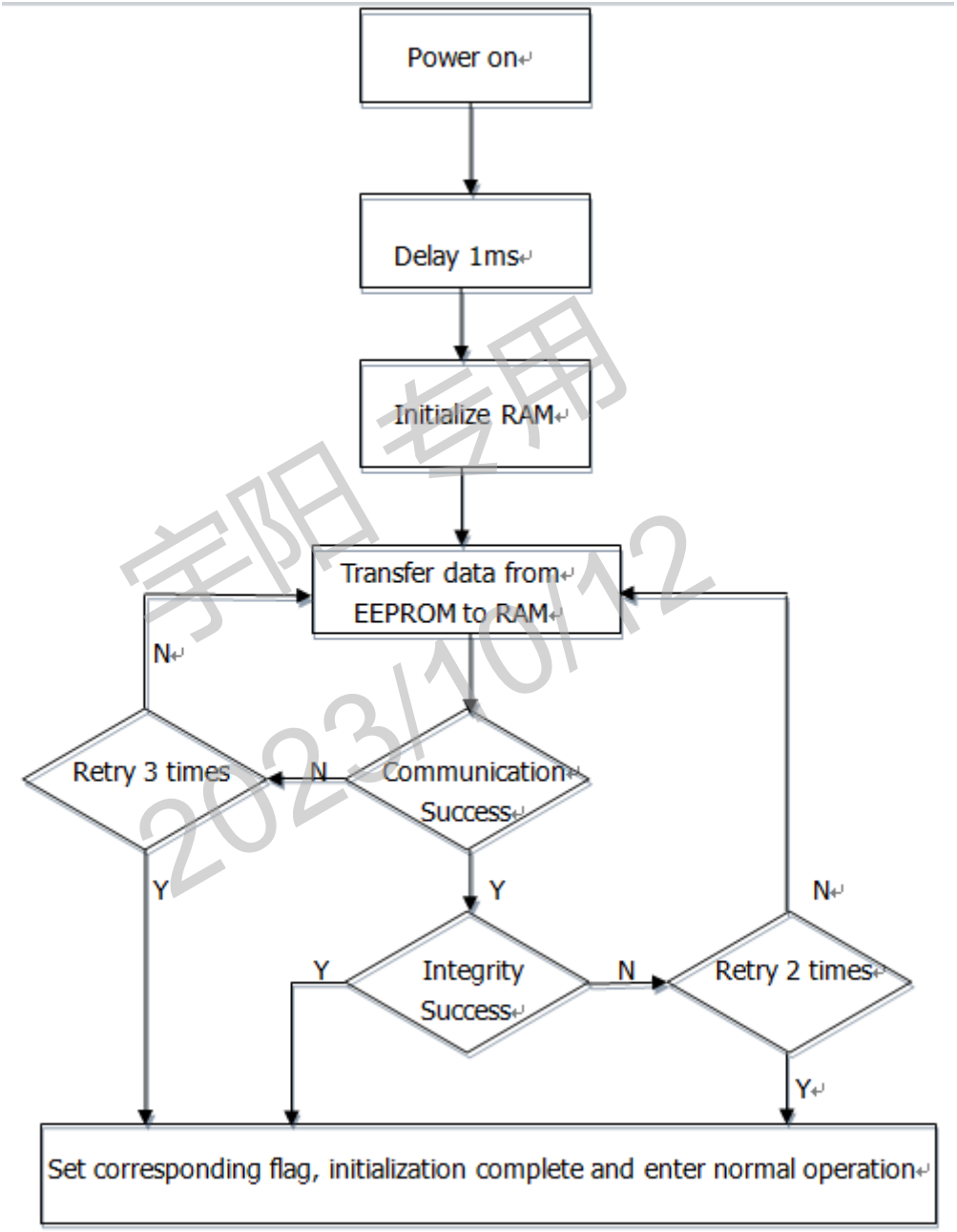
Table select byte(hex)	TABLE NAME
00	User defined region
01	
80	Device setting
81	BIAS TLUT
82	MOD TLUT
83	APD TLUT
84	APC current TLUT and TX EQ decoder
85	Dark current&RX EQ &LOS TLUT and RX PE decoder
86	TX EMP AMP TLUT
87	Chip id and Debug Data

5.2 Device Initialization Sequence

The Initialization Sequence is illustrated in Figure 5-2. The Data_Ready_Bar 6E(0)h bit in the STA_CTRL0 register indicates when data from the ADCs may be read after power up. It is firstly set to '1' before the 2-wire serial slave interface is enabled to indicate that the UX3361 is not ready. Once initialization is complete and the ADC data is ready,

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Data_Ready_Bar is cleared to '0'. This event can be used by the external host/MCU as a signal that the UX3361 is ready for uploading data from/to the UX3361 RAM.



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Figure 5-2. The Initialization Sequence

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5.2.1 Data Integrity Checking

Table 5-2: The Value of Data Integrity Check

Addr	Register	Value(hex)
table 80h, 80h	EEPROMIdentifier	AA
table 80h, E6h	EEPROMchksum	Contains the low order 8 bits of the sum of table 81h(80h-E8h)，table 82h(80h-E8h)，table 83h(80h-E8h)，table 84h(80h-D3h,D6h-DDh,E0h-EAh) ,table 85h(80h-94h,A0h-AAh,B0h-B7h,C0h-D4h),table 86h(80h-A9h) and table 80h(81h-B6h,B8h-E5h)

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On power-up, UX3361 will attempt to load data to RAM from the EEPROM. If reading EEPROM fails due to a problem on TWI, such as not being correctly acknowledged for three times, then the corresponding bits of the INIT_STATE and EEPROM_FAIL_FLAG0 register will be both set to '1' and initialization will be stalled. After data transfer is finished, the data integrity will be checked. The check process is carried out in the following sequence of events.

First, after communicating with EEPROM, UX3361 will accumulate an 8 bit checksum for the A0h ram address range from 00h to 3Eh. If this accumulated checksum isn't equal to data stored in A0h ram address 3Fh, it tries for the second time. If it fails again, then dsfail0 will be set to '1'.

Second, UX3361 will accumulate an 8 bit checksum for the A0h ram address range from 40h to 5Eh. If this accumulated checksum isn't equal to data stored in A0h ram address 5Fh, it tries for the second time. If it fails again, then dsfail1 will be set to '1'.

Third, UX3361 will accumulate an 8 bit checksum for the A2h ram address range from 00h to 5Eh. If this accumulated checksum isn't equal to data stored in A2h ram address 5Fh, it tries for the second time. If it fails again, then dsfail2 will be set to '1'.

Four, UX3361 compare the byte read from addresses at EEPROMIdentifier (table 80h, 80h) with the value show in Table 5-2. If there is a mismatch, tries for the second time. If it fails again, then dsfail3 is set to '1', and the initialization will be stalled.

If EEPROMIdentifier=AAh, then UX3361 will accumulate an 8 bit checksum in the region of A2h RAM(table 81h(80h-E8h), table 82h(80h-E8h), table 83h(80h-E8h), table

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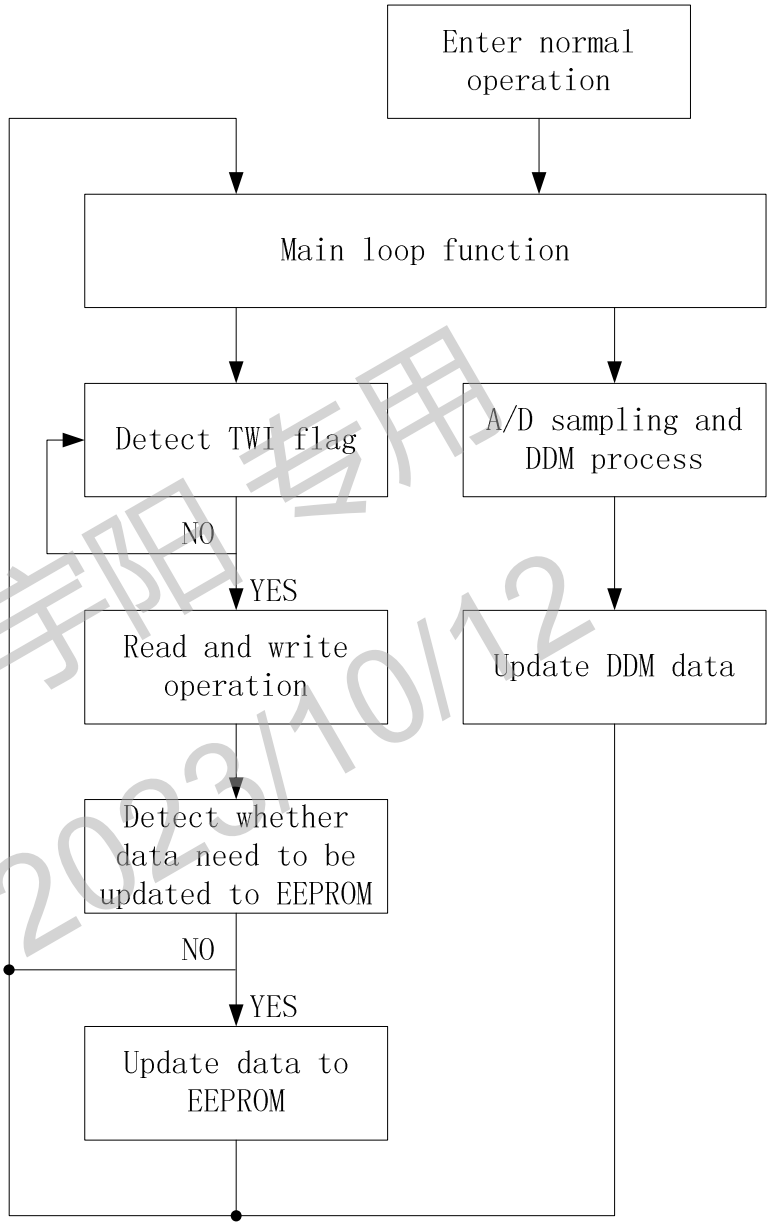
84h(80h-D3h, D6h-DDh,E0h-EAh), table 85h(80h-94h, A0h-AAh, B0h-B7h, C0h-D4h), table 86h(80h-A9h) and table 80h(81h-B6h, B8h-E5h)). If this accumulated checksum isn't equal to the EEPROMchksum byte, it tries for the second time. If it fails again, then dsfail3 will be set to '1', and initialization will be stalled.

Once all checks are complete, the hardware registers in the UX3361 are updated from the RAM, and the state machine will enable the 2-wire serial slave interface and enter the normal operation.

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5.3 Main Control loop



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Figure 5-3. Main Control Loop Function

After initialization，the main controller mainly runs the following two operating loops:

First, the controller transacts with the host, writing data from host to ram or reading data from ram to host. When UX3361 detects a write operation, the controller set the internal flag to '1', then the data is updated into the EEPROM. To ensure the transaction with the

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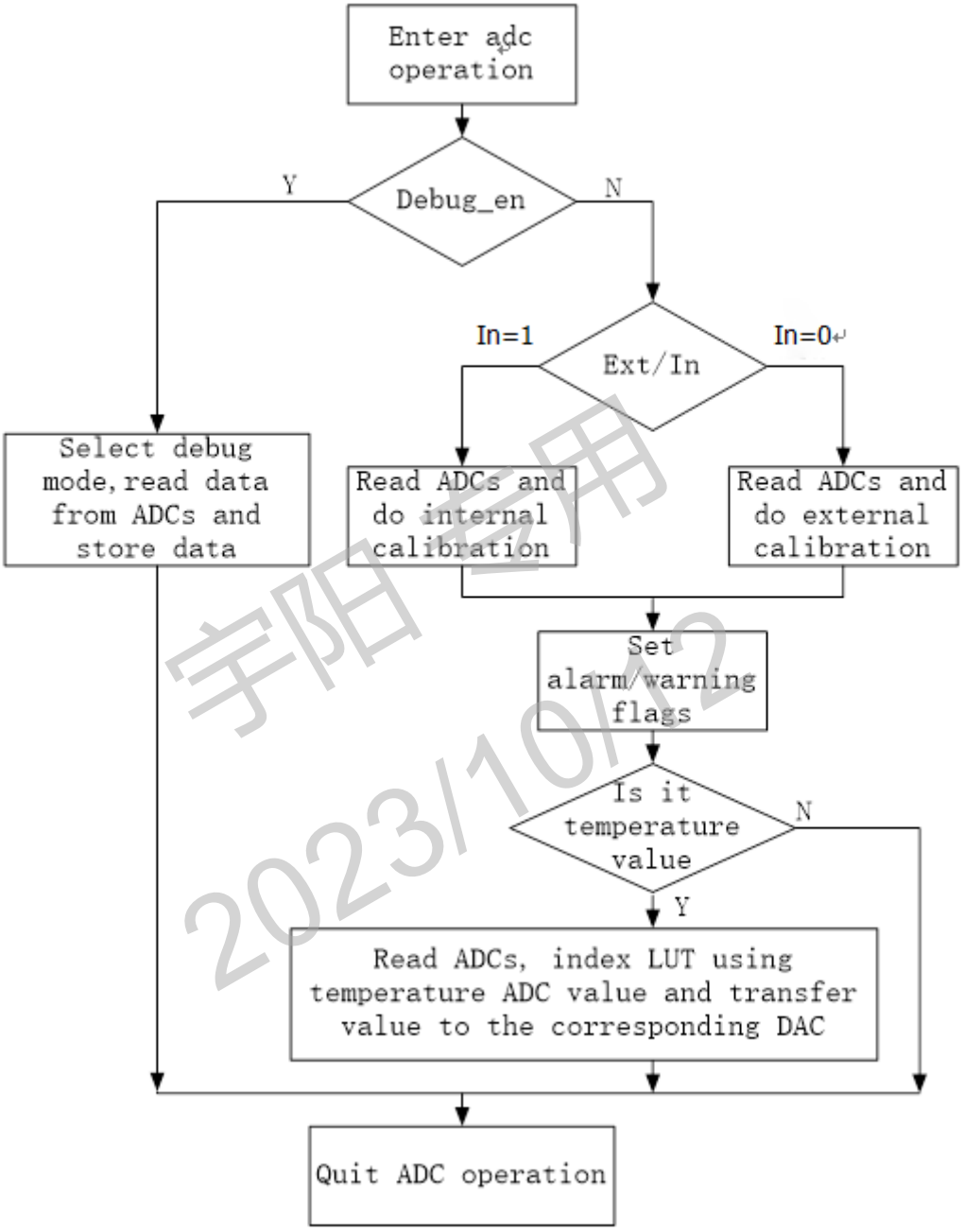
IIC is correct, the operation is set to the highest priority in the main state machine;

Second, the controller deals with A/D sampling of five analog monitors, including Supply Voltage, Temperature, Tx Bias current, Tx Power and RXPower, and runs digital diagnose and monitor function, including storage, internal and external calibration, and setting of the alarm and warning flags.

5.3.1 ADC_CTRL LOOP(Internal/External calibration、alarm and warning judgement)

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Figure 5-4. ADC Control Loop and DDM Function

After the main state machine enter in the ADC control operation, the controller check register bit 'debug_en'(table 80h, E5h, bit 5). If the bit is '1', the main state machine sets the debug mode, reads data from ADCs, and store in the register DEBUG_DATA(table 87h, 87-88h).If the bit is '0', the controller will check the register bits 'In' (table 80h, E5h, bit6).

If the register bit 'In' is '0', the controller reads the ADCs and do the external calibration; If

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the register bit 'In' is '1', the controller reads the ADCs and do the internal calibration.

After the calibration, the controller reads the preset alarm/warning thresholds of the five analog monitors, then compares with the corresponding calibrated data and sets the alarm/warning flags.

An external host is required to apply the correct calibration slope and offset values to the UX3361 in order that DDM and the real time reports are meaningful. The internal calibration for each analog is given by the following equation:

ADCcal = Slope * ADCraw + offset

ADCcal:the ADC value after calibration

ADCraw:the raw ADC value after shift

Slope and offset are stored in the ram which are calculated by host. Table 5-3 shows the memory locations of the five analog signal.

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Table 5-3: The Register Locations of DDM Parameter

Address(hex)	Name	Width(bit)
BA-BBh	TEMP_SLOPE2	16
BC-BDh	TEMP_OFFSET2	16
BE-BFh	TEMP_SLOPE1	16
C0-C1h	TEMP_OFFSET1	16
C2-C3h	TEMP_SLOPE0	16
C4-C5h	TEMP_OFFSET0	16
C6-C7h	VCC_SLOPE	16
C8-C9h	VCC_OFFSET	16
CA-CBh	BIAS_SLOPE	16
CC-CDh	BIAS_OFFSET	16
CE-CFh	TX_SLOPE	16
D0-D1h	TX_OFFSET	16
D2-D3h	RX_SLOPE2	16
D4-D5h	RX_OFFSET2	16
D6-D7h	RX_SLOPE1	16
D8-D9h	RX_OFFSET1	16
DA-DBh	RX_SLOPE0	16
DC-DDh	RX_OFFSET0	16

UX3361 provides a three line calibration for temperature calibration (as shown in Tab 7). TEMP_COMP1(table 80h，B8h) and TEMP_COMP0(table 80h，B9h) is the two turning

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points.

Table 5-4: Three Line Temperature Calibration

ADC value	Slope	offset
ADCraw(8:1)>TEMP_COMP1	TEMP_SLOPE2	TEMP_OFFSET2
TEMP_COMP0<ADCraw(8:1)≤TEMP_COMP1	TEMP_SLOPE1	TEMP_OFFSET1
ADCraw(8:1)≤TEMP_COMP0	TEMP_SLOPE0	TEMP_OFFSET0

UX3361 provides a multi-slope and multi-offset for the RX POWER calibration (as shown in Tab 8). RX_COMP0 (table 80h, E0-E1h), and RX_COMP1 (table 80h, DE-DFh), is the two turning points of the calibration curve.

Table 5-5: A Multi-Slope and Multi-Offset for RX POWER Calibration

ADC value	Slope	offset
ADCraw≥RX_COMP1	RX_SLOPE2	RX_OFFSET2
RX_COMP0≤ADCraw<RX_COMP1	RX_SLOPE1	RX_OFFSET1
ADCraw<RX_COMP0	RX_SLOPE0	RX_OFFSET0

Table 5-6 shows the variable format of analog signals.

Table 5-6: Variable Format of Analog Signal

Analog signal	format
Temperature	Two's complement
Vcc	Unsigned
Bias	Unsigned
Tx power	Unsigned
Rx power	unsigned

5.3.2 Calculating the value of analog signal

Table 5-7: Temperature Bit Weights

Most Significant Byte(60h)							
D7	D6	D5	D4	D3	D2	D1	D0
SIGN	64	32	16	8	4	2	1
Most Significant Byte(61h)							
D7	D6	D5	D4	D3	D2	D1	D0
1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256

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Table 5-8: Temperature Conversion Examples

Temperature	Binary		HEX	
	HIGH BYTE	LOW BYTE	HIGH BYTE	LOW BYTE
25	00011001	00000000	19	00
1	00000001	00000000	01	00
0.004	00000000	00000001	00	01
-40	11011000	00000000	D8	00

To calculate the temperature, treat the two's complement value binary number as an unsigned binary number, then convert to decimal and divide by 256. If the result is greater than or equal to 128, subtract 256 from the result.

Temperature: high byte: -128℃ to +127℃ signed; low byte: 1/256℃

Table 5-9: Vcc/Bias/Tx power/Rx Power Bit Weights

MSB	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
LSB	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

The LSB = 100uV for Vcc, the LSB = 2uA for Bias, the LSB = 0.1uW for Tx Power and Rx Power when using factory default settings.

Table 5-10: Vcc Conversion Examples

Vcc	Binary		Hex	
	High byte	Low byte	High byte	Low byte
3.3V	10000000	11101000	80	E8
2.97V	01110100	00000100	74	04
3.63V	10001101	11001100	8D	CC

To calculate Vcc, convert the unsigned 16-bit value to decimal and multiply by 100uV.

Table 5-11: Bias Conversion Examples

Bias	Binary		Hex	
	High byte	Low byte	High byte	Low byte
131 mA	11111111	11011100	FF	DC
100 uA	00000000	00110010	00	32

To calculate Bias, convert the unsigned 16-bit value to decimal and multiply by 2uA.

Table 5-12: Tx power and Rx Power Conversion Examples

Tx power and Rx power	Binary	Hex

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mW	dBm	High byte	Low byte	High byte	Low byte
5	7.0	11000011	01010000	C3	50
0.1	-10	00000011	11101000	03	E8

To calculate Tx power and Rx power, convert the unsigned 16-bit value to decimal and multiply by 0.1uW.

5.3.3 Algorithm for temperature look-up table

5.3.3.1 BIAS Current and Mod Current and APD Voltage TLUT

Table 5-13: Bias Current and Mod Current and APD Voltage TLUT

Temperature ADC value (hex)	CORRESPONDING LOOK-UP TABLE ADDRESS
<56	80h+81(7:6)h
56	80h+81(7:6)h
5B	81(5:0)h+82(7:4)h
60	82(3:0)h+83(7:2)h
65	83(1:0)h+84h
6A	85h+86(7:6)h
6F	86(5:0)h+87(7:4)h
74	87(3:0)h+88(7:2)h
79	88(1:0)h+89h
-	-
1E6	E4h+E5(7:6)
1EB	E5(5:0)+E6(7:4)
1F0	E6(3:0)+E7(7:2)
1F5	E7(1:0)+E8h
>1F5	E7(1:0)+E8h

The temperature look-up table use the temperature ADC value as index, and for each temperature the corresponding look-up table DAC value are 10 bits wide, of which the higher byte stored in the lower address, and lower byte stored in the higher address. The algorithm used is described below:

Index = TEMP_DATA-56h

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Index1 = round(Index/5)

addr0 = Index1+(Index1>>2)+80h

addr1 = addr0+1

Table 5-14 shows the relationship between the index value and the address:

Table 5-14: The Relationship between Index Value and Address

Index value Index 1 for low two bits	Corresponding look-up table address
00	addr0(7:0)+addr1(7:6)
01	addr0(5:0)+addr1(7:4)
10	addr0(3:0)+addr1(7:2)
11	addr0(1:0)+addr1(7:0)

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5.3.3.2 APC Current TLUT

Table 5-15: APC Current TLUT

Temperature ADC value (hex)	CORRESPONDING LOOK-UP TABLE ADDRESS
<56	80h+81(7:6)h, 81(5:0)h
56	80h+81(7:6)h, 81(5:0)h
60	82h+83(7:6)h, 83(5:0)h
6A	84h+83(7:6)h, 85(5:0)h
-	-
1E6	D0h+D1(7:6)h, D1(5:0)h
1F0	D2h+D3(7:6)h, D3(5:0)h
>1F0	D2h+D3(7:6)h, D3(5:0)h

The temperature look-up table use the temperature ADC value as index, and the corresponding look-up table DAC value of APC current for each temperature are 10 bits and 6 bits, of which the higher byte stored in the lower address, and lower in the higher address. The algorithm used is described below:

Index = TEMP_DATA-56h

Index1 = round(Index/10)

addr0 = Index1<<1+80h

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addr1 = addr0+1

note: pa_set ={addr0,addr1(7:6)}, Reserved=addr1(5:0)

5.3.3.3 LOS Alarm Threshold TLUT

Table 5-16: LOS Alarm Threshold TLUT

Temperature ADC value (hex)	CORRESPONDING LOOK-UP TABLE ADDRESS
<56	C0h
56	C0h
6A	C1h
7E	C2h
A6	C3h
-	-
1D2	D3h
1E6	D4h
>1E6	D4h

The temperature look-up table use the temperature ADC value as index. The algorithm used is described below:

Index = TEMP_DATA-56h

Index1 = round(Index/5)

Addr0 = (Index1>>2)+C0h

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5.3.3.4 Dark Current TLUT

Table 5-17: Dark Current TLUT

Temperature ADC value (hex)	CORRESPONDING LOOK-UP TABLE ADDRESS
<56	80h
56	80h
6A	81h
7E	82h
A6	83h
-	-
1D2	93h
1E6	94h

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>1E6	94h

The temperature look-up table use the temperature ADC value as index. The algorithm used is described below:

Index = TEMP_DATA-56h

Index1 = round(Index/5)

Addr0 = (Index1>>2)+80h

5.3.3.5 RX PE Decoder LUT

Table 5-18: RX PE Decoder LUT

value of 73(7-4)h(hex)	CORRESPONDING LOOK-UP TABLE ADDRESS
1	B0(7-4)h
2	B0(3-0)h
3	B1(7-4)h
4	B1(3-0)h
5	B2(7-4)h
6	B2(3-0)h
7	B3(7-4)h
8	B3(3-0)h
9	B4(7-4)h
A	B4(3-0)h
B	B5(7-4)h
C	B5(3-0)h
D	B6(7-4)h
E	B6(3-0)h
F	B7(7-4)h

If the value of 73(7:4)h is zero, then output DAC value should be zero.

5.3.3.6 TX EQ Decoder LUT

Table 5-19: TX EQ Decoder LUT

value of 73(7-4)h(hex)	CORRESPONDING LOOK-UP TABLE ADDRESS

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1	D6(7-4)h
2	D6(3-0)h
3	D7(7-4)h
4	D7(3-0)h
5	D8(7-4)h
6	D8(3-0)h
7	D9(7-4)h
8	D9(3-0)h
9	DA(7-4)h
A	DA(3-0)h
B	DB(7-4)h
C	DB(3-0)h
D	DC(7-4)h
E	DC(3-0)h
F	DD(7-4)h

If the value of 72(7:4)h is zero, then output DAC value should be zero.

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5.3.3.7 RX EQ TLUT

Table 5-20: RX EQ TLUT

Temperature ADC value (hex)	CORRESPONDING LOOK-UP TABLE ADDRESS
<56	A0(7:4)h
56	A0(7:4)h
6A	A0(3:0)h
7E	A1(7:4)h
92	A1(3:0)h
-	-
1D2	A9(3:0)h
1E6	AA(7:4)h
>1E6	AA(7:4)h

The temperature look-up table use the temperature ADC value as index. The algorithm used is described below:

Index = TEMP_DATA-56h

Index1 = round(Index/5)>>2

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Index2 = Index1>>1

addr0 = Index2+A0h

If Index1 is even, get the higher 4 bits of value looked up from addr0.

If Index1 is odd, get the lower 4 bits of value looked up from addr0.

5.3.3.8 TX EMP AMP TLUT

Table 5-21: TX EMP AMP TLUT

Temperature ADC value (hex)	CORRESPONDING LOOK-UP TABLE ADDRESS
<56	80(7:4)h
56	80(7:4)h
5B	80(3:0)h
60	81(7:4)h
65	81(3:0)h
-	-
1F0	A9(7:4)h
1F5	A9(3:0)h
>1F5	A9(3:0)h

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The temperature look-up table use the temperature ADC value as index. The algorithm used is described below:

Index = TEMP_DATA-56h

Index1 = round(Index/5)

Index2 = Index1>>1

addr0 = Index2+80h

If Index1 is even, get the higher 4 bits of value looked up from addr0.

If Index1 is odd, get the lower 4 bits of value looked up from addr0.

5.3.4 Password protection

Before attempting to read and write any data from memory, it is important to check the memory map provided in a subsequent description to verify what level of password is required. Password protection is effective both at slave default address A0 and A2 region.

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The UX3361 uses two 4-byte passwords to achieve three levels of access to various memory locations. The three levels of access are:

User Access: This is the default state after power-up. It allows read access to standard monitoring and status functions.

Level 1 Access: This allows access to customer data table in addition to everything granted by User access. This level is granted by entering Password 1 (PW1).

Level 2 Access: This allows access to all memory, settings, and features, in addition to everything granted by Level 1 and User access. This level is granted by entering Password 2 (PW2).

To obtain a particular level of access, the corresponding password must be entered in the Password Entry (PWE) bytes located in the Main Device at 7Bh to 7Eh. The value entered is compared to both the PW1 (table 80h, E7-EAh) and PW2 (table 80h, EB-EEh).respectively, to determine which access should be granted. Access is granted until the password is changed or until power is cycled.

Writing PWE is allowed under any level of access, although PWE can never be read.

Writing PW1 and PW2 requires PW2 access. However, PW1 and PW2 can never be read, even with PW2 access.

On power-up, PWE is set to all 1s (FFFFh). As long as neither of the passwords is ever changed to FFFFh, then User access is the power-up default.

The level of the UX3361 at slave default address A0 region, table 0 region, and A2h region can be changed to a level other than the default level (see description of address at table 80h, B4-B7h). To change the access level, the host writes a new value to the register of table 80h, B4-B7h. The level of password is described in Table 5-22.

Table 5-22: Access Region of Different Password Level

Region	Write	Read
A0 _lower	PW2/PW1/User	PW2/PW1/User
A0_upper	PW2/PW1/ User	PW2/PW1/User
A2_lower	PW2/PW1/User	User
User define	PW2/PW1/ User	PW2/PW1/User
CHIP SETTING	PW2	PW2
Bias Tlut	PW2	PW2
MOD Tlut	PW2	PW2
APD Tlut	PW2	PW2

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APC Tlut and TX EQ decoder	PW2	PW2
Dark current, RX EQ,RX PE and LOS Tlut	PW2	PW2
TX EMP AMP decoder	PW2	PW2

5.3.5 Data update and timer function

UX3361 in the I2C communication process has a self-reset function. When Timer (table 80h, E3h) is not 0, UX3361 will start the timer after detecting the address matched the device address. Once the counter exceeds the value, UX3361 will exit from the I2C communication, then enters the idle state and waits for the arrival of next communication. When the timer value is 0, the timer will be disabled.

5.4 2-wire Serial Interface

UX3361 has a pair of 2-wire serial interfaces: a slave for interfacing to a host for module setup and programming, and a master for interfacing to an external EEPROM for device configuration after power up. Both interfaces communicate using the protocol described in this section.

5.4.1 Framing and Data Transfer

The 2-wire interface comprises a clock line (SCL) and a data line (SDA). When the bus is idle, master SDA and SCL are pulled high within UX3361 by 10kΩ pull-ups.

An individual transaction is framed by a start condition and a stop condition. Within the frame, the master has exclusive control of the bus. UX3361 supports REPEAT START conditions where by the master may simultaneously end one frame and start another without releasing the bus by replacing the STOP condition with a START condition.

Within a frame, a data bit is transferred on a low-to-high transition of SCL. Data is arranged in packets of 9 bits. The first 8 bits represent data to be transferred (most significant bit first). The last bit is an acknowledge bit. The recipient of the data holds SDA low during the ninth clock cycle of a data packet to acknowledge (ACK) the byte. Leaving SDA to float high on the ninth bit signals a not-acknowledged (NACK) condition. The interpretation of the acknowledge bit by the sender will depend on the type of transaction and the nature of the byte being received.

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5.4.2 Device Addressing

Clock and Data Transitions: The SDA pin is normally pulled high with an external resistor or device. Data on the SDA pin may only change during SCL-low time periods. Data changes during SCL-high periods will indicate a START or STOP condition depending on the conditions discussed below.

START Condition: A high-to-low transition of SDA with SCL high is a START condition that must precede any other command.

STOP Condition: A low-to-high transition of SDA with SCL high is a STOP condition.

Acknowledge: All address and data bytes are transmitted through a serial protocol. The UX3361 pulls the SDA line low during the ninth clock pulse to acknowledge that it has received each word.

The first byte to be sent after a START condition is an address byte. The first seven bits of the byte contain the target slave address (MSB first). The eighth bit indicates the transaction type – '0' = write, '1' = read. Each slave interface on the bus is assigned a 7-bit slave address. If no slave matches the address broadcast by the master then SDA will be left to float high during the acknowledge bit and the master receives a NACK. Then the master must assert a STOP condition. If a slave identifies the address then it acknowledges the master and proceeds with the transaction.

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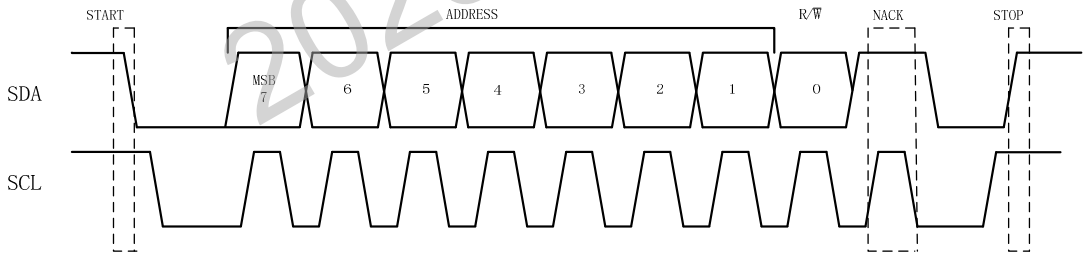


Figure 5-5. Address Decoding Example – Slave Not Addressing

5.4.3 Write Transaction

Figure 5-6 shows an example of a write transaction. The address byte is successfully acknowledged by the slave, and the type bit is set low to signify a write transaction. After acknowledge the master sends a single data byte. All signal is controlled by the master except for the SDA line during the acknowledge bits. During acknowledge the direction of the SDA line is reversed and the slave pulls SDA low to return a '0' (ACK) to the master.

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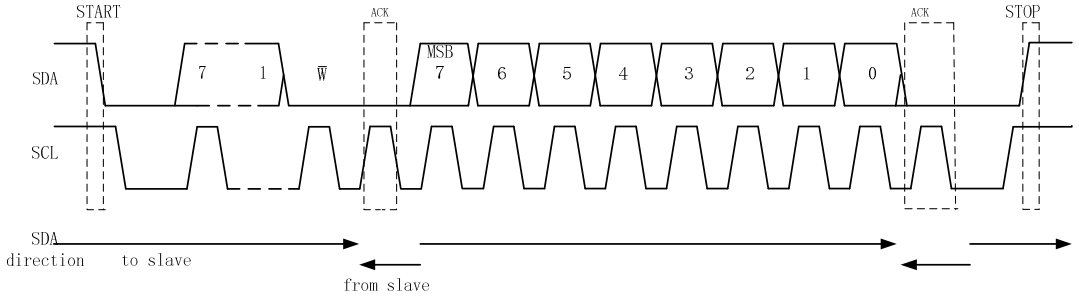


Figure 5-6. Write Transaction

If the slave is unable to receive data then it should return a NACK after the data byte. This will cause the master to issue a STOP and thus terminate the transaction.

UX3361 interprets the first data byte as a register address. This will be used to set an internal memory pointer. Subsequent data bytes within the same transaction will then be written to the memory location addressed by the pointer. The pointer is auto-incremented after each byte. There is no limit to the number of bytes which may be written in a single burst to the internal RAM in the UX3361. If, however, whether the controller needs to refresh data to EEPROM depends on the update flag for each transmission .the write access is destined for the EEPROM the requirements of page writes specified for the EEPROM application. The external EEPROM is 2k bytes, such as 24c16. The A2 hardware address pin of these EEPROMs should be connected to 0V.

If the slave is not ready to receive a byte then it may hold SCL low immediately after the acknowledge bit. When SCL is released the master starts to send the next byte. This is known as clock stretching. UX3361 slave interface will not clock stretch at up to 400 kHz SCL frequency.

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5.4.4 **Read Transaction**

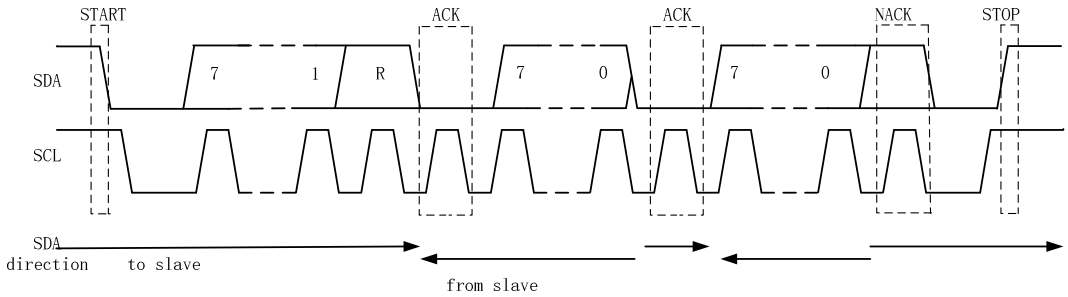


Figure 5-7. Read Transaction

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Figure 5-7 shows an example of a 2 bytes read transaction. The address byte is successfully acknowledged by the slave, and the type bit is set high to signify a read. After the ACK the slave returns a byte from the location identified by the internal memory pointer. This pointer is then auto-incremented. The slave then releases SDA so that the master can ACK the byte. If the slave receives an ACK then it will send another byte. The master identifies the last byte by sending a NACK to the slave. The master then issues a STOP to terminate the transaction.

Thus, to implement a random access read transaction, a write must first be issued by the master containing a slave address byte and a single data byte (the register address). A read is then sent to retrieve data from this address, as shown in Figure 5-6 and Figure 5-7.

6 Rgister Map

Where a single power-on reset (PoR) value is shown for a range of addresses, which value applies to all bytes in the range. Note that the power on reset values may be overwritten during initialization from the EEPROM.

For registers containing a single 8-bit field, the most significant bit of the field is stored in bit 7 of the register byte.

R Bit is read only. A write to this bit via the TWI will have no effect. The value may be changed by the device itself as part of its normal operation.

R/W Bit is readable and writable via the TWI. The value will not be changed by the device itself except under a device reset.

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6.1 Password permission

Table 6-1: Password Permission

Permission	Read	Write
A	USER	PW2/PW1/USER
B	USER	NA
C	PW2	PW2
D	USER	USER
E	PW1	PW1
F	USER	PW1

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G	NA	USER
H	NA	PW2
I	NA	NA

6.2 Digital diagnostics register

Table 6-2: Digital Diagnostics Registers

Addr(Hex)	Bytes	Name	Access
00-01	2	Temp High alarm	See SFF 8472 specification
02-03	2	Temp Low alarm	See SFF 8472 specification
04-05	2	Temp High warning	See SFF 8472 specification
06-07	2	Temp Low warning	See SFF 8472 specification
08-09	2	Voltage High alarm	See SFF 8472 specification
0A-0B	2	Voltage Low alarm	See SFF 8472 specification
0C-0D	2	Voltage High warning	See SFF 8472 specification
0E-0F	2	Voltage Low warning	See SFF 8472 specification
10-11	2	Bias High alarm	See SFF 8472 specification
12-13	2	Bias Low alarm	See SFF 8472 specification
14-15	2	Bias High warning	See SFF 8472 specification
16-17	2	Bias Low warning	See SFF 8472 specification
18-19	2	TX Power High alarm	See SFF 8472 specification
1A-1B	2	TX Power Low alarm	See SFF 8472 specification
1C-1D	2	TX Power High warning	See SFF 8472 specification
1E-1F	2	TX Power Low warning	See SFF 8472 specification
20-21	2	RX Power High alarm	See SFF 8472 specification
22-23	2	RX Power Low alarm	See SFF 8472 specification
24-25	2	RX Power High warning	See SFF 8472 specification
26-27	2	RX Power Low warning	See SFF 8472 specification
28-37	16	RESERVED	See SFF 8472 specification

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38-3B	4	Rx_PWR(4)	See SFF 8472 specification
3C-3F	4	Rx_PWR(3)	See SFF 8472 specification
40-43	4	Rx_PWR(2)	See SFF 8472 specification
44-47	4	Rx_PWR(1)	See SFF 8472 specification
48-4B	4	Rx_PWR(0)	See SFF 8472 specification
4C-4D	2	Tx_I(Slope)	See SFF 8472 specification
4E-4F	2	Tx_I(Offset)	See SFF 8472 specification
50-51	2	Tx_PWR(Slope)	See SFF 8472 specification
52-53	2	Tx_PWR(Offset)	See SFF 8472 specification
54-55	2	T (Slope)	See SFF 8472 specification
56-57	2	T(Offset)	See SFF 8472 specification
58-59	2	V(Slope)	See SFF 8472 specification
5A-5B	2	V(Offset)	See SFF 8472 specification
5C-5E	3	RESERVED	See SFF 8472 specification
5F	1	Checksum	See SFF 8472 specification
60-61	2	Temperature	See SFF 8472 specification
62-63	2	VCC	See SFF 8472 specification
64-65	2	Tx Bias	See SFF 8472 specification
66-67	2	TX Power	See SFF 8472 specification
68-69	2	RX Power	See SFF 8472 specification
6A-6D	4	RESERVED	See SFF 8472 specification
6E	1	STA_CTRL0	See SFF 8472 specification
6F	1	STA_CTRL1	See SFF 8472 specification
70-71	2	Alarm flags	See SFF 8472 specification
72	1	tx_eq_ctrl	TX input equalization control
73	1	rx_emphasis_ctrl	RX output emphasis control
74-75	2	Warning flags	See SFF 8472 specification
76-77	2	RESERVED	See SFF 8472 specification
78-7A	3	Vendor Specific	See SFF 8472 specification
7B-7E	4	PWE	Password Entry

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7F	1	table_select	table select byte

6.3 Table 00/01h

Table 6-3: Table 00/01h

addr(hex)	Bytes	Name	Access
80-F7	120	User EEPROM	See SFF 8472 specification
F8-FF	8	Vendor Specific	See SFF 8472 specification

6.4 Table 80h

Table 6-4: Table 80h

Addr(hex)	Bytes	Name	Access	Description
80	1	EEPROMIdentifier	C	Pro number/ load check
81	1	TX_CTRL0	C	TX controls
82	1	TX_CTRL1	C	TX controls
83	1	TX_CTRL2	C	TX controls
84	1	TX_CTRL3	C	TX controls
85	1	Biasmax	C	Set the maximum bias current in close loop
86-87	2	BIASPRE	C	Set the constant bias current
88-89	2	Imodc	C	Set the constant mod current
8A	1	TX_CTRL4	C	TX controls
8B	1	TX_CTRL5	C	TX controls
8C	1	TX_CTRL6	C	TX controls
8D-8E	2	PA_SETC	C	Set the constant average optical power
8F	1	TX_CTRL7	C	TX controls
90	1	TX_CTRL8	C	TX controls
91	1	Imodmax	C	set the high 8 bit of maximum Imod DAC in close loop
92	1	TX_CTRL9	C	TX controls
93-94	2	TX_PD	C	RESERVED
95	1	TX_CTRL10	C	TX controls

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96	1	TX_CTRL11	C	TX controls
97	1	TX_CTRL12	C	TX controls
98	1	TX_CTRL13	C	TX controls
99	1	TX_CTRL14	C	TX controls
9A	1	TX_CTRL15	C	TX controls
9B	1	TX_CTRL16	C	TX controls
9C	1	TX_CTRL17	C	TX controls
9D	1	TX_CTRL18	C	TX controls
9E	1	APD_DA_CTRL0	C	APD and DA controls
9F-A0	2	APD_TARGET	C	Set the constant APD target voltage
A1-A2	2	DROP_VALUE	C	Set the APD drop value when it is in smart over-current protection
A3	1	APD_DA_CTRL1	C	APD and DA controls
A4	1	APD_DA_CTRL2	C	APD and DA controls
A5	1	APD_DA_CTRL3	C	APD and DA controls
A6	1	APD_DA_CTRL4	C	APD and DA controls
A7	1	APD_DA_CTRL5	C	APD and DA controls
A8	1	ANA_CTRL	C	Analog controls
A9	1	RX_CTRL1	C	RX controls
AA	1	RX_CTRL2	C	RX controls
AB	1	RX_CTRL3	C	RX controls
AC	1	RX_CTRL4	C	RX controls
AD	1	LOSCTRLC	C	The constant alarm threshold controls
AE	1	RX_CTRL5	C	RX controls
AF	1	RX_CTRL6	C	RX controls
B0	1	SYS_CTRL1	C	System controls
B1	1	SYS_CTRL2	C	System controls
B2	1	SYS_CTRL8	C	System controls
B3	1	TX_LOCK_TIMER	C	Set the hold-off time for TX optical power when BEN is de-assert
B4	1	SYS_CTRL3	C	System controls
B5	1	SYS_CTRL4	C	System controls
B6	1	SYS_CTRL5	C	System controls
B7	1	SYS_CTRL6	C	System controls

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B8	1	TEMP_COMP1	C	High turning point of temperature internal calibration
B9	1	TEMP_COMP0	C	Low turning point of temperature internal calibration
BA-BB	2	TEMP_SLOPE2	C	Slope2 for temperature internal calibration
BC-BD	2	TEMP_OFFSET2	C	Offset2 for temperature internal calibration
BE-BF	2	TEMP_SLOPE1	C	Slope1 for temperature internal calibration
C0-C1	2	TEMP_OFFSET1	C	Offset1 for temperature internal calibration
C2-C3	2	TEMP_SLOPE0	C	Slope0 for temperature internal calibration
C4-C5	2	TEMP_OFFSET0	C	Offset0 for temperature internal calibration
C6-C7	2	VCC_SLOPE	C	Slope for supply voltage internal calibration
C8-C9	2	VCC_OFFSET	C	Offset for supply voltage internal calibration
CA-CB	2	BIAS_SLOPE	C	Slope for bias current internal calibration
CC-CD	2	BIAS_OFFSET	C	Offset for bias current internal calibration
CE-CF	2	TX_SLOPE	C	Slope for transmit power internal calibration
D0-D1	2	TX_OFFSET	C	Offset for transmit power internal calibration
D2-D3	2	RX_SLOPE2	C	Slope2 for received power internal calibration
D4-D5	2	RX_OFFSET2	C	Offset2 for received power internal calibration
D6-D7	2	RX_SLOPE1	C	Slope1 for received power internal calibration
D8-D9	2	RX_OFFSET1	C	Offset1 for received power internal calibration

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DA-DB	2	RX_SLOPE0	C	Slope0 for received power internal calibration
DC-DD	2	RX_OFFSET0	C	Offset0 for received power internal calibration
DE-DF	2	RX_COMP1	C	High turning point of received power internal calibration
E0-E1	2	RX_COMP0	C	Low turning point of received power internal calibration
E2	1	SYS_CTRL7	C	System controls
E3	1	Timer	C	Set the interrupt time of slave I2C
E4	1	SLAVE_ADDRESS	C	Device address of slave I2C
E5	1	DDM_CTRL	C	DDM controls
E6	1	EEPROMchksum	C	Checksum byte
E7-EA	4	PW1	H	Level 1 access password (PW1)
EB-EE	4	PW2	H	Level 2 access password (PW2)
EF	1	TX_STATUS1	B	TX fault status indicator register
F0-F1	2	BIASCT_R	B	The bias current DA display registers
F2-F3	2	IMOD_DAC	B	The I_{mod} current DA display registers
F4	1	STATUS0	B	Status register
F5	1	STATUS1	B	Status register
F6	1	STATUS2	B	Status register
F7-F8	2	TEMP_DATA	B	ADC value of the sampled temperature
F9-FA	2	RX_ADC_VALUE	B	ADC value of the sampled RX POWER
FB-FC	2	APD_VOL	B	ADC value of the sampled APD voltage
FD	1	SYS_STATUS	B	Chip password access permission level indicator
FE	1	INIT_STATE	B	Indicate the initialization status after power up

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FF	1	EEPROM_FAIL_FLAG1	B	The register indicate Whether the data is written to EEPROM

6.5 Table 81h

Table 6-5: Table 81h

Addr(hex)	Bytes	Name	Access	Description
80-E8	105	BIAS TLUT	C	Temperature Indexed BIAS Current Look-Up Table
E9-EA	2	BIASTLUT(9:0)	B	BIAS current displaying register
EB-FF	21	RESERVED	I	RESERVED

Note: BIASTLUT = {E9h, EA(1:0)h}

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6.6 Table 82h

Table 6-6: Table 82h

Addr(hex)	Bytes	Name	Access	Description
80-E8	105	MOD TLUT	C	Temperature Indexed Imod Current Look-Up Table
E9-EA	2	IMOD(9:0)	B	MOD current displaying register
EB-FF	21	RESERVED	I	RESERVED

Note: IMOD = {E9h, EA(1:0)h}

6.7 Table 83h

Table 6-7: Table 83h

Addr(hex)	Bytes	Name	Access	Description

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80-E8	105	APD TLUT	C	Temperature Indexed APD voltage Look-Up Table
E9-EA	2	APD_DAC(9:0)	B	APD voltage displaying register
EB-FF	21	RESERVED	I	RESERVED

Note:APD_DAC={E9h,EA(1:0)h}

6.8 Table 84h

Table 6-8: Table 84h

Addr(hex)	Bytes	Name	Access	Description
80-D3	84	APC TLUT	C	Temperature Indexed APC current Look-Up Table
D4-D5	2	PA_SET	B	PA current displaying register
D6-DD	8	TX EQ LUT	C	TX EQ decoder
DE	1	TX_EQSET	B	TX EQ displaying register
DF	1	RESERVED	I	RESERVED
E0	1	TX_EMP_THR	C	Set the temperature thresthold value of Tx emp Tlut
E1	1	SYS_CTRL9	C	System controls
E2	1	SYS_CTRL10	C	System controls
E3	1	DOCSETC	C	Set the constant DAC value of TX DC offset
E4	1	TX_CTRL19	C	TX controls
E5	1	TX_CTRL20	C	TX controls
E6	1	TX_CTRL21	C	TX controls
E7	1	RESERVED	C	Internal use
E8	1	TX_CTRL22	C	TX controls
E9	1	TX_CTRL23	C	TX controls
EA	1	Vdcdc	C	TX controls
EB	1	TX_STATUS2	B	TX status register
EC	1	DOCSET	B	indicate the DAC value of TX DC offset
ED-FF	19	RESERVED	I	RESERVED

Note: pa_set = {D4h, D5(7:6)h}, Reserved = D5(5:0)h, tx_eqset = DE(3:0)h

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6.9 Table 85h

Table 6-9: Table 85h

Addr(hex)	Bytes	Name	Access	Description
80-94	21	Dark current TLUT	C	Temperature Indexed dark current Look-Up Table
95-96	2	RX_DARK_CURR(15:0)	B	Dark current displaying register
97-9F	9	RESERVED	I	RESERVED
A0-AA	11	RX EQ TLUT	C	Temperature Indexed RX EQ Look-Up Table
AB	1	Rx_eqset(3:0)	B	RX EQ displaying register
AC-AF	4	RESERVED	I	RESERVED
B0-B7	8	RX PE LUT	C	RX PE decoder
B8	1	Pectrl(3:0)	B	RX PE displaying register
B9-BF	7	RESERVED	I	RESERVED
C0-D4	21	LOS TLUT	C	Temperature Indexed LOS alarm threshold Look-Up Table
D5	1	LOSDAC(7:0)	B	The threshold of LOS
D6-FF	42	RESERVED	I	RESERVED

Note: rx_eqset = AB(3:0)h, pectrl = B8(3:0)h

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6.10 Table 86h

Table 6-10: Table 86h

Addr(hex)	Bytes	Name	Access	Description
80-A9	42	TX emp amp TLUT	C	Temperature Indexed TX emp amp Look-Up Table
AA	1	Emp_amp(4:0)	B	TX EMP amplitude displaying register
AB-FF	85	RESERVED	I	RESERVED

Note: emp_amp = AA(4:0)h

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6.11 Table 87h

Table 6-11: Table 87h

Addr(hex)	Bytes	Name	Access	Description
80-86	7	Chip_id	B	Chip identifier 55_58_33_33_36_33_31h
87-88	2	Debug_data(9:0)	I	Indicate the ADC value of the sampled data in debug mode
89-FF	119	RESERVED	I	RESERVED

6.12 Register Descriptions

Table 6-12: Register Descriptions

6Eh	STA_CTRL0			Optional status/control bits Note:PON_EN **bit must be set to enable bit 5 and bit 3**
Bit	Field name	Type	Por	
7	TX Disable State	R	0	Digital state of the TX Disable Input Pin. Updated within 100msec of change on pin.
6	Soft TX Disable	R/W	0	Read/write bit that allows software disable of laser. Writing '1' disables laser. Turn on/off time is 100 msec max from acknowledgement of serial byte transmission. This bit is 'OR'd with the hard TX_DISABLE pin value. Note, per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is 0.
5	Rogue_onu	R	0	Set to 1 if a ROGUE_ONU condition has been detected.
4	Apd_fault	R/W	0	Set to 1 if either an APD over-voltage or over-current event has been detected.
3	Rogue_txp_lo_flag	R/W	0	Set to 1 if the TXP_LO_FLAG has been set by the alarm threshold and the Rogue_txp_lo_en bit is set. Latched (default) or non-latched.
2	LtchFt_R	R	0	Digital state of the TX Fault Output Pin. Updated within 100msec of change on pin.

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1	LOS	R	0	Digital state of the LOS Output Pin. Updated within 100msec of change on pin.
0	Data_Ready_Bar	R	1	Indicates transceiver has achieved power up and data is ready. Bit remains high until data is ready to be read at which time the device sets the bit low.

6Fh	STA_CTRL1			Optional status/control bits
Bit	Field name	Type	Por	Note:PON_EN **bit must be set to enable this register**
7	RESERVED	R/W	0	RESERVED
6	TX_FAST_SLEEP	R/W	0	Fast start up after sleep 0: disable 1: enable
5	RX_SOFT_SLEEP	R/W	0	RX sleep soft shutdown function 0: disable 1: enable
4	RESERVED	R	0	RESERVED
3	TX_SOFT_SLEEP	R/W	0	TX sleep soft shutdown function 0: disable 1: enable
2	TX_SLEEP_STATE	R	0	TX SLEEP pin state
1	APCSCALE(1)	R/W	0	Set optical power attenuation coefficient
0	APCSCALE(0)	R/W	0	00: 0db 01: 3db 10/11: RESERVED

72h	tx_eq_ctrl			TX input equalization control
Bit	Field name	Type	Por	
7	TX_eqset(3)	R/W	0	When R114_SEL= 1, Transmitter input equalizer compensation control: 0000: 0dB
6	TX_eqset(2)	R/W	0	
5	TX_eqset(1)	R/W	0	

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4	TX_eqset(0)	R/W	0	0001:0.6dB 0010:1.2dB 0011:1.8dB 0100:2.4dB 0101:3.0dB 0110:3.6dB 0111:4.2dB 1000:4.8dB 1001:5.4dB 1010:6.0dB 1011:6.6dB 1100:7.2dB 1101:7.8dB 1110:8.4dB 1111:9.0dB
3	TX_eqset(3)	R/W	0	When R114_SEL= 0, Transmitter input equalizer compensation control: 0000: 0dB 0001:0.6dB 0010:1.2dB 0011:1.8dB 0100:2.4dB 0101:3.0dB 0110:3.6dB 0111:4.2dB 1000:4.8dB 1001:5.4dB 1010:6.0dB 1011:6.6dB 1100:7.2dB 1101:7.8dB 1110:8.4dB 1111:9.0dB
2	TX_eqset(2)	R/W	0	
1	TX_eqset(1)	R/W	0	
0	TX_eqset(0)	R/W	0	

73h	rx_emphasis_ctrl			RX output emphasis control
Bit	Field name	Type	Por	
7	Pectrl(3)	R/W	0	When R115_sel=1, RX output pre-emphasis to compensated for losses in the PCB between the
6	Pectrl(2)	R/W	0	

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5	Pectrl(1)	R/W	0	chip and the MAC.
4	Pectrl(0)	R/W	0	0000: 0mV Vppd 0001: 20mV Vppd 0010: 40mV Vppd 0011: 60mV Vppd 0100: 80mV Vppd 0101: 100mV Vppd 0110: 120mV Vppd 0111: 140mV Vppd 1000: 160mV Vppd 1001: 180mV Vppd 1010: 200mV Vppd 1011: 220mV Vppd 1100: 240mV Vppd 1101: 260mV Vppd 1110: 280mV Vppd 1111: 300mV Vppd
3	Pectrl(3)	R/W	0	When R115_sel=0, RX output pre-emphasis to compensated for losses in the PCB between the chip and the MAC. 0000: 0mV Vppd 0001: 20mV Vppd 0010: 40mV Vppd 0011: 60mV Vppd 0100: 80mV Vppd 0101: 100mV Vppd 0110: 120mV Vppd 0111: 140mV Vppd 1000: 160mV Vppd 1001: 180mV Vppd 1010: 200mV Vppd 1011: 220mV Vppd 1100: 240mV Vppd 1101: 260mV Vppd 1110: 280mV Vppd 1111: 300mV Vppd
2	Pectrl(2)	R/W	0	
1	Pectrl(1)	R/W	0	
0	Pectrl(0)	R/W	0	

7B-7Eh	PWE	Controls read/write access to registers. Level 1

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Type	W	Por	FFh	access when PWE = PW1. Level 2 access when PWE = PW2.

7Fh	TABLE_SELECT			Indicate the map address for register tables.
Type	R/W	Por	00h	

80h	EEPROMIdenfier			Pro number/ load check, the value must be equal to AAh
Type	R/W	Por	00h	

81h	TX_CTRL0			TX controls
Bit	Field name	Type	Por	
7	tx_sd_rogue_time(3)	R/W	0	Set the amount of time the TX_SD has to be asserted HIGH continuously before a ROGUE_ONU flag is set. 0000: inhibit 0001: 1.64ms 0010: 3.28ms 0011: 6.55ms 0100: 13.11ms 0101: 26.21ms 0110: 52.43ms 0111: 104.86ms 1000: 209.72ms 1001: 419.43ms 1010: 838.86ms 1011: 1.68s 1100: 3.36s 1101: 3.36s 1110: 3.36s 1111: 3.36s
6	tx_sd_rogue_time(2)	R/W	0	
5	tx_sd_rogue_time(1)	R/W	0	
4	tx_sd_rogue_time(0)	R/W	0	
3	ben_rogue_time(3)	R/W	0	Set the amount of time the BEN inputs have to be asserted HIGH before a ROGUE_ONU flag is set.
2	ben_rogue_time(2)	R/W	0	
1	ben_rogue_time(1)	R/W	0	

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0	ben_rogue_time(0)	R/W	0	0000: inhibit 0001: 1.64ms 0010: 3.28ms 0011: 6.55ms 0100: 13.11ms 0101: 26.21ms 0110: 52.43ms 0111: 104.86ms 1000: 209.72ms 1001: 419.43ms 1010: 838.86ms 1011: 1.68s 1100: 3.36s 1101: 3.36s 1110: 3.36s 1111: 3.36s

82h	TX_CTRL1			TX controls
Bit	Field name	Type	Por	
7	SOFT_TX_DIS_INHIBIT	R/W	0	Set to disable SOFT_TX_DISABLE (A2 lower 0x6E bit 6). 0: disable 1: enable
6	RESERVED	R/W	0	Internal use
5	Rogue_tx_dis	R/W	0	Set to disable the transmitter if a ROGUE_ONU flag occurs. 0: disable 1: enable
4	Rogue_onu_latch_inhibit	R/W	0	Set to inhibit latching behavior of ROGUE ONU. 0: disable 1: enable
3	Tx_dis_onu_clr_en	R/W	0	Control of clearing of ROGUE_ONU flag by toggling the TX_DISABLE function. 0: disable clearing of ROGUE_ONU flag 1: enable clearing of ROGUE_ONU flag

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2	Rogue_txp_lo_en	R/W	0	Set to generate a Rogue ONU event on TX Power Low Alarm assertion (70(0)h). 0: disable 1: enable
1	Tx_disable_on_rx_los	R/W	0	Control of the Transmitter to be disabled on assertion of the Rx LOS output. Timing needs to be compliant with hardware timing for SFF-8472. 0: TX NOT disabled on RX LOS 1: TX disabled on RX LOS
0	Soft_tx_dis_sel	R/W	0	Set the value of SOFT_TX_DISABLE on power-up 0: SOFT_TX_DISABLE=1 on power-up 1: SOFT_TX_DISABLE=0 on power-up

83h	TX_CTRL2			TX controls
Bit	Field name	Type	Por	
7	Bsluten	R/W	0	Set Bias TLUT enable signal 0: disable 1: enable
6	ModLutEn	R/W	0	Set MOD TLUT enable signal 0: disable 1: enable
5	Lpow	R/W	0	TX power control bit 0: normal 1: low power
4	CL_OLn	R/W	0	Select the close/open loop mode 0: open loop 1: close loop
3	Inpolsw	R/W	0	Select the polarity of the signal channel 0: in-phase 1: reverse
2	Ftshdnen	R/W	0	Set to enable the function of shutting down the laser while Fault 0: not shutting down the laser while Fault 1: shutting down the laser while Fault
1	RESERVED	R/W	0	RESERVED

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0	Starten_nclr	R/W	0	Control of clearing the 9D(1)h register for initial failure on power-up 0: NOT clearing the 9D(1)h register 1: clearing the 9D(1)h register

84h	TX_CTRL3			TX controls
Bit	Field name	Type	Por	
7	Apcfsst	R/W	0	set the function of the fast apc 0: disable 1: enable
6	txsdset(1)	R/W	0	Set the TX_SD current is corresponds to a proportion of the APCSET current. 00: 12.5% of Iapcset 01: 20.8% of Iapcset 10: 29% of Iapcset 11: 37.5% of Iapcset
5	txsdset(0)	R/W	0	
4	BW_CTRL	R/W	0	Select the bandwidth of the transmitting channel 0: low 1: high
3	RESERVED	R/W	0	Internal use
2	RESERVED	R/W	0	
1	RESERVED	R/W	0	
0	RESERVED	R/W	0	

85h	Biasmax			Set the maximum bias current in close loop
Type	R/W	Por	00h	

86h	Biaspre1			Set the upper 8 bits of constant bias current
Type	R/W	Por	00h	

87h	Biaspre0			TX controls
Bit	Field name	Type	Por	
7:2	RESERVED	R/W	000000	Internal use
1	Biaspre(1)	R/W	0	Set the lower 2 bits of constant bias current
0	Biaspre(0)	R/W	0	

88h	Imodc1	Set the upper 8 bits of constant Imod current

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Type	R/W	Por	00h	

89h	Imodc0			TX controls
Bit	Field name	Type	Por	
7:2	RESERVED	R/W	000000	Internal use
1	Imodc(1)	R/W	0	Set the lower 2 bits of constant Imod current
0	Imodc(0)	R/W	0	

8Ah	TX_CTRL4			TX controls
Bit	Field name	Type	Por	
7	Pon_en	R/W	0	Control of PON control functions in A2h Lower registers: 6Eh, 6Fh 0: disable PON control functions 1: enable PON control functions
6	RESERVED	R/W	0	RESERVED
5	Bsmaxprotect	R/W	0	the protection function of bias over-current 0: disable 1: enable
4	BIAS_half	R/W	0	The reference current of the bias current is halved 0: the default reference current 1: the reference current and the full range current are halved
3	MOD_half	R/W	0	The reference current of the modulation current is halved 0: the default reference current 1: the reference current and the full range current are halved
2	Apcscale_en	R/W	0	Select the source of the average optical power down level when power up. 0: Values from apcscale 1: Values from apcscaleset
1	Apcscaleset(1)	R/W	0	Power-up initialization, set the average optical power down level(Power Leveling) 00: 0dB 01: -3dB 10/11: RESERVED
0	Apcscaleset(0)	R/W	0	

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8Bh	TX _CTRL5			TX controls
Bit	Field name	Type	Por	
7	Burst0_cm1	R/W	0	Set the operating mode of TX 0: burst mode 1: continuous mode
6	Apcrange(1)	R/W	0	Set APC hysteresis comparator range 00: 1% 01: 2% 10: 3% 11: 5%
5	Apcrange(0)	R/W	0	
4:3	RESERVED	R/W	00	Internal use
2	BEN_pch	R/W	0	Select the polarity of the BEN signal 0: in-phase 1: reverse
1	CMOS_SEL	R/W	0	TX SD output voltage level 0: TTL 1: CMOS
0	Soft_tx_sleep_en	R/W	0	Set to disable to use SOFT_TX_DISABLE as TX_SLEEP control when txd0_sleep1 is set to '1'. 0 :disable 1 :enable

8Ch	TX_CTRL6			TX controls
Bit	Field name	Type	Por	
7	Fault_pol	R/W	0	Select the polarity of TX_fault 0: high level alarm 1: low level alarm
6	FaultSet(6)	R/W	0	Set the qualifications of TX FAULT 0: disable 1: enable FaultSet(0): VDD>4.3V FaultSet(1): Whether internal current source is working properly FaultSet(2): LDOP or LDON short to ground FaultSet(3): BIASP short to ground FaultSet(4): BIAS > or = BIASMAX FaultSet(5): When a rogue ONU is detected(BEN signal is low and the TX_SD signal is high) FaultSet(6): Light-emitting detection
5	FaultSet(5)	R/W	0	
4	FaultSet(4)	R/W	0	
3	FaultSet(3)	R/W	0	
2	FaultSet(2)	R/W	0	
1	FaultSet(1)	R/W	0	
0	FaultSet(0)	R/W	0	

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8Dh	PA_SETC1			Set the upper 8 bits of the average optical power
Type	R/W	Por	00h	

8Eh	PA_SETC0			TX controls
Bit	Field name	Type	Por	
7:2	RESERVED	R/W	000000	Internal use
1	PA_SETC(1)	R/W	0	Set the lower 2 bits of the average optical power
0	PA_SETC(0)	R/W	0	

8Fh	TX_CTRL7			TX controls
Bit	Field name	Type	Por	
7:3	RESERVED	R/W	00000	Internal use
2	Vout_sel	R/W	0	Select the connection to the cathode of the laser 0: connect to LDOP 1: connect to LDON
1	IN_PCH_DL	R/W	0	select to increase overshoot or undershoot compensation for the TX output 0: overshoot compensation 1: undershoot compensation
0	RESERVED	R/W	0	Internal use

90h	TX_CTRL8			TX controls
Bit	Field name	Type	Por	
7:1	RESERVED	R/W	0000000	Internal use
0	IBIAS_SEL	R/W	0	Set IOUTN PIN character 0: IOUTN no internal pull up resistor to TX VDD 1: IOUTN with internal pull up resistor to TX VDD

91h	Imodmax			set the high 8 bit of maximum Imod DAC in close loop
Type	R/W	Por	00h	

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92h	TX_CTRL9			TX controls
Bit	Field name	Type	Por	
7	Iapcset_en	R/W	0	Control of the optical power current LUT 0: disable optical power current LUT 1: enable optical power current LUT
6:5	RESERVED	R/W	00	Internal use
4	TXD0_sleep1	R/W	0	Multiplexing control of PIN 10 0: as TX_DISABLE pin, SLEEP function is disable 1: SLEEP pin, TX_DISABLE function is enable
3	ModMaxProtect	R/W	0	The protection of the maximum Imod current in the closed loop 0: not protected 1: protection for maximum Imod current limit
2	RESERVED	R/W	0	Internal use
1	Io_on0_off1	R/W	0	Setting BEN OFF, whether the modulation current and the bias current is open 0: the current is still on, the output from the Ibenoff pin 1: current off
0	RESERVED	R/W	0	Internal use

93-94h	TX_PD			Internal use
Type	R/W	Por	0000h	

95h	TX_CTRL10			TX controls
Bit	Field name	Type	Por	
7:1	RESERVED	R/W	0000 000	Internal use
0	Imod_mon_en	R/W	0	Selects what RAW value is used for the TX Bias DDMI calibration calculation 0: the value of TX bias current 1: the value of TX bias and mod current

96h	TX_CTRL11			TX controls
Bit	Field name	Type	Por	
7:5	RESERVED	R/W	000	Internal use

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4	TX_EQ_EN	R/W	0	Control of the function of TX input equalization 0: disable TX input equalization 1: enable TX input equalization
3	TX_EQ_LUT_EN	R/W	0	Control of TX input equalization TLUT 0: disable TX input equalization TLUT 1: enable TX input equalization TLUT
2	TX_EMP_AMP_LUT_EN	R/W	0	Control of the TLUT function of increasing overshoot or undershoot compensation in TX data output 0: disable compensation 1: enable compensation
1	R114_SEL	R/W	0	Select the source of TX_eqset register 0: TX_eqset can be set from bits (3:0) of A2 lower-memory address 0x72 1: TX_eqset can be set from bits (7:4) of A2 lower-memory address 0x72
0	RESERVED	R/W	0	RESERVED

97h	TX_CTRL12			TX controls
Bit	Field name	Type	Por	
7:5	RESERVED	R/W	000	Internal use
4:0	RESERVED	R/W	00000	RESERVED

98h	RESERVED			RESERVED
Bit	Field name	Type	Por	
7:0	RESERVED	R/W	00h	Internal use

99h	TX_CTRL14			TX controls
Bit	Field name	Type	Por	
7	EMP_EN	R/W	0	Set to enable the function of increasing overshoot or undershoot compensation in TX data output
6	EMP_AMP(3)	R/W	0	Set the amplitude for overshoot or undershoot compensation in TX data output 0000: 0
5	EMP_AMP(2)	R/W	0	
4	EMP_AMP(1)	R/W	0	

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3	EMP_AMP(0)	R/W	0	0001: 1/40*IMOD 0010: 1/20*IMOD ... 1111: 15/40*IMOD
2:0	RESERVED	R/W	000	Internal use

9Ah	TX_CTRL15			TX controls
Bit	Field name	Type	Por	
7:2	RESERVED	R/W	000000	Internal use
1	Fapc_loadt	R/W	0	Fast APC setting time 0: 800ns 1: 1600ns
0	Dark_current_mode	R/W	0	Select the dark current precision mode 0: high precision mode 1: low precision mode

9Bh	TX_CTRL16			TX controls
Bit	Field name	Type	Por	
7:1	RESERVED	R/W	0000000	Internal use
0	TX_SLEEP_INV	R/W	0	TX_DIS/TX_SLP pin polarity selection 0: Low level TX work, high level off 1: High level TX work, low level off

9Ch	TX_CTRL17			TX controls
Bit	Field name	Type	Por	
7:1	RESERVED	R/W	0000000	Internal use
0	APC_CLK_SEL	R/W	0	APC clock set 0: 50us 1: 6.4us

9Dh	TX_CTRL18			TX controls
Bit	Field name	Type	Por	
7:2	RESERVED	R/W	000000	Internal use

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1	Starten	R/W	0	TX output enable bit 0: disable 1: enable
0	RESERVED	R/W	0	Internal use

9Eh	APD_DA_CTRL0			APD and DA controls
Bit	Field name	Type	Por	
7	CUR_THH(3)	R/W	0	Set the threshold of over-current protection 0000: 0.5mA 0001: 0.6mA 0010: 0.7mA …… 1111: 2mA
6	CUR_THH(2)	R/W	0	
5	CUR_THH(1)	R/W	0	
4	CUR_THH(0)	R/W	0	
3	RESERVED	R/W	0	Internal use
2	RESERVED	R/W	0	
1	RESERVED	R/W	0	
0	RESERVED	R/W	0	

9Fh	APD_TARGET 1			Set the upper 8 bits of constant APD target voltage
Type	R/W	Por	00h	

A0h	APD_TARGET 0			APD and DA controls
Bit	Field name	Type	Por	
7	RX_ovflag	R/W	0	Select the min value of the receive optical power when it is overflow 0: 0000h 1: 0001h
6	A0_dis	R/W	0	Set to mask the slave addressed A0h 0: disable 1: enable
5	APD_CTRL	R/W	0	Control of the APD voltage TLUT 0: enable APD voltage TLUT 1: disable APD voltage TLUT
4	Apd_fault_sel	R/W	0	Set to enable latching of fault signals. 0: latched 1: not latched
3	Apd_250us_sel(1)	R/W	0	Select the fast discharge time 00: 250us

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2	Apd_250us_sel(0)	R/W	0	01: 500us 10: 1000us 11: 2000us
1	APD_TARGET(1)	R/W	0	Set the lower 2 bits of constant APD target voltage
0	APD_TARGET(0)	R/W	0	

A1h	DROP_VALUE 1			Internal use
Type	R/W	Por	00h	

A2h	DROP_VALUE 0			APD and DA controls
Bit	Field name	Type	Por	
7	Temp_cal_sel	R/W	0	Set to select the temperature value for LUT index 0: the raw temperature value 1: the calibrated temperature value
6	RESERVED	R/W	0	Internal use
5	darkluten	R/W	0	Control of the dark current TLUT 0: disable dark current TLUT 1: enable dark current TLUT
4	Fast_discg_en	R/W	0	Control of the function of fast discharge 0: disable fast discharge 1: enable fast discharge
3:0	RESERVED	R/W	0000	Internal use

A3h	APD_DA_CTRL1			APD and DA controls
Bit	Field name	Type	Por	
7	BURP_RSTR_EN	R/W	0	Control of burp protection mode 0: disable burp protection 1: enable burp protection
6:0	RESERVED	R/W	0000000	Internal use

A4h	APD_DA_CTRL2			APD and DA controls
Bit	Field name	Type	Por	
7	Ocp_stup_en	R/W	0	Control of over-current detect When power up 0: disable over-current detect 1: enable over-current detect
6:5	RESERVED	R/W	00	Internal use

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4	RESET_DCDC	R/W	0	Soft reset signal of DCDC module 0: disable 1: enable
3	IRSSI_SEL(2)	R/W	0	Select the proportion of the RSSI current
2	IRSSI_SEL(1)	R/W	0	000:0
1	IRSSI_SEL(0)	R/W	0	001: RSSI*1/20 010: RSSI*2/20 011: RSSI*3/20 100: RSSI*4/20 101: RSSI*5/20 110: RSSI*6/20 111: RSSI*7/20
0	RESERVED	R/W	0	Internal use

A5h	APD_DA_CTRL3			APD and DA controls
Bit	Field name	Type	Por	
7	OVPCODE(2)	R/W	0	Select threshold for over-voltage protection
6	OVPCODE(1)	R/W	0	000: 1.05*set value
5	OVPCODE(0)	R/W	0	001: 1.075*set value 010: 1.1*set value 011: 1.125*set value 100: 1.15*set value 101: 1.175*set value 110: 1.2*set value 111: 1.25*set value
4	DUTYCODE(2)	R/W	0	Select the max duty cycle
3	DUTYCODE(1)	R/W	0	000: 45%
2	DUTYCODE(0)	R/W	0	001: 50% 010: 55% 011: 60% 100: 65% 101: 70% 110: 75% 111: 80%
1	PD_OVP	R/W	0	Set the enable the over-voltage protection function 0: enable 1: disable

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0	PD_OCP	R/W	0	Set the enable the over-current protection function 0: enable 1: disable

A6h	APD_DA_CTRL4			APD and DA controls
Bit	Field name	Type	Por	
7	RESERVED	R/W	0	RESERVED
6	Clk10k_sel	R/W	0	Select DCDC soft start time 0: 10ms 1: 20ms
5	PD_DCDC	R/W	0	DCDC module start-up enable bit 0: enable 1: disable
4	FRQSEL	R/W	0	Select the operating frequency 0: 250KHz 1: 500KHz
3:1	RESERVED	R/W	000	Internal use
0	FIX_ADJ_SEL	R/W	0	Select the mode of max duty cycle 0: fixed 1: variable

A7h	APD_DA_CTRL5			APD and DA controls
Bit	Field name	Type	Por	
7	DAO_OFFSET(3)	R/W	0	Add an offset value to DA output 1. Source full range DA mode 0000: 0
6	DAO_OFFSET(2)	R/W	0	
5	DAO_OFFSET(1)	R/W	0	

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4	DAO_OFFSET(0)	R/W	0	0001: 60.3uA 0010: 120.6uA …… 1111: 905uA 2. Sink full range DA mode 0000: 0 0001: 15.4uA 0010: 30.8uA …… 1111: 231uA ---------- 3. PWM voltage 0000: 0 0001: 38.75mV 0010: 77.5mV …… 1111: 581.25mV
3	DA0_PWM1	R/W	0	Select the output of APD_DA current/voltage 0: DA current output 1: PWM voltage output
2	ISIO_HALF	R/W	0	Select the output of DA current 0: full range 1: half range
1	ISIO_SEL	R/W	0	Select the output direction of DA current 0: sink 1: source
0	DA_LPOW	R/W	0	DA current start-up enable bit 0: normal 1: low power

A8h	ANA_CTRL			Analog controls
Bit	Field name	Type	Por	

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7	RX_SLEEP_CTRL	R/W	0	Set to control RX_SLEEP from the TX_DISABLE function (applies to both hard and soft controls) 0: disable 1: enable
6:1	RESERVED	R/W	000 000	Internal use
0	RX_NOPWR_ON_LOS	R/W	0	Set to report minimum Rx power when RX_LOS is set 0: normal 1: min

A9h	RX_CTRL1			RX controls
Bit	Field name	Type	Por	
7	AMPCTRL(2)	R/W	0	Set the LA output voltage amplitude 000: 300 mVppd 001: 400 mVppd 010: 500 mVppd 011: 600 mVppd 100: 700 mVppd 101: 800 mVppd 110: 900 mVppd 111: 1000 mVppd
6	AMPCTRL(1)	R/W	0	
5	AMPCTRL(0)	R/W	0	
4	Los_delatch(4)	R/W	0	Set the latch cycle of LOS release signal 00000: inhibit 00001: 12.8 us 00010: 25.6 us 00011: 38.4 us 00100: 51.2 us 00101: 64 us 00110: 76.8 us 00111: 89.6 us … 11111: 396.8us
3	Los_delatch(3)	R/W	0	
2	Los_delatch(2)	R/W	0	
1	Los_delatch(1)	R/W	0	
0	Los_delatch(0)	R/W	0	

AAh	RX_CTRL2			RX controls
Bit	Field name	Type	Por	

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7	DPOLCTRL	R/W	0	Set the RX output polarity 0: in-phase 1: reverse
6	RESERVED	R/W	0	RESERVED
5	DOC_DIS	R/W	0	Control of automatic compensation for DC offset 0: enable automatic compensation 1: disable automatic compensation
4	Los_latch(4)	R/W	0	Set the latch cycle of LOS alarm signal 00000: inhibit 00001: 12.8 us 00010: 25.6 us 00011: 38.4 us 00100: 51.2 us 00101: 64 us 00110: 76.8 us 00111: 89.6 us … 11111: 396.8us
3	Los_latch(3)	R/W	0	
2	Los_latch(2)	R/W	0	
1	Los_latch(1)	R/W	0	
0	Los_latch(0)	R/W	0	

ABh	RX_CTRL3			RX controls
Bit	Field name	Type	Por	
7	RX_EQ_EN	R/W	0	Control of RX input equalizer 0: disable RX input equalizer 1: enable RX input equalizer
6	RX_EQSETC(3)	R/W	0	Set to control RX input equalizer compensation 0001: 1.2dB 0101: 3.2dB 1011: 5dB 1111: 6dB
5	RX_EQSETC(2)	R/W	0	
4	RX_EQSETC(1)	R/W	0	
3	RX_EQSETC(0)	R/W	0	
2	PWROFF_EN	R/W	0	RX low-power mode control 0: RX power on 1: RX power off
1	ROPLOS_EN	R/W	0	Set to select the alarm mode of average optical power 0: OMA 1: ROP

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0	SQU_DIS	R/W	0	Control of RX output squelch due to the alarm of LOS 0: enable RX output squelch 1: disable RX output squelch

ACh	RX_CTRL4			RX controls
Bit	Field name	Type	Por	
7	Loslut_en	R/W	0	Control of LOS TLUT 0: disable LOS TLUT 1: enable LOS TLUT
6	LOSRANGE(1)	R/W	0	Set the range of the LOS Deassert thresholds 00: 10~25 mVppd 01: 20~60 mVppd 10: 40~120 mVppd 11: N.A
5	LOSRANGE(0)	R/W	0	
4	Lospolctrl	R/W	0	Set to control the LOS/SD output 0: LOS 1: SD
3	LSTAT_C	R/W	0	Set the polarity between the alarm register and LOS_SD pin 0: in-phase 1: reverse
2	HYSCTRL(2)	R/W	0	Set the alarm hysteresis 001: 1dB 011: 2dB 101: 2.5dB 111: 3dB
1	HYSCTRL(1)	R/W	0	
0	HYSCTRL(0)	R/W	0	

ADh	LOSCTRLC			The constant alarm threshold controls
Type	R/W	Por	00h	

AEh	RX_CTRL5			RX controls
Bit	Field name	Type	Por	
7	LOSFLT(1)	R/W	0	Set the filter time for the alarm signals 00: 3us 01: 6us 10: 9us 11: 12us
6	LOSFLT(0)	R/W	0	

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5	CTRL_IROP	R/W	0	Set to control the input resistor of LA Irop 0:auto control 1:set by bits 4 an bit 3 of register addressed AEh
4	IROPC(1)	R/W	0	Set the input level of LA monitor current 00: 80uA~2mA(-10~3dBm) 01: 10uA~112uA(-20~-8dBm) 10: 1.2uA~15uA(-30~-18dBm) 11: 0.1uA~1.9 uA(-38~-28dBm)
3	IROPC(0)	R/W	0	
2	TPEDLY(2)	R/W	0	Set the RX pre-emphasis delay 000: 1.2UI ... 101: 0.8UI
1	TPEDLY(1)	R/W	0	
0	TPEDLY(0)	R/W	0	

AFh	RX_CTRL6			RX controls
Bit	Field name	Type	Por	
7:3	RESERVED	R/W	00000	Internal use
2	TRIN(2)	R/W	0	Set the LA input impedance 000: 45 ohm ... 111: 65 ohm
1	TRIN(1)	R/W	0	
0	TRIN(0)	R/W	0	

B0h	SYS_CTRL1			System controls
Bit	Field name	Type	Por	
7	R115_SEL	R/W	0	Select the source of pectrl register 0: pectrl can be set from bits (3:0) of A2 lower-memory address 0x73 1: pectrl can be set from bits (7:4) of A2 lower-memory address 0x73
6	Vcc_temp_adj_sel(1)	R/W	0	Set the value to adjust the temperature varied inversely with voltage(3V~3.63V) 00: 0.25℃/50mV 01: 0.375℃/50mV 10: 0.5℃/50mV 11: 0.625℃/50mV
5	Vcc_temp_adj_sel(0)	R/W	0	
4	Vcc_temp_adj_en	R/W	0	Set to enable the function of adjusting the temperature varied inversely with voltage

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3	Rx_pe_lut_en	R/W	0	Control of RX PE LUT 0: disable PE LUT 1: enable PE LUT
2	Rx_eq_lut_en	R/W	0	Control of RX EQ TLUT 0: disable EQ TLUT 1: enable EQ TLUT
1:0	RESERVED	R/W	00	Internal use

B1h	SYS_CTRL2			System controls
Bit	Field name	Type	Por	
7	Sda_ctrl	R/W	0	Set the delay between slave SDA and SCL. 0: less than 300ns 1: greater than 300ns
6:3	RESERVED	R/W	0000	Internal use
2	rxsoftsleep_en	R/W	0	Control of whether RX is response for RX_SOFT_SLEEP bit 0: RX NOT response 1: RX response
1	tx_dis_sel	R/W	0	Set to whether the TX_DISABLE pin is included in the status of TX_DISABLE 0: exclude 1: include
0	tx_disable_set	R/W	0	Set the state of Tx disable signal located on 6Eh 0: TX DISABLE pin 1: Soft TX_disable is 'OR'd with the hard TX_DISABLE pin

B2h	SYS_CTRL8			System controls
Bit	Field name	Type	Por	
7:4	RESERVED	R/W	0000	Internal use
3	RREFSEL	R/W	0	Select the Multiplexing control of PIN

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2	EXT_SENSOR	R/W	0	ADC_IN 00:APD voltage input 01: external temperature sensor 10: external reference resistor 11: RESERVED
1:0	RESERVED	R/W	00	Internal use

B3h	TX_LOCK_TIMER			Set the hold-off time for TX optical power when BEN is off. One step is 105ms
Type	R/W	Por	00h	

B4h	SYS_CTRL3			System controls
Bit	Field name	Type	Por	
7:0	MEM_ACCESS0	R/W	00h	Please contract to UX for details

B5h	SYS_CTRL4			System controls
Bit	Field name	Type	Por	
7:0	MEM_ACCESS1	R/W	00h	Please contract to UX for details

B6h	SYS_CTRL5			System controls
Bit	Field name	Type	Por	
7:3	MEM_ACCESS2	R/W	00000	Please contract to UX for details
2	Table0_dis	R/W	0	Control of the Table 0 0: enable Table 0 1: disable Table 0
1:0	MEM_ACCESS3	R/W	00	Please contract to UX for details

B7h	SYS_CTRL6			System controls
Bit	Field name	Type	Por	
7	RESERVED	R/W	0	Internal use

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6	Cs_en	R/W	0	Chip address selected signal When the position is high, TX_DISABLE pin can be used as a chip address selected signal. When TX_DISABLE pin is high, the chip from the I2C communication will be banned. Note: when the power is on, the position is always zero.
5:1	MEM_ACCESS4	R/W	00000	Please contract to UX for details
0	EE_UPDATE_DIS	R/W	0	Control EEPROM updates of A0/A2h 0: enable EEPROM updates 1: disable EEPROM updates

B8h	TEMP_COMP1			High turning point of temperature internal calibration
Type	R/W	Por	00h	

B9h	TEMP_COMP0			Low turning point of temperature internal calibration
Type	R/W	Por	00h	

BA-BBh	TEMP_SLOPE2			Slope2 for temperature internal calibration
Type	R/W	Por	0000h	

BC-BDh	TEMP_OFFSET2			Offset2 for temperature internal calibration
Type	R/W	Por	0000h	

BE-BFh	TEMP_SLOPE1			Slope1 for temperature internal calibration
Type	R/W	Por	0000h	

C0-C1h	TEMP_OFFSET1			Offset1 for temperature internal calibration
Type	R/W	Por	0000h	

C2-C3h	TEMP_SLOPE0			Slope0 for temperature internal calibration
Type	R/W	Por	0000h	

C4-C5h	TEMP_OFFSET0			Offset0 for temperature internal calibration
Type	R/W	Por	0000h	

C6-C7h	VCC_SLOPE	Slope for supply voltage internal calibration

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Type	R/W	Por	0000h	

C8-C9h	VCC_OFFSET			Offset for supply voltage internal calibration
Type	R/W	Por	0000h	

CA-CBh	BIAS_SLOPE			Slope for bias current internal calibration
Type	R/W	Por	0000h	

CC-CDh	BIAS_OFFSET			Offset for bias current internal calibration
Type	R/W	Por	0000h	

CE-CFh	Tx_SLOPE			Slope for transmit power internal calibration
Type	R/W	Por	0000h	

D0-D1h	Tx_OFFSET			Offset for transmit power internal calibration
Type	R/W	Por	0000h	

D2-D3h	Rx_SLOPE2			Slope2 for received power internal calibration
Type	R/W	Por	0000h	

D4-D5h	Rx_OFFSET2			Offset2 for received power internal calibration
Type	R/W	Por	0000h	

D6-D7h	Rx_SLOPE1			Slope1 for received power internal calibration
Type	R/W	Por	0000h	

D8-D9h	Rx_OFFSET1			Offset1 for received power internal calibration
Type	R/W	Por	0000h	

DA-DBh	Rx_SLOPE0			Slope0 for received power internal calibration
Type	R/W	Por	0000h	

DC-DDh	Rx_OFFSET0			Offset0 for received power internal calibration
Type	R/W	Por	0000h	

DE-DFh	RX_COMP1			High turning point of received power internal calibration
Type	R/W	Por	0000h	

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E0-E1h	RX_COMP0			Low turning point of received power internal calibration
Type	R/W	Por	0000h	

E2h	SYS_CTRL7			System controls
Bit	Field name	Type	Por	
7	Tx_threshold(3)	R/W	0	Set the threshold of TX POWER, when the raw ADC value is below it, TX POWER is reported to zero.
6	Tx_threshold(2)	R/W	0	
5	Tx_threshold(1)	R/W	0	
4	Tx_threshold(0)	R/W	0	
3	Rx_threshold(3)	R/W	0	Set the threshold of RX POWER, when the calibration ADC value is below it, RX POWER is reported to zero.
2	Rx_threshold(2)	R/W	0	
1	Rx_threshold(1)	R/W	0	
0	Rx_threshold(0)	R/W	0	

E3h	Timer			Set the interrupt time of I2C slaver, 1LSB is about 13ms, the maximum interrupt time is 3.3s
Type	R/W	Por	00h	

E4h	SLVAE_ADDRESS			The two-wire serial slave interface address. The two least significant bits will be saved as zeros. The saved address is thus a new A0h address.A2h is always slaveaddress+2
Type	R/W	Por	A2h	

E5h	DDM_CTRL			DDM controls
Bit	Field name	Type	Por	
7	RESERVED	R/W	0	Internal use
6	IN	R/W	0	Set to select calibration mode 0: external calibration 1: internal calibration
5	DEBUG_EN	R/W	0	Set to enable the debug mode 0: normal mode 1: debug mode
4	SD_ROGUE_C	R/W	0	PIN 21 output select 0: TX_SD 1: ROGUE_ONU
3	AMUX_ADDR(3)	R/W	0	Set the amux address for debug mode 0000: Temperature 0001: VDD 0010: BIAS
2	AMUX_ADDR(2)	R/W	0	

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1	AMUX_ADDR(1)	R/W	0	0011: MD 0100: ROP 0101: NC 0110: NC 0111: NC 1000: VCF 1001: Vassert_la 1010: Vdeassert_la 1011: DAO 1100: VAPCH 1101: Vbg_la 1110: NC 1111: NC
0	AMUX_ADDR(0)	R/W	0	

E6h	EEPROMchksum			Contains the low order 8 bits of the sum of table 81h(80h-E8h)，table 82h(80h-E8h)，table 83h(80h-E8h)，table 84h(80h-D3h,D6h-DDh,E0h-EAh) ,table 85h(80h-94h,A0h-AAh,B0h-B7h,C0h-D4h),table 86h(80h-A9h) and table 80h(81h-B6h,B8h-E5h)
Type	R/W	Por	00h	

E7-EAh	PW1			Level 1 access password (PW1)
Type	R/W	Por	00000000h	

EB-EEh	PW2			Level 2 access password (PW2)
Type	R/W	Por	00000000h	

EFh	TX_STATUS1			TX fault status indicator register
Bit	Field name	Type	Por	
7	RESERVED	R	0	RESERVED
6	Fault(6)	R	0	TX fault status indicate 0: No alarm 1: Alarm Fault(0): VDD>4.3V Fault(1): Whether internal current source is working properly Fault(2): LDOP or LDON short to ground Fault(3): BIASP short to ground Fault(4): BIAS >= BIASMAX
5	Fault(5)	R	0	
4	Fault(4)	R	0	
3	Fault(3)	R	0	
2	Fault(2)	R	0	

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1	Fault(1)	R	0	Fault(5): When a rogue ONU is detected(BEN signal is low and the TX_SD signal is high) Fault(6): Light-emitting detection
0	Fault(0)	R	0	

F0h	BiasCT_R1			The bias current DA high 8-bit display registers
Type	R	Por	00h	

F1h	BiasCT_R0			TX status registers
Bit	Field name	Type	Por	
7:4	RESERVED	R	0000	RESERVED
3	benalarm	R	0	Reports the current status of the BEN function
2	txsdalarm	R	0	Reports current status of the TX_SD pin
1	BIASCT_R(1)	R	0	The bias current DA low 2 bit status value
0	BIASCT_R(0)	R	0	

F2h	IMOD_DAC1			The I_{mod} current DA high 8-bit display registers
Type	R	Por	00h	

F3h	IMOD_DAC0			The I_{mod} current DA low bit display registers
Bit	Field name	Type	Por	
7:2	RESERVED	R	000000	RESERVED
1	IMOD_DAC(1)	R	0	The I_{mod} current DA low 2 bit status value
0	IMOD_DAC(0)	R	0	

F4h	STATUS0			Status register
Bit	Field name	Type	Por	
7:6	RESERVED	R	00	RESERVED
5	Dcdc_state	R	0	DCDC lpow status bit
4	DA_STATE	R	0	DA lpow status bit
3	LA_STATE	R	0	RX lpow status bit
2	TX_STATE	R	0	TX lpow status bit
1	ROP_STATE(1)	R	0	The status of IROP current
0	ROP_STATE(0)	R	0	

F5h	STATUS1			Status register
Bit	Field name	Type	Por	

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7	RESERVED	R	0	RESERVED
6	OCP_LATCH	R	0	latched when over-current
5	OVP_LATCH	R	0	latched when over-voltage
4	ONCE_PROTECT	R	0	One-time alarm mode flag 0: normal 1: alarm
3	BURP_RSTR_FORBID	R	0	Whether Burp restart is counted 3 times 0: no 1: yes
2	LOWERPOW_NEED	R	0	Whether the voltage is over the lower threshold 0: normal 1: over
1	OCP_SMART_FORBID	R	0	Whether smart over-current protection is forbidden 0: normal 1: forbid
0	OVER_HICTH	R	0	Whether the voltage is over the high threshold 0: normal 1: over

F6h	STATUS2			Status register
Bit	Field name	Type	Por	
7:5	RESERVED	R	000	RESERVED
4	Fast_discg	R	0	Fast discharge flag 0: normal 1: discharge
3	VPWM_ABLE	R	0	VPWM output enable flag 0: disable 1: enable
2	OCP_OUT	R	0	The status of over-current signal 0: normal 1: over
1	OVP_OUT	R	0	The status of over-voltage signal 0: normal 1: over

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0	SS_FINISH	R	0	Soft start finish flag 0: not finished 1: finished

F7h	TEMP_DATA1			Indicate the upper 8 bits value of the sampled temperature
Type	R	Por	00h	

F8h	TEMP_DATA0			Indicate the low bit value of the sampled temperature
Bit	Field name	Type	Por	
7:1	RESERVED	R	0000000	RESERVED
0	TEMP_DATA (0)	R	0	Indicate the lower bit value of the sampled temperature

F9-FAh	RX_ADC_VALUE			Indicate the ADC value of the sampled RX POWER, high byte in low address
Type	R	Por	0000h	

FBh	APD_VOL1			Indicate the upper 8 bits register of the sampled APD voltage
Type	R	Por	00h	

FCh	APD_VOL0			Indicate the low bit value of the sampled APD voltage
Bit	Field name	Type	Por	
7:1	RESERVED	R	0000000	RESERVED
0	APD_VOL (0)	R	0	Indicate the low bit value of the sampled APD voltage

FDh	SYS_STATUS			The register indicates the current password access level
Bit	Field name	Type	Por	
7	eerxfailflag9	R	0	the bit is set to '1' by the device if the data of table 85h written to EEPROM fails to its check.
6	eerxfailflag8	R	0	the bit is set to '1' by the device if the data of table 84h written to EEPROM fails to its check.
5	EEPROM_FAIL4	R	0	The bit is set to '1'by the device if the DMA from the A8 region of EEPROM does not complete successfully
4:2	RESERVED	R	000	RESERVED

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1	Security(1)	R	0	Indicate the current password access level 00: user level 01: level 1 10: level 2 11: undefined
0	Security(0)	R	0	

FEh	INIT_STATE			The most significant four bits indicating EEPROM DMA load fail ('1' = no response from EEPROM during power up), The least significant four bits indicating Data structure corrupt ('1' = data integrity bytes read from EEPROM during power up are incorrect).
Bit	Field name	Type	Por	
7	EEPROM_FAIL3	R	0	The bit is set to '1'by the device if the DMA from the A6 region of EEPROM does not complete successfully
6	EEPROM_FAIL2	R	0	The bit is set to '1'by the device if the DMA from the A4 region of EEPROM does not complete successfully
5	EEPROM_FAIL1	R	0	The bit is set to '1' by the device if the DMA from the A2 region of EEPROM does not complete successfully
4	EEPROM_FAIL0	R	0	The bit is set to '1' by the device if the DMA from the A0 region of EEPROM does not complete successfully
3	dsfail3	R	0	The bit is set to '1' by the device if the data from the A4 and A6 region of eeprom fails its integrity check
2	dsfail2	R	0	The bit is set to '1' by the device if the data from the A2 lower region of eeprom fails its integrity check
1	dsfail1	R	0	The bit is set to '1' by the device if the data from bytes 64-94h in A0 region of eeprom fails its integrity check
0	dsfail0	R	0	The bit is set to '1' by the device if the data from bytes 0-62h in A0 region of eeprom fails its integrity check

FFh	EEPROM_FAIL_FLAG1			The register indicate Whether the data is written to EEPROM
Bit	Field name	Type	Por	

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7	eerxfailflag7	R	0	the bit is set to '1' by the device if the data of table 83h written to EEPROM fails to its check.
6	eerxfailflag6	R	0	the bit is set to '1' by the device if the data of table 82h written to EEPROM fails to its check.
5	eerxfailflag5	R	0	the bit is set to '1' by the device if the data of table 81h written to EEPROM fails to its check.
4	eerxfailflag4	R	0	the bit is set to '1' by the device if the data of table 80h written to EEPROM fails to its check.
3	eerxfailflag3	R	0	the bit is set to '1' by the device if the data of table 0 written to EEPROM fails to its check.
2	eerxfailflag2	R	0	the bit is set to '1' by the device if the data of A2 lower region written to EEPROM fails to its check.
1	eerxfailflag1	R	0	the bit is set to '1' by the device if the data of A0 upper region written to EEPROM fails to its check.
0	eerxfailflag0	R	0	the bit is set to '1' by the device if the data of A0 lower region written to EEPROM fails to its check.

Table 84h:

80-D3h	APC TLUT			Temperature Indexed APC current Look-Up Table
Type	R/W	Por	00h	

D4h	PA_SET1			PA current displaying register
Bit	Field name	Type	Por	
7:0	PA_SET(9:2)	R	00h	The upper bits of PA current

D5h	PA_SET0			System controls
Bit	Field name	Type	Por	
7	PA_SET(1)	R	0	The lower bits of PA current
6	PA_SET(0)	R	0	
5:0	Reserved	R	000000	Reserved

D6-DDh	TX EQ LUT			TX EQ decoder
Type	R/W	Por	00h	

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DEh	TX_EQSET			TX EQ displaying register
Bit	Field name	Type	Por	
7:4	RESERVED	R	0000	RESERVED
3	TX_EQSET(3)	R	0	The value of TX equalizer
2	TX_EQSET(2)	R	0	
1	TX_EQSET(1)	R	0	
0	TX_EQSET(0)	R	0	

DFh	RESERVED			RESERVED
Type	R/W	Por	00h	

E0h	TX_EMP_THR			Set the temperature thresthold value of Tx emp Tlut
Bit	Field name	Type	Por	
7	TX_EMP_TEMP_THR(6)	R/W	0	Set the temperature thresthold value of Tx emp Tlut
6	TX_EMP_TEMP_THR(5)	R/W	0	
5	TX_EMP_TEMP_THR(4)	R/W	0	
4	TX_EMP_TEMP_THR(3)	R/W	0	
3	TX_EMP_TEMP_THR(2)	R/W	0	
2	TX_EMP_TEMP_THR(1)	R/W	0	
1	TX_EMP_TEMP_THR(0)	R/W	0	
0	RESERVED	R/W	0	RESERVED

E1h	SYS_CTRL9			System controls
Bit	Field name	Type	Por	
7	rx_data_hold_sel(2)	R/W	0	Set the Hysteresis range of rx power 000:disable 001:0.1dBm 010:0.15dBm 011:0.2dBm 100:0.25dBm 101:0.3dBm 110:0.35dBm 111:0.4dBm
6	rx_data_hold_sel(1)	R/W	0	
5	rx_data_hold_sel(0)	R/W	0	
4	tx_data_hold_sel(2)	R/W	0	Set the Hysteresis range of tx power 000:disable
3	tx_data_hold_sel(1)	R/W	0	

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2	tx_data_hold_sel(0)	R/W	0	001:0.1dBm 010:0.15dBm 011:0.2dBm 100:0.25dBm 101:0.3dBm 110:0.35dBm 111:0.4dBm
1:0	RESERVED	R/W	00	Internal use

E2h	SYS_CTRL10			System controls
Bit	Field name	Type	Por	
7:3	RESERVED	R/W	0000 0	Internal use
2	SD_C(1)	R/W	0	TX_SD time constant debugging bit 00:min delay 11:max delay
1	SD_C(0)	R/W	0	
0	RESERVED	R/W	0	Internal use

E3h	DOCSETC			Set the constant DAC value of TX DC offset
Type	R/W	Por	00h	

E4h	TX_CTRL19			TX controls
Bit	Field name	Type	Por	
7	DCD_EN	R/W	0	Control of the function of TX DCD 0:disable TX DCD 1:enable TX DCD
6	DOC_EN	R/W	0	Control of the function of TX auto DC offset 0:disable TX auto DC offset 1:enable TX auto DC offset
5:2	RESERVED	R/W	0000	Internal use
1	FAPC_CLK(1)	R/W	0	Set fast APC clock 00: 88ns 01: 94ns 10: 120ns 11: 180ns
0	FAPC_CLK(0)	R/W	0	

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E5h	TX_CTRL20			TX controls
Bit	Field name	Type	Por	
7	IMD_LOW1	R/W	0	Set MD current range 0: 0~1500uA 1: 0~370uA
6	RESERVED	R/W	0	Internal use
5	MD_PN	R/W	0	Set to select the direction of MD current 0:source 1:sink
4:1	RESERVED	R/W	0000	Internal use
0	tx_ovflag	R/W	0	Select the min value of the transmit optical power when it is overflow 0: 0000h 1: 0001h

E6h	TX_CTRL21			TX controls
Bit	Field name	Type	Por	
7	RC_LDOP(1)	R/W	0	Set to trimming the RC filter of TX LDOP 00:disable 01:250fF 10:500fF 11:750fF
6	RC_LDOP(0)	R/W	0	
5	RC_LDON(1)	R/W	0	Set to trimming the RC filter of TX LDON 00:disable 01:250fF 10:500fF 11:750fF
4	RC_LDON(0)	R/W	0	
3:2	RESERVED	R/W	00	Internal use
1	Autodoc_rst	R/W	0	Set the reset signal of automatic compensation function for DC. 0:Normal. 1:RST.

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0	Autodoc_enable	R/W	0	Set to select the compensation function for DC. 0:manual 1:auto

E7h	RESERVED			Internal use
Type	R/W	Por	00h	

E8h	TX_CTRL22			TX controls
Bit	Field name	Type	Por	
7: 3	RESERVED	R/W	0	Internal use
2	ACT_DL_LBW(2)	R/W	0	Set to trimming the delay of low rate channel 000:260ps 001:275ps 010:290ps 011:305ps 100:320ps 101:335ps 110:350ps 111:365ps
1	ACT_DL_LBW(1)	R/W	0	
0	ACT_DL_LBW(0)	R/W	0	

E9h	TX_CTRL23			TX controls Internal use
Bit	Field name	Type	Por	
7:0	RESERVED	R/W	00h	Internal use

EAh	Vdcdc			Set duty-cycle distortion of eye diagram. If the TX power ddm value should be right even no ac input, the value of Vdcdc should be probably set to 80h.
Type	R/W	Por	00h	

EBh	TX_STATUS2			TX status indicator register
Bit	Field name	Type	Por	
7	RESERVED	R	0	RESERVED
6:2	RESERVED	R	00000	Internal use

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1	Autodoc_en	R	0	Indicate the enable state of automatic compensation function for DC. 0:Disable. 1:Enable.
0	RESERVED	R	0	Internal use

ECh	DOCSET			Set the DAC value of TX DC offset
Type	R	Por	00h	

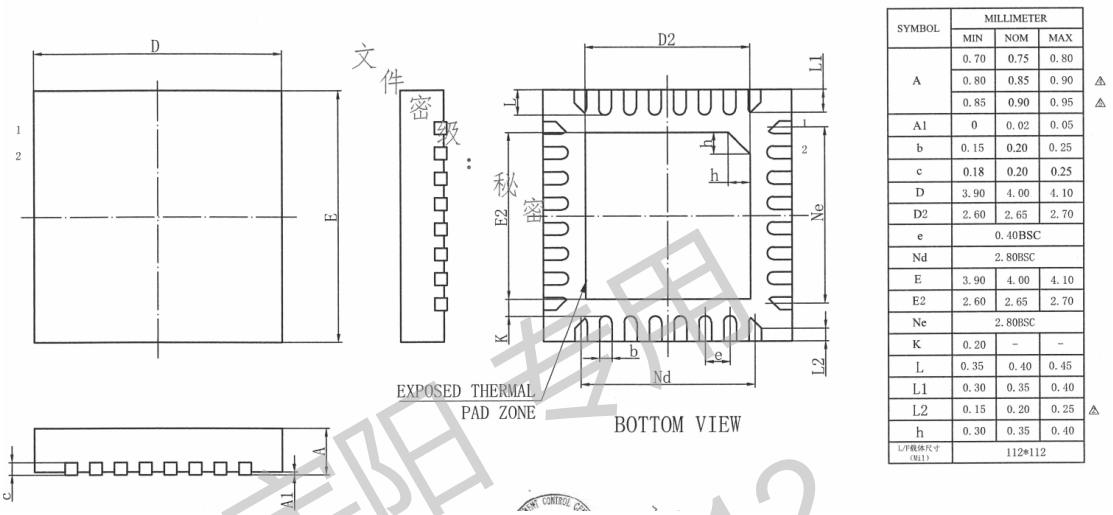
ED-FFh	RESERVED			RESERVED
Type	R	Por	FFh	

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Package information

UX3361 is a 4mm*4mm, 32-pin QFN.



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
	0.80	0.85	0.90
	0.85	0.90	0.95
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.60	2.65	2.70
e	0.40BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.60	2.65	2.70
Ne	2.80BSC		
K	0.20	-	-
L	0.35	0.40	0.45
L1	0.30	0.35	0.40
L2	0.15	0.20	0.25
h	0.30	0.35	0.40
L/F载体尺寸 (MIL)	112*112		

Figure 0-1. Package Information

All dimensions in mm.

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Modify Record

Version Number	Modify Content	Modify time
V0.1	Original version	2021-05-10
V0.2	Reg Description and default setting	2021-05-26
V0.3	Reg Description and default setting	2021-05-31
V0.4	Reg Description	2022-01-20
V1.0	Initial Release	2022-01-25
V1.01	Detail description 4.9.1	2022-02-21
V1.02	Update Detail description A7h Bit7-4	2022-09-16
V1.1	Add transmitter input level spec	2022-11-02
V1.2	Update package information	2023-05-04
V1.21	Corrected typo	2023-08-01

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